HARRIS SEMICONDUCTOR

CD74FCT827T, CD74FCT828T, CD74FCT2827T, CD74FCT2828T

August 1996

Fast CMOS 10-Bit Buffers

Features

- Advanced 0.8 micron CMOS Technology
- These Devices are Pin Compatible with Bipolar FAST™ Series at a Higher Speed And Lower Power Consumption
- 25Ω Series Resistor on All Outputs (CD74FCT2827T, CD74FCT2828T Only)
- TTL Input and Output Levels
- Low Ground Bounce Outputs
- Extremely Low Static Power
- Hysteresis on All Inputs

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT827ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT827ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT827BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT827BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT827CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT827CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT828ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT828ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT828BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT828BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT828CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT828CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2827ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2827ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2827BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2827BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2827CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2827CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2828ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2828ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2828BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2828BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2828CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2828CTQM	-40 to 85	24 Ld QSOP	M24.15-P

NOTE: QSOP is commonly known as SSOP.

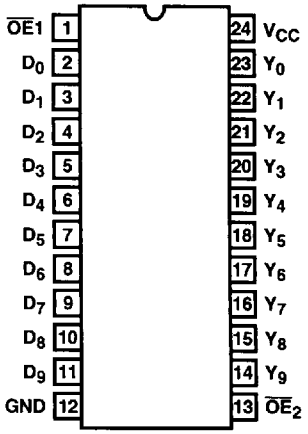
Description

These devices are 10-bit wide bus drivers providing high-performance bus interface buffering for wide address/data paths or buses carrying parity. The 10-bit buffers have NAND-ed output enables for maximum control flexibility. They are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. The CD74FCT827T and CD74FCT2827T are non-inverting versions of the CD74FCT828T and CD74FCT2828T.

All CD74FCT2827T and CD74FCT2828T devices have a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

Pinout

CD74FCT827T, CD74FCT828T, CD74FCT2827T, CD74FCT2828T (QSOP, SOIC)
TOP VIEW

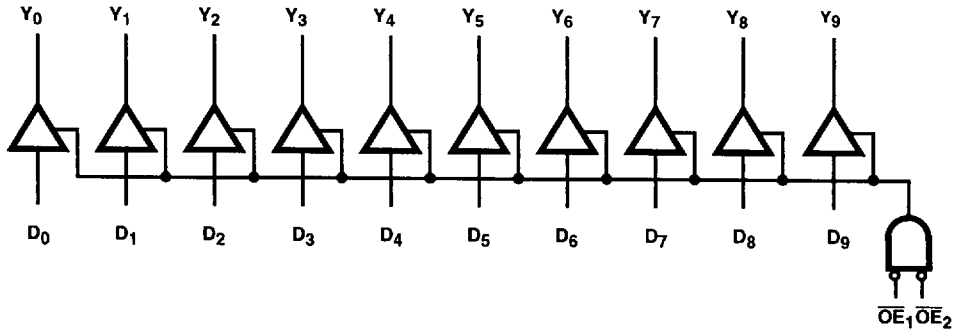


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
FAST™ is a trademark of Fairchild Semiconductor.

File Number **4179.1**

Functional Block Diagram

CD74FCT827T



TRUTH TABLE (NOTE 1)

FUNCTION	Inputs			Outputs
	$\overline{OE}_1$	$\overline{OE}_2$	D_N	Y_N
CD74FCT827T, CD74FCT2827T (Non-Inverting)				
Transparent	L	L	L	L
	L	L	H	H
Three-State	H	X	X	Z
	X	H	X	Z
CD74FCT828T, CD74FCT2828T (Inverting)				
Transparent	L	L	L	H
	L	L	H	L
Three-State	H	X	X	Z
	X	H	X	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{OE}_N$	Output Enable Input (Active LOW)
D_0-D_9	10-Bit Data Inputs
Y_0-Y_9	10-Bit Data Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs & V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs & D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
SOIC Package 75
QSOP Package 100
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETERS	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA	-	0.3	0.50	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA (25Ω Series)	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}		V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 6)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 7)	-	0.5	2.5	mA

Electrical Specifications (Continued)

PARAMETERS	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Supply Current per Input per MHz (Note 8)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OE}_1$ or $\overline{OE}_2$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	0.15	0.25	mA/ MHz
Total Power Supply Current (Note 10)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{OE}_1$ or $\overline{OE}_2$ = GND f_i = 5MHz One Bit toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	-	1.7	4.0 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	2.0	5.0 (Note 9)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{OE}_1$ or $\overline{OE}_2$ = GND Eight Bits Toggling f_i = 2.5MHz 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	3.2	6.5 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	5.2	14.5 (Note 9)	mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	AT		BT		CT		UNITS
			(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	
CD74FCT827T, CD74FCT2827T									
Propagation Delay D_N to Y_N	t_{PLH}, t_{PHL}	C_L = 50 pF R_L = 500Ω	1.5	6.5	1.5	5.0	1.5	4.4	ns
		C_L = 300 pF (Note 13) R_L = 500Ω	1.5	15.0	1.5	13.0	1.5	10.0	ns
Output Enable Time $\overline{OE}_N$ to Y_N	t_{PZH}, t_{PZL}	C_L = 50 pF R_L = 500Ω	1.5	9.5	1.5	8.0	1.5	7.0	ns
		C_L = 300 pF (Note 13) R_L = 500Ω	1.5	23.0	1.5	15.0	1.5	14.0	ns
Output Disable Time $\overline{OE}_N$ to Y_N (Note 13)	t_{PHZ}, t_{PLZ}	C_L = 5 pF (Note 13) R_L = 500Ω	1.5	8.5	1.5	6.0	1.5	5.7	ns
		C_L = 50 pF R_L = 500Ω	1.5	10.0	1.5	7.0	1.5	6.0	ns
CD74FCT828T, CD74FCT2828T									
Propagation Delay D_N to Y_N	t_{PLH}, t_{PHL}	C_L = 50 pF R_L = 500Ω	1.5	6.5	1.5	5.5	1.5	4.4	ns
		C_L = 300 pF (Note 13) R_L = 500Ω	1.5	15.0	1.5	13.0	1.5	10.0	ns

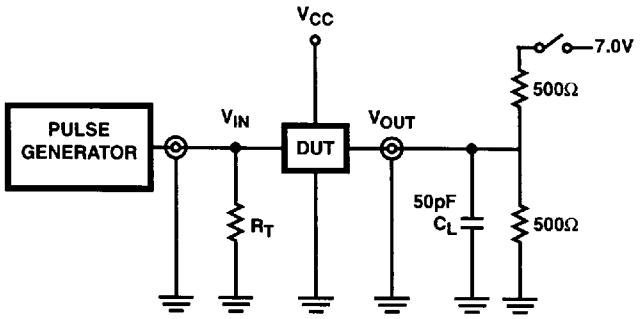
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	AT (NOTE 12) MIN	AT MAX	BT (NOTE 12) MIN	BT MAX	CT (NOTE 12) MIN	CT MAX	UNITS
Output Enable Time $\overline{OE}_N$ to Y_N	t_{PZH}, t_{PZL}	C_L = 50 pF, R_L = 500Ω	1.5	9.5	1.5	8.0	1.5	7.0	ns
		C_L = 300 pF (Note 13), R_L = 500Ω	1.5	23.0	1.5	15.0	1.5	14.0	ns
Output Disable Time $\overline{OE}_N$ to Y_N (Note 13)	t_{PHZ}, t_{PLZ}	C_L = 5 pF (Note 13), R_L = 500Ω	1.5	8.5	1.5	6.0	1.5	5.7	ns
		C_L = 50 pF, R_L = 500Ω	1.5	10.0	1.5	7.0	1.5	6.0	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Characteristics for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is determined by device characterization but is not production tested.
7. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
9. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
11. See test circuit and wave forms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. This parameter is guaranteed but not production tested.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

14. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

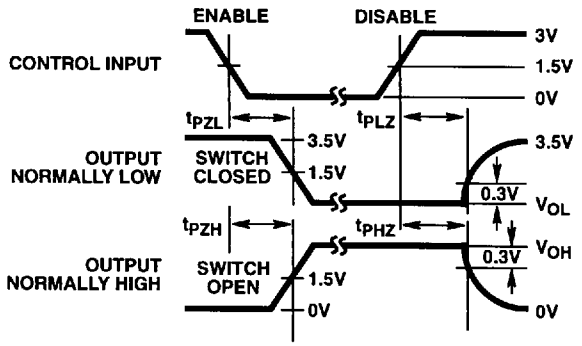


FIGURE 2. ENABLE AND DISABLE TIMING

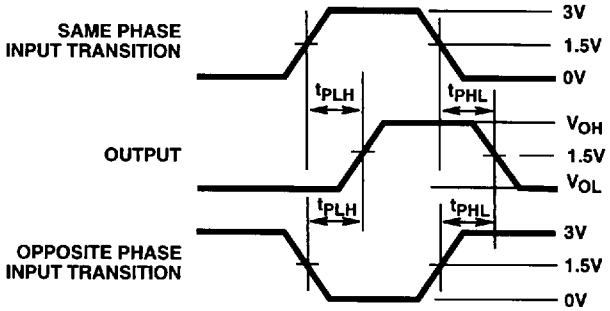
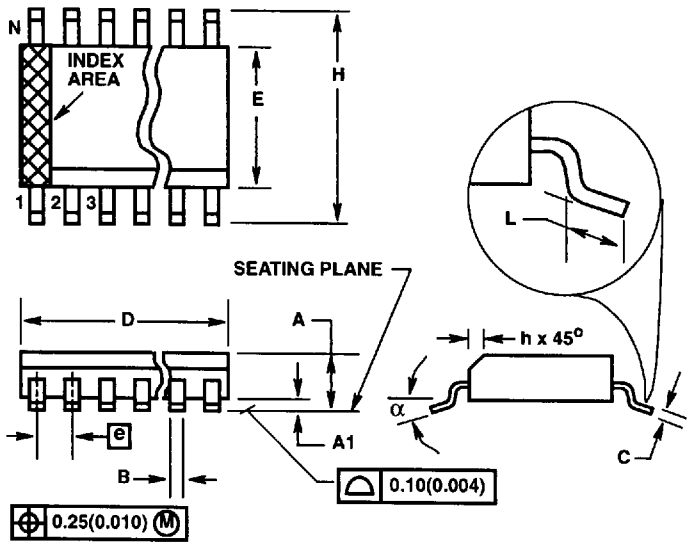


FIGURE 3. PROPAGATION DELAY

Small Outline Plastic Packages (SOIC)



M24.3-P

24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

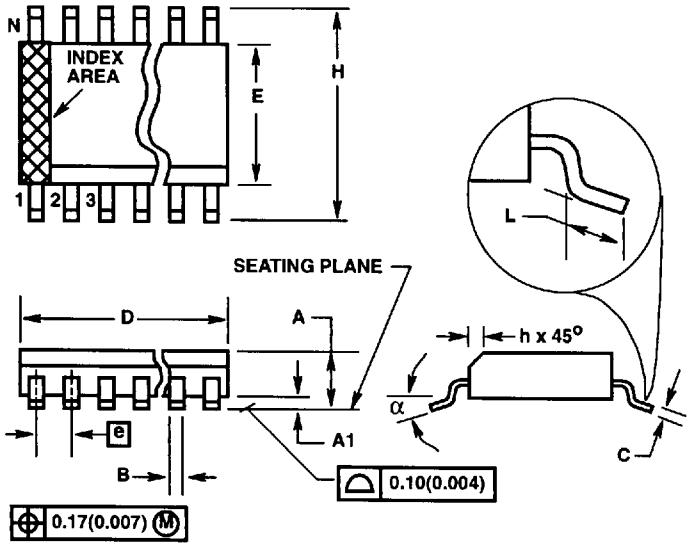
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.092	0.105	2.34	2.67	-
A1	0.004	0.012	0.102	0.302	-
B	0.013	0.020	0.330	0.508	-
C	0.009	0.011	0.229	0.279	-
D	0.598	0.614	15.19	15.60	1
E	0.291	0.299	7.39	7.59	2
e	0.050 BSC		1.27 BSC		-
H	0.401	0.411	10.18	10.44	-
h	0.010	0.029	0.254	0.737	-
L	0.016	0.050	0.41	1.27	3
N	24		24		4
α	0^o	8^o	0^o	8^o	-

Rev. 0 5/96

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs.
2. Dimension "E" does not include interlead flash or protrusions.
3. "L" is the length of terminal for soldering to a substrate.
4. "N" is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

Shrink Small Outline Plastic Packages (SSOP/QSOP)



M24.15-P

24 LEAD SHRINK NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.007	0.011	0.178	0.279	-
B	0.008	0.012	0.203	0.305	-
C	0.007	0.010	0.178	0.254	-
D	0.337	0.344	8.56	8.74	1
E	0.149	0.157	3.78	3.99	2
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.79	6.20	-
h	0.015		0.38		-
L	0.016	0.050	0.41	1.27	3
N	24		24		4
α	0^o	8^o	0^o	8^o	-

Rev. 1 7/96

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs.
2. Dimension "E" does not include interlead flash or protrusions.
3. "L" is the length of terminal for soldering to a substrate.
4. "N" is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

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NORTH AMERICA
Harris Semiconductor
P. O. Box 883, Mail Stop 53-210
Melbourne, FL 32902
TEL: 1-800-442-7747
(407) 729-4984
FAX: (407) 729-5321

EUROPE
Harris Semiconductor
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Harris Semiconductor PTE Ltd.
No. 1 Tannery Road
Cencon 1, #09-01
Singapore 1334
TEL: (65) 748-4200
FAX: (65) 748-0400

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