NEC

MOS INTEGRATED CIRCUIT

μPD23C8001EJ

8M-BIT MASK-PROGRAMMABLE ROM
1M-WORD BY 8-BIT

Description

The μPD23C8001EJ is a 8,388,608 bits (1,048,576 words by 8 bits) mask-programmable ROM.

The active levels of OE (Output Enable Input) can be selected with mask-option.

The μPD23C8001EJ is packed in 32-pin plastic DIP, 32-pin plastic SOP and 32-pin plastic TSOP (I).

Features

- Word organization : 1,048,576 words by 8 bits
- Operating supply voltage : 5.0 V ± 0.5 V

Operating supply voltage V_{CC}	Access time ns (MAX.)	Power supply current (Active mode) mA (MAX.)	Standby current (CMOS level input) μA (MAX.)
5.0 V ± 0.5 V	120	50	100

Ordering Information

Part number	Package
μPD23C8001EJCZ-xxx	32-pin plastic DIP (600 mil)
μPD23C8001EJGW-xxx	32-pin plastic SOP (525 mil)
μPD23C8001EJGU-xxx-9JH	32-pin plastic TSOP (I) (8 × 13.4 mm) (Normal bent)
μPD23C8001EJGU-xxx-9KH	32-pin plastic TSOP (I) (8 × 13.4 mm) (Reverse bent)

(xxx : ROM code suffix No.)

The information in this document is subject to change without notice.

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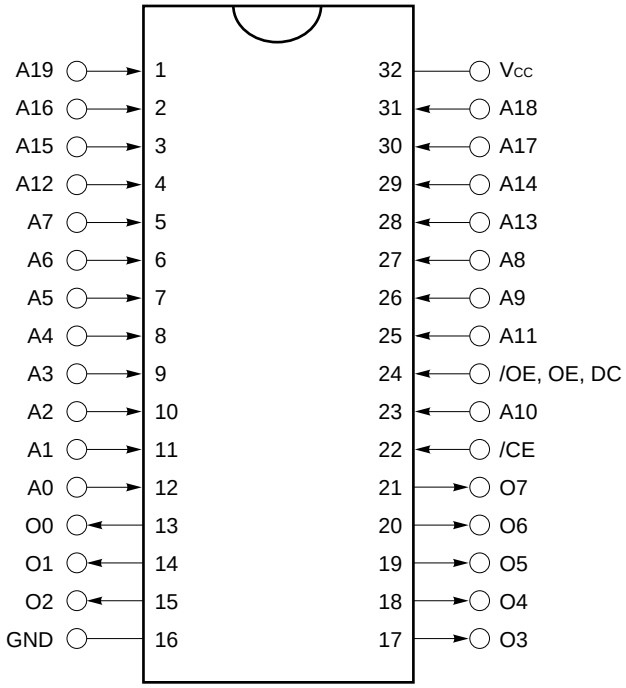
The mark ★ shows major revised points.

Pin Configuration (Marking Side)

/xxx indicates active low signal.

32-pin Plastic DIP (600 mil)
[μPD23C8001EJCZ]

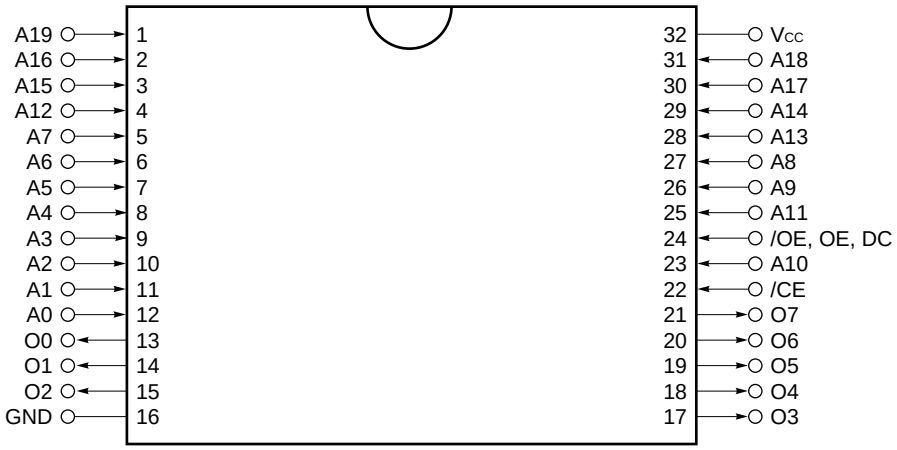
32-pin Plastic SOP (525 mil)
[μPD23C8001EJGW]



A0 - A19	:	Address inputs
O0 - O7	:	Data Outputs
/CE	:	Chip Enable
/OE, OE	:	Output Enable
VCC	:	Supply Voltage
GND	:	Ground
DC	:	Don't Care

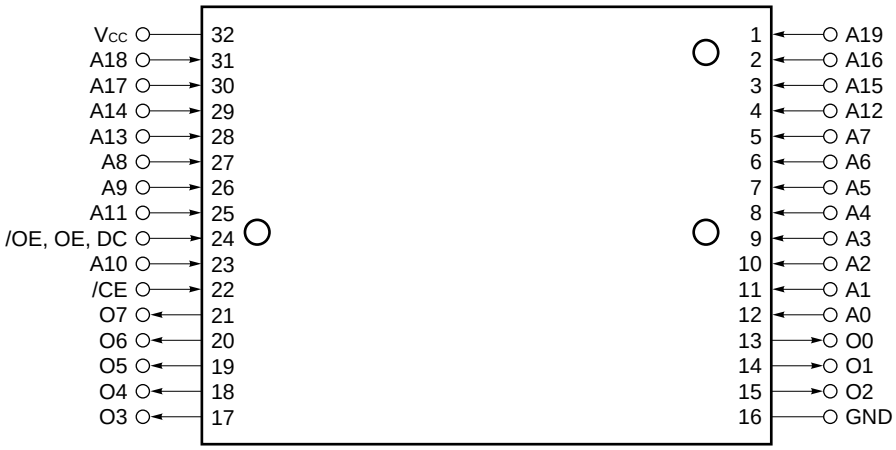
32-pin Plastic TSOP (I) (8 × 13.4 mm) (Normal Bent)

[μPD23C8001EJGU-9JH]



32-pin Plastic TSOP (I) (8 × 13.4 mm) (Reverse Bent)

[μPD23C8001EJGU-9KH]

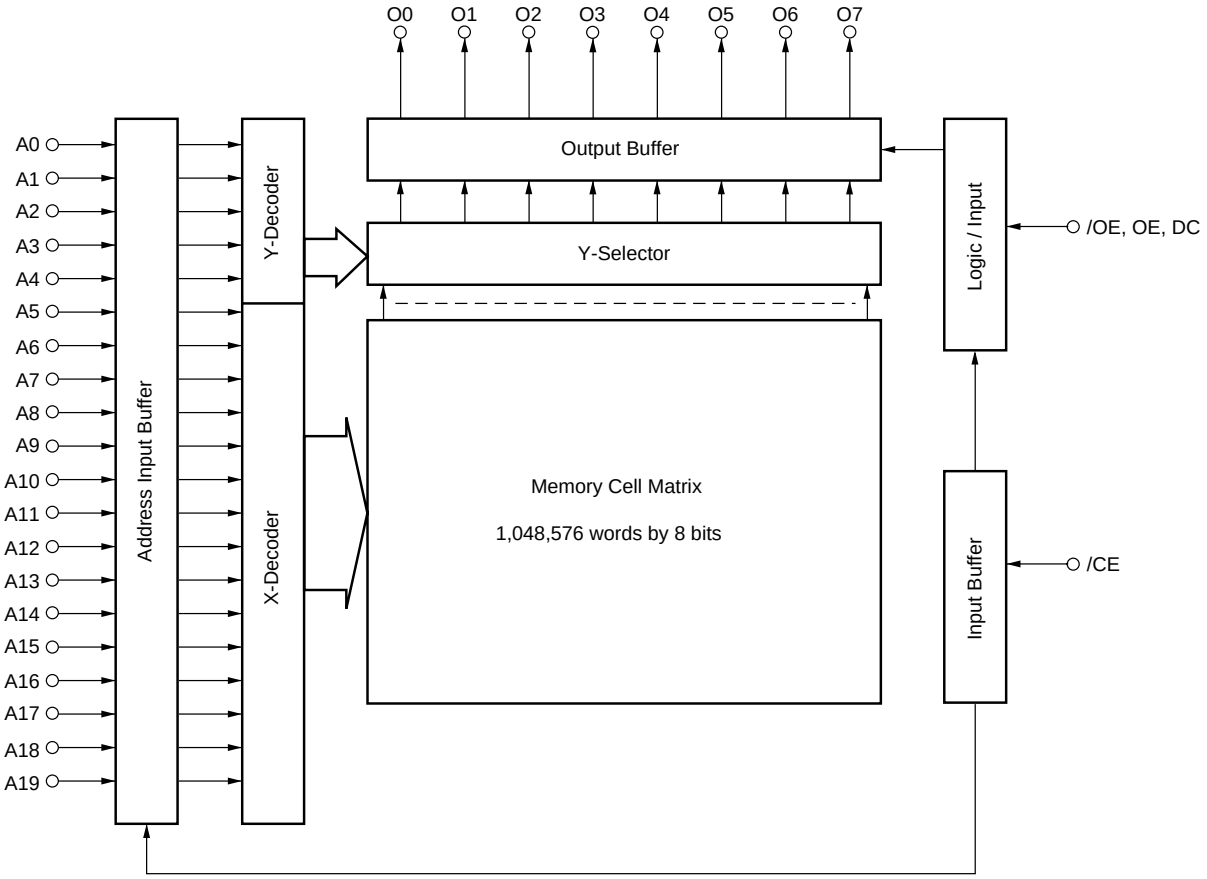


A0 - A19	:	Address inputs
O0 - O7	:	Data Outputs
/CE	:	Chip Enable
/OE, OE	:	Output Enable
VCC	:	Supply Voltage
GND	:	Ground
DC	:	Don’t Care

Input / Output Pin Functions

Pin name	Input / Output	Function
A0 to A19 (Address input)	Input	Address bus.
O0 to O7 (Data output)	Output	Output data bus.
/CE (Chip Enable)	Input	Chip activating signal. When the OE is active, output states are following. **High level** : High impedance **Low level** : Data out
/OE, OE, DC (Output Enable)	Input	Output enable signal. The active level of OE is mask option. The active level of OE can be selected from high active, low active and Don't care at order.
V_{CC}	–	Supply voltage
GND	–	Ground

Block Diagram



Mask Option

The active levels of output enable pin (/OE, OE, DC) are mask programmable and optional, and can be selected from among "0" "1" "×" shown in the table below.

Option	/OE, OE, DC	OE active level
0	/OE	L
1	OE	H
×	DC	Don't Care

Operation modes for each option are shown in the tables below.

Operation mode (Option : 0)

/CE	/OE	Mode	Output state
L	L	Active	Data out
	H		High impedance
H	H or L	Standby	High impedance

Operation mode (Option : 1)

/CE	OE	Mode	Output state
L	L	Active	High impedance
	H		Data out
H	H or L	Standby	High impedance

Operation mode (Option : ×)

/CE	DC	Mode	Output state
L	H or L	Active	Data out
H	H or L	Standby	High impedance

Remark L : Low level input
H : High level input

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		–0.3 to +7.0	V
Input voltage	V_I		–0.3 to V_{CC} + 0.3	V
Output voltage	V_O		–0.3 to V_{CC} + 0.3	V
Operating ambient temperature	T_A		–10 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Capacitance (T_A = 25 °C)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz			15	pF
Output capacitance	C_O				15	pF

DC Characteristics (T_A = –10 to +70 °C, V_{CC} = 5.0 V ± 0.5 V)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH}		2.2		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		–0.3		+0.8	V
High level output voltage	V_{OH1}	I_{OH} = –400 μA	2.4			V
	V_{OH2}	I_{OH} = –100 μA	V_{CC} – 0.5			
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V
Input leakage current	I_{LI}	V_I = 0 V to V_{CC}	–10		+10	μA
Output leakage current	I_{LO}	V_O = 0 V to V_{CC}, Chip deselected	–10		+10	μA
Power supply current	I_{CC1}	/CE = V_{IL} (Active mode), I_O = 0 mA			50	mA
Standby current	I_{CC2}	/CE = V_{IH} (Standby mode)			1.5	mA
	I_{CC3}	/CE = V_{CC} – 0.2 V (Standby mode)			100	μA

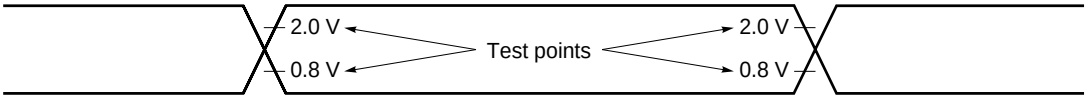
AC Characteristics (T_A = –10 to +70 °C, V_{CC} = 5.0 V ± 0.5 V)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Address access time	t_{ACC}				120	ns
Chip enable access time	t_{CE}				120	ns
Output enable access time	t_{OE}				60	ns
Output hold time	t_{OH}		0			ns
Output disable time	t_{DF}		0		30	ns

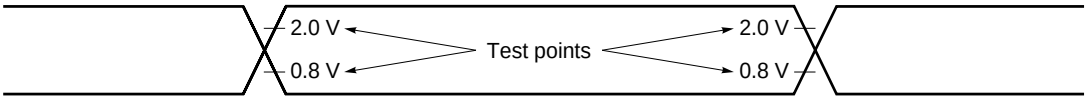
Remark t_{DF} is the time from inactivation of /CE or /OE, OE to high-impedance state output.

★ **AC Test Conditions**

Input Waveform (Rise / Fall Time ≤ 5 ns)



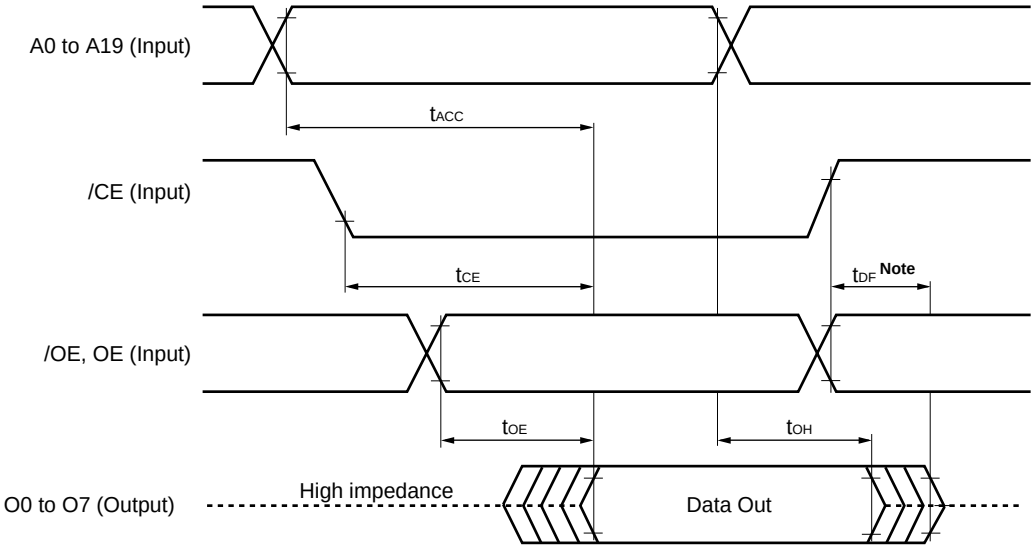
Output Waveform



Output Load

1 TTL + 100 pF

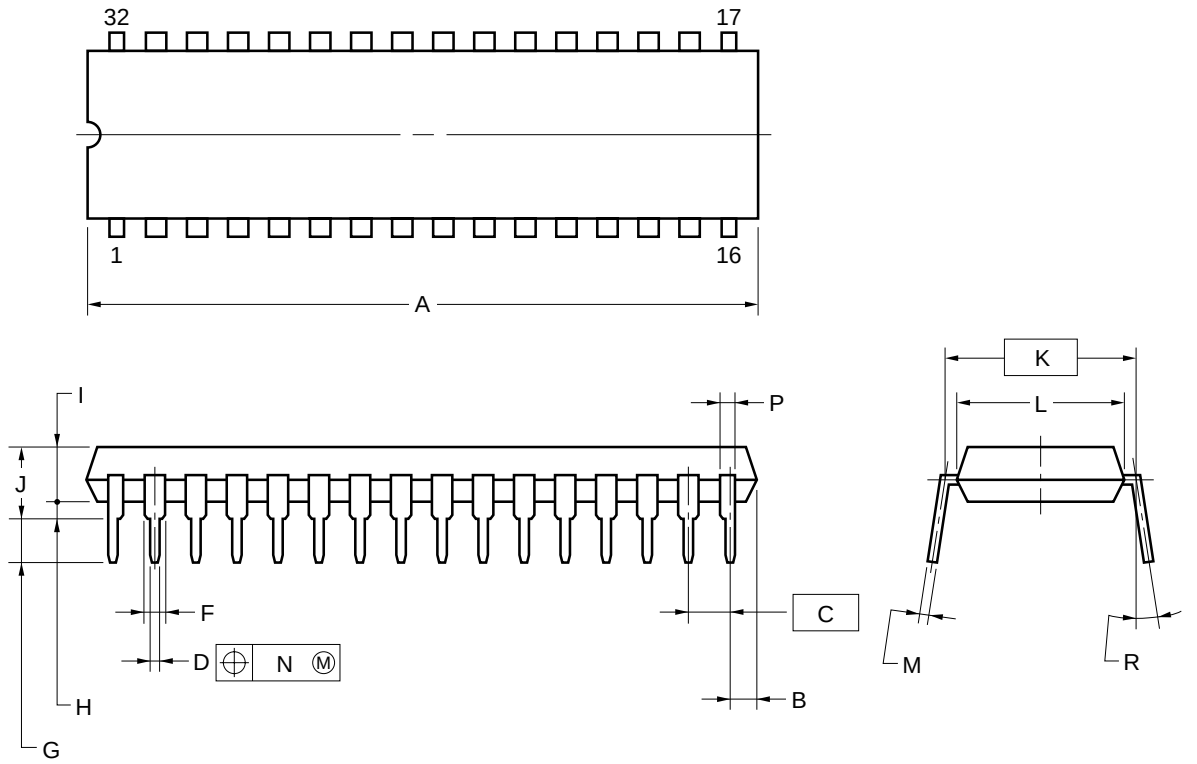
Read Cycle Timing Chart



Note t_{DF} is the time from inactivation of /CE or /OE, OE.

Package Drawings

32PIN PLASTIC DIP (600 mil)



NOTES

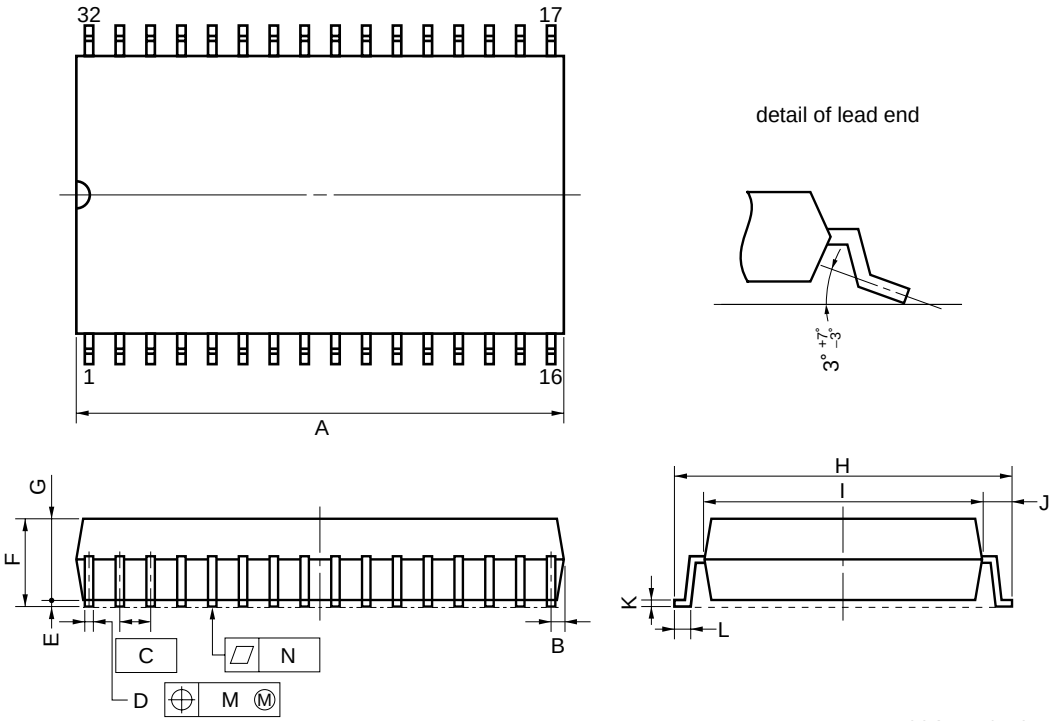
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	40.64 MAX.	1.600 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	1.1 MIN.	0.043 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.
R	0~15°	0~15°

P32C-100-600A-1

32 PIN PLASTIC SOP (525 mil)



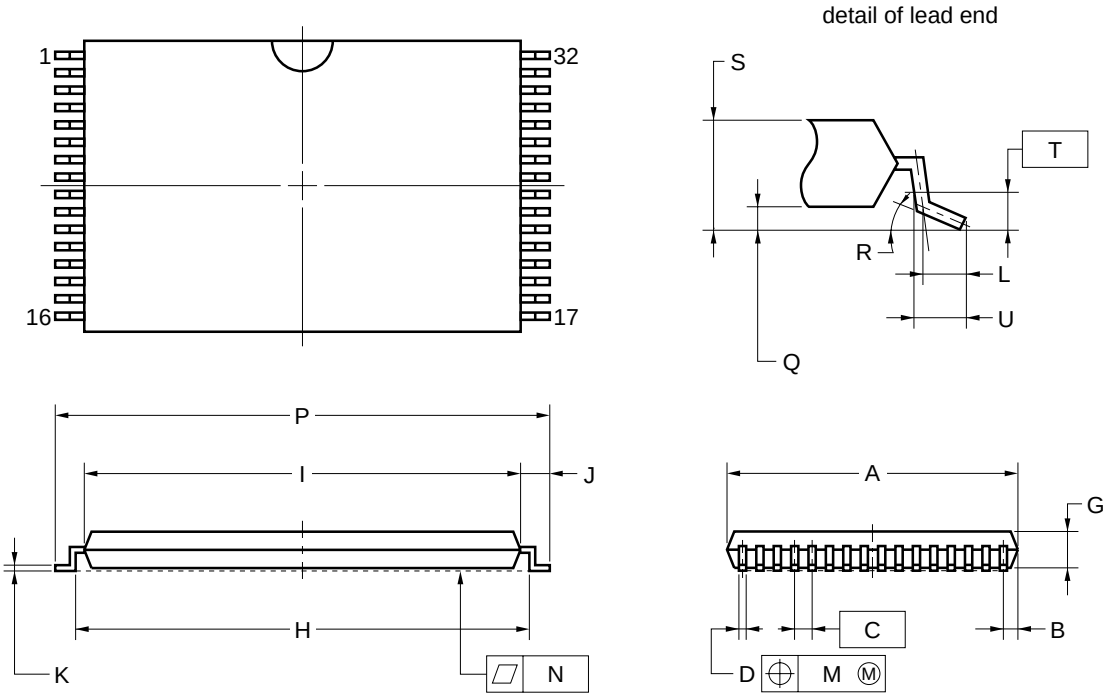
P32GW-50-525A

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	20.61 MAX.	0.812 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.15±0.05	0.006
F	2.95 MAX.	0.117 MAX.
G	2.7	0.106
H	14.1±0.3	0.555±0.012
I	11.3	0.445
J	1.4±0.2	0.055±0.008
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005
N	0.10	0.004

32PIN PLASTIC TSOP (I) (8x13.4)



NOTE

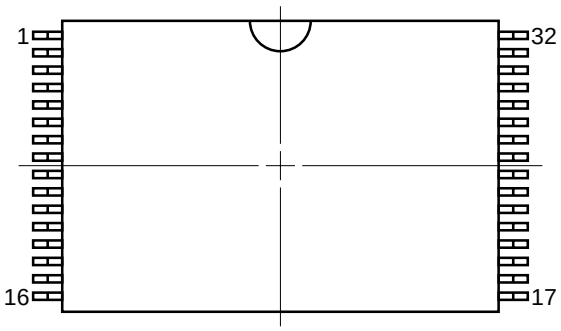
(1) Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

(2) "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX. <0.331 inch MAX.>)

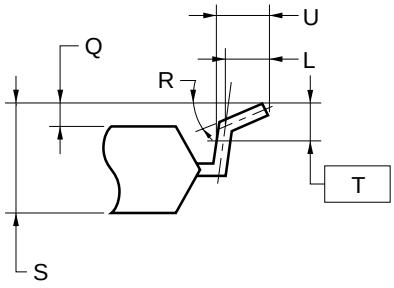
ITEM	MILLIMETERS	INCHES
A	8.0±0.1	0.315±0.004
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.22 ± 0.05	$0.009^{+0.002}_{-0.003}$
G	1.0 ± 0.05	$0.039^{+0.003}_{-0.009}$
H	12.4±0.2	0.488±0.008
I	11.8 ± 0.1	$0.465^{+0.004}_{-0.005}$
J	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5	0.020
M	0.08	0.003
N	0.08	0.003
P	13.4 ± 0.2	$0.528^{+0.008}_{-0.009}$
Q	0.1 ± 0.05	0.004±0.002
R	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
S	1.2 MAX.	0.048 MAX.
T	0.25	0.010
U	0.6 ± 0.15	$0.024^{+0.006}_{-0.007}$

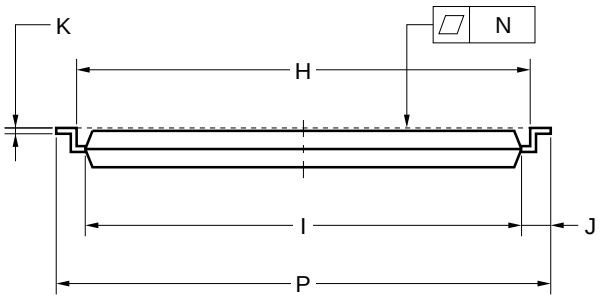
P32GU-50-9JH-1

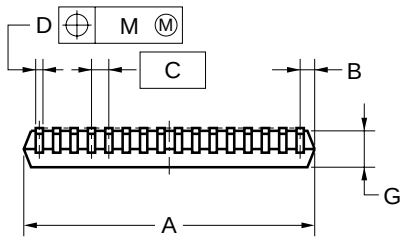
32PIN PLASTIC TSOP (I) (8x13.4)



detail of lead end







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G	1.0±0.05	$0.039^{+0.003}_{-0.009}$
H	12.4±0.2	0.488±0.008
I	11.8±0.1	$0.465^{+0.004}_{-0.005}$
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5	0.020
M	0.08	0.003
N	0.08	0.003
P	13.4±0.2	$0.528^{+0.008}_{-0.009}$
Q	0.1±0.05	0.004±0.002
R	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
S	1.2 MAX.	0.048 MAX.
T	0.25	0.010
U	0.6±0.15	$0.024^{+0.006}_{-0.007}$

P32GU-50-9KH-1

Recommended Soldering Conditions

The following conditions (see table below) must be met when soldering the μPD23C8001EJ.

For more details, refer to our document "**SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL**" **(C10535E)**.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Type of Surface Mount Device

μPD23C8001EJGW : 32-pin plastic SOP (525 mil)

μPD23C8001EJGU-9JH : 32-pin plastic TSOP (I) (8 × 13.4 mm) (Normal bent)

μPD23C8001EJGU-9KH : 32-pin plastic TSOP (I) (8 × 13.4 mm) (Reverse bent)

Please consult with our sales offices.

Type of Through Hole Mount Device

μPD23C8001EJCZ : 32-pin plastic DIP (600 mil)

Soldering process	Soldering conditions
Wave soldering (Only to leads)	Solder temperature : 260 °C or below, Flow time : 10 seconds or below
Partial heating method	Lead temperature : 300 °C or below, Time : 3 seconds or below (Per one lead)

Caution Do not jet molten solder on the surface of package.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

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