STK10C68
CMOS nvSRAM
High Performance
8K x 8 Nonvolatile Static RAM

SIMTEK

FEATURES

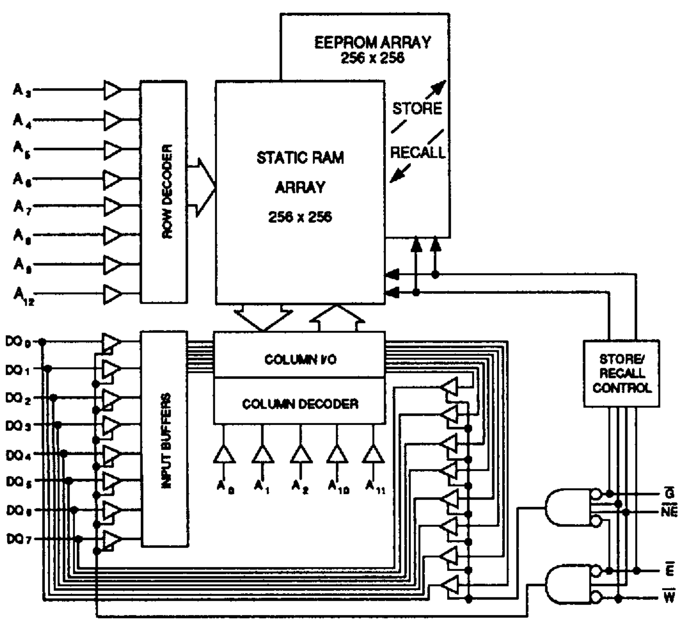
- **25, 30, 35 and 45ns Access Times**
- **12, 15, 20 and 25ns Output Enable Access**
- **Unlimited Read and Write to SRAM**
- **Hardware *STORE* Initiation**
- **Automatic *STORE* Timing**
- **100,000 *STORE* cycles to EEPROM**
- **10 year data retention in EEPROM**
- **Automatic *RECALL* on Power Up**
- **Hardware *RECALL* Initiation**
- **Unlimited *RECALL* cycles from EEPROM**
- **Single 5V±10% Operation**
- **Commercial and Industrial Temperatures**
- **Available in multiple standard packages**

DESCRIPTION

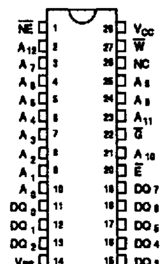
The Simtek STK10C68 is a fast static RAM (25, 30, 35, and 45ns), with a nonvolatile electrically-erasable PROM (EEPROM) element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in EEPROM. Data may easily be transferred from the SRAM to the EEPROM (*STORE*), or from the EEPROM to the SRAM (*RECALL*) using the $\overline{NE}$ pin. It combines the high performance and ease of use of a fast SRAM with nonvolatile data integrity.

The STK10C68 features industry standard pinout for nonvolatile RAMs in a 28-pin 300 mil plastic or ceramic DIP, and a 28-pin SOIC package. MIL-STD-883 and Standard Military Drawing (SMD #5962-93056) devices are also available.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATIONS



28 - 300 PDIP
28 - 300 CDIP
28 - 350 SOIC

PIN NAMES

A_0 - A_{12}	Address Inputs
$\overline{W}$	Write Enable
DQ_0 - DQ_7	Data In/Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{NE}$	Nonvolatile Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS[a]

Voltage on typical input relative to V_{SS} . . . . –0.6V to 7.0V
Voltage on DQ_{0-7} and $\overline{G}$ . . . . –0.5V to (V_{CC}+0.5V)
Temperature under bias . . . . –55°C to 125°C
Storage temperature . . . . –65°C to 150°C
Power dissipation 1W
DC output current 15mA
(One output at a time, one second duration)

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC_1}[b]	Average V_{CC} Current		90		95	mA	t_{AVAV} = 25ns
			85		90	mA	t_{AVAV} = 30ns
			80		85	mA	t_{AVAV} = 35ns
			75		80	mA	t_{AVAV} = 45ns
I_{CC_2}[d]	Average V_{CC} Current during *STORE* cycle		50		50	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ all others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{SB_1}[c]	Average V_{CC} Current (Standby, Cycling TTL Input Levels)		30		34	mA	t_{AVAV} = 25ns
			27		30	mA	t_{AVAV} = 30ns
			23		27	mA	t_{AVAV} = 35ns
			20		23	mA	t_{AVAV} = 45ns
							$\overline{E} \geq V_{IH}$; all others cycling
I_{SB_2}[c]	Average V_{CC} Current (Standby, Stable CMOS Input Levels)		1		1	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ all others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current (Any Input)		±1		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current		±5		±5	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
V_{IH}	Input Logic "1" Voltage	2.2	V_{CC}+.5	2.2	V_{CC}+.5	V	All Inputs
V_{IL}	Input Logic "0" Voltage	V_{SS}–.5	0.8	V_{SS}–.5	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	I_{OUT} = –4mA
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	I_{OUT} = 8mA
T_A	Operating Temperature	0	70	–40	85	°C	

Note b: I_{CC_1} is dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
Note c: Bringing $\overline{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.
Note d: I_{CC_2} is the average current required for the duration of the store cycle (t_{STORE}) after the sequence (t_{WC}) that initiates the cycle.

AC TEST CONDITIONS

Input Pulse Levels . . . . V_{SS} to 3V
Input Rise and Fall Times . . . . ≤ 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . See Figure 1

CAPACITANCE[e] (T_A=25°C, f=1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note e: These parameters are guaranteed but not tested.

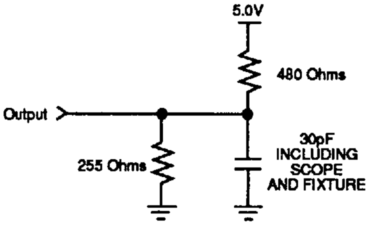


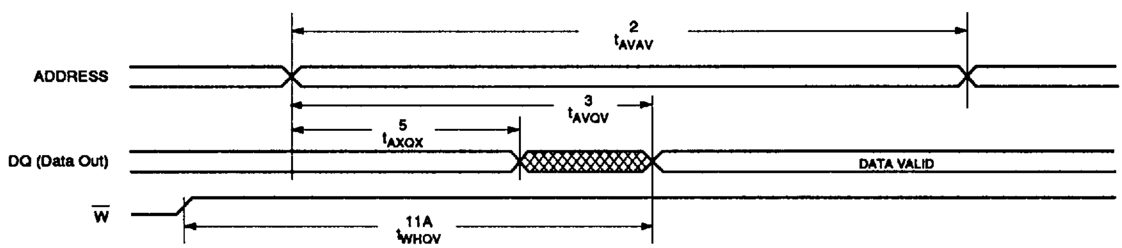
Figure 1: AC Output Loading

READ CYCLES #1 & #2

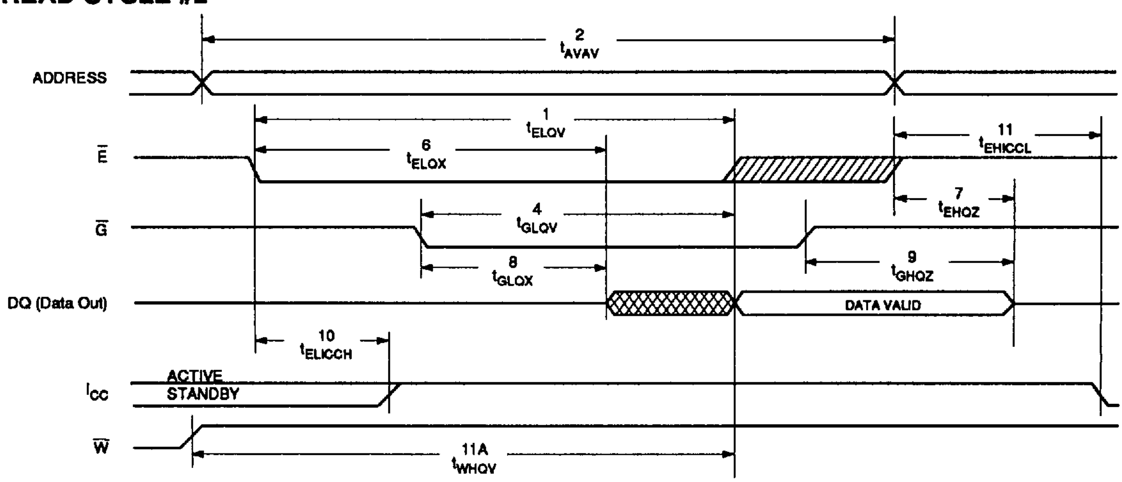
NO.	SYMBOLS #1, #2	SYMBOLS Alt.	PARAMETER	STK10C68-25 MIN	STK10C68-25 MAX	STK10C68-30 MIN	STK10C68-30 MAX	STK10C68-35 MIN	STK10C68-35 MAX	STK10C68-45 MIN	STK10C68-45 MAX	UNITS
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		30		35		45	ns
2	$t_{AVAV}{}^{g}$	t_{RC}	Read Cycle Time	25		30		35		45		ns
3	$t_{AVQV}{}^{h}$	t_{AA}	Address Access Time		25		30		35		45	ns
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		12		15		20		25	ns
5	t_{AXQX}	t_{OH}	Output Hold After Address Change	5		5		5		5		ns
6	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		5		ns
7	$t_{EHQZ}{}^{i}$	t_{HZ}	Chip Disable to Output Inactive		13		15		17		20	ns
8	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		0		ns
9	$t_{GHQZ}{}^{i}$	t_{OHZ}	Output Disable to Output Inactive		13		15		17		20	ns
10	$t_{ELICCH}{}^{e}$	t_{PA}	Chip Enable to Power Active	0		0		0		0		ns
11	$t_{EHICCL}{}^{c,e}$	t_{PS}	Chip Disable to Power Standby		25		30		35		45	ns
11A	t_{WHQV}	t_{WR}	Write Recovery Time		30		35		45		55	ns

Note c: Bringing $\overline{E}$ high will not produce standby currents until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.
Note e: Parameter guaranteed but not tested.
Note f: $\overline{NE}$ must be high during entire cycle.
Note g: For READ CYCLE #1 and #2, $\overline{W}$ and $\overline{NE}$ must be high for entire cycle.
Note h: Device is continuously selected with $\overline{E}$ low and $\overline{G}$ low.
Note i: Measured ± 200mV from steady state output voltage.

READ CYCLE #1 f,g,h



READ CYCLE #2 f,g



WRITE CYCLES #1 & #2; $\overline{G}$ high

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS #1	SYMBOLS #2	SYMBOLS Alt.	PARAMETER	STK10C68-25 MIN	STK10C68-25 MAX	STK10C68-30 MIN	STK10C68-30 MAX	STK10C68-35 MIN	STK10C68-35 MAX	STK10C68-45 MIN	STK10C68-45 MAX	UNITS
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	25		30		35		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		30		35		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		25		30		35		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	12		15		18		20		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		25		30		35		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		0		ns

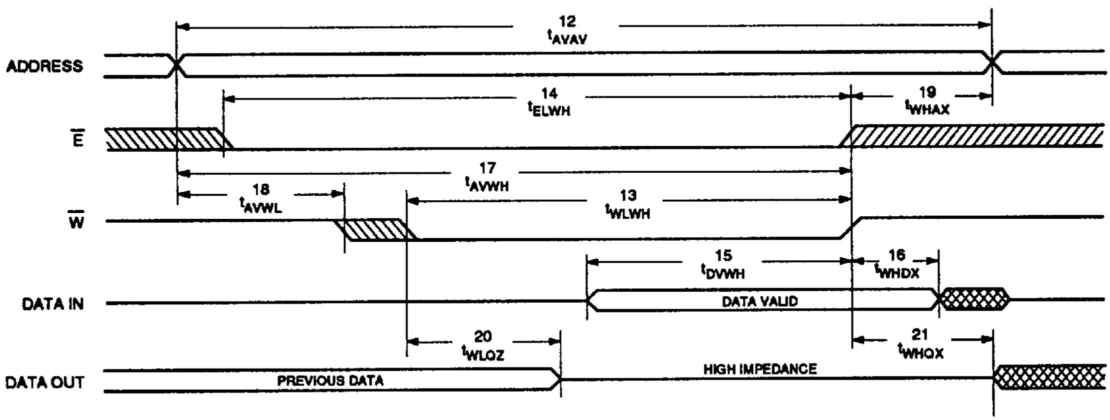
WRITE CYCLES #1 & #2; $\overline{G}$ low

(V_{CC} = 5.0V ± 10%)

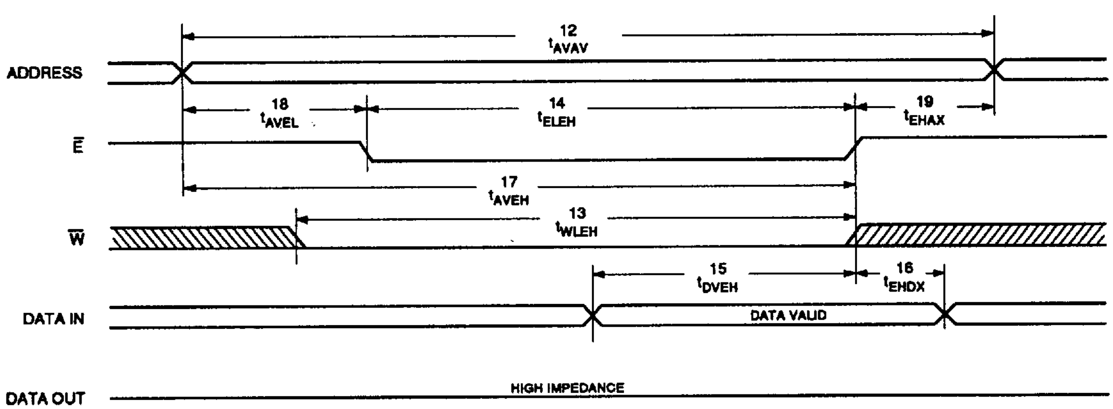
NO.	SYMBOLS #1	SYMBOLS #2	SYMBOLS Alt.	PARAMETER	STK10C68-25 MIN	STK10C68-25 MAX	STK10C68-30 MIN	STK10C68-30 MAX	STK10C68-35 MIN	STK10C68-35 MAX	STK10C68-45 MIN	STK10C68-45 MAX	UNITS
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	45		45		45		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	35		35		35		35		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	35		35		35		35		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	30		30		30		30		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	35		35		35		35		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		0		ns
20	$t_{WLQZ}{}^{l,m}$		t_{WZ}	Write Enable to Output Disable		35		35		35		35	ns
21	t_{WHQX}		t_{OW}	Output Active After End of Write	5		5		5		5		ns

Note f: $\overline{NE}$ must be ≥ V_{IH} during entire cycle.
Note l: Measured ± 200mV from steady state output voltage.
Note k: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note m: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.

WRITE CYCLE #1: $\overline{W}$ CONTROLLED[f,k]



WRITE CYCLE #2: $\overline{E}$ CONTROLLED[f,k]



NONVOLATILE MEMORY OPERATION

MODE SELECTION

$\overline{E}$	$\overline{W}$	$\overline{G}$	$\overline{NE}$	MODE	POWER
H	X	X	X	Not Selected	Standby
L	H	L	H	Read RAM	Active
L	L	X	H	Write RAM	Active
L	H	L	L	Nonvolatile *RECALL*[n]	Active
L	L	H	L	Nonvolatile *STORE*	I_{CC_2}
L	L	L	L	No operation	Active
L	H	H	X		

STORE CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS			PARAMETER	MIN	MAX	UNITS
	#1	#2	Alt.				
22	t_{WLOX}[p]	t_{ELOXS}	t_{STORE}	*STORE* Cycle Time		10	ms
23	t_{WLNH}[q]	t_{ELNHS}	t_{WC}	*STORE* Initiation Cycle Time	25		ns
24	t_{GHNL}			Output Disable Set-up to $\overline{NE}$ Fall	5		ns
25		t_{GHEL}		Output Disable Set-up to $\overline{E}$ Fall	5		ns
26	t_{NLWL}	t_{NLEL}		$\overline{NE}$ Set-up	5		ns
27	t_{ELWL}			Chip Enable Set-up	5		ns
28		t_{WLEL}		Write Enable Set-up	5		ns

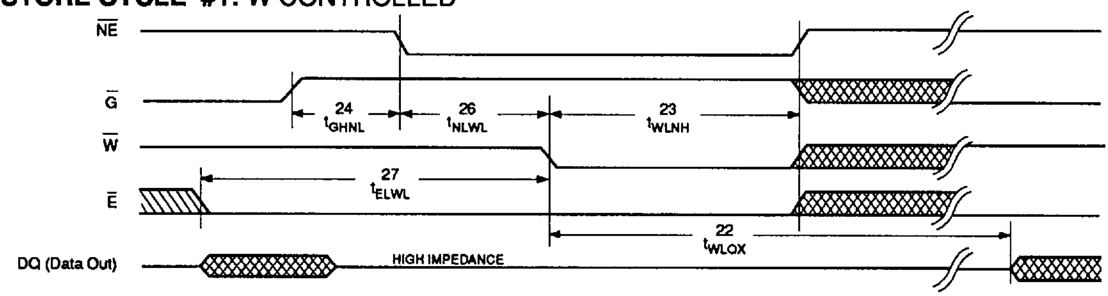
Note n: An automatic *RECALL* also takes place at power up, starting when V_{CC} exceeds 4.0V, and taking $t_{RESTORE}$ from the time at which V_{CC} exceeds 4.5V. V_{CC} must not drop below 4.0V once it has been exceeded for the *RECALL* to function properly.

Note o: If $\overline{E}$ is low for any period of time in which $\overline{W}$ is high while $\overline{G}$ and $\overline{NE}$ are low, then a *RECALL* cycle may be initiated.

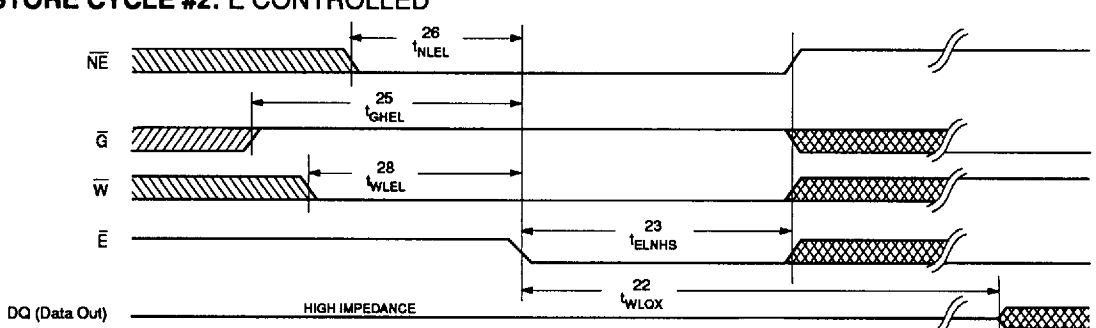
Note p: Measured with $\overline{W}$ and $\overline{NE}$ both returned high, and $\overline{G}$ returned low. Note that *STORE* cycles are inhibited/aborted by V_{CC} < 4.0V (*STORE* inhibit).

Note q: Once t_{WC} has been satisfied by $\overline{NE}$, $\overline{G}$, $\overline{W}$ and $\overline{E}$, the *STORE* cycle is completed automatically. Any of $\overline{NE}$, $\overline{G}$, $\overline{W}$ or $\overline{E}$ may be used to terminate the *STORE* initiation cycle.

STORE CYCLE #1: $\overline{W}$ CONTROLLED[o]



STORE CYCLE #2: $\overline{E}$ CONTROLLED[o]



8274887 0000830 054

RECALL CYCLES #1, #2 & #3

(V_{CC} = 5.0V ± 10%)

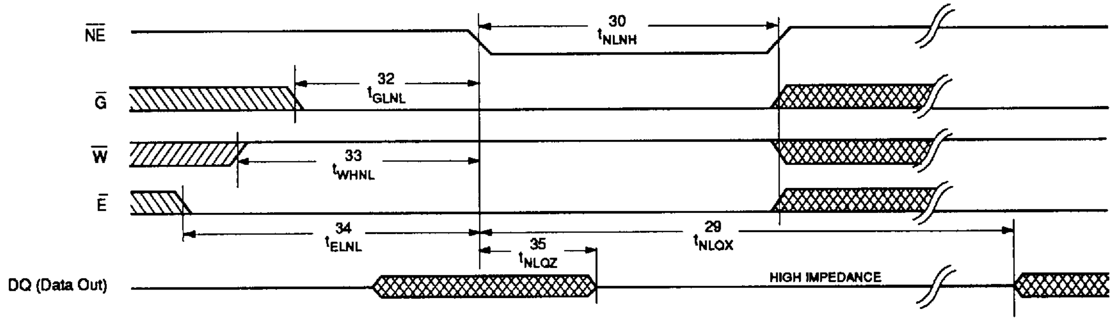
NO.	SYMBOLS #1	SYMBOLS #2	SYMBOLS #3	PARAMETER	MIN	MAX	UNITS
29	$t_{NLQX}{}^{r}$	t_{ELQXR}	t_{GLQXR}	*RECALL* Cycle Time		20	µs
30	$t_{NLNH}{}^{s}$	t_{ELNHR}	t_{GLNH}	*RECALL* Initiation Cycle Time	25		ns
31		t_{NLEL}	t_{NLGL}	$\overline{NE}$ Set-up	5		ns
32	t_{GLNL}	t_{GLEL}		Output Enable Set-up	5		ns
33	t_{WHNL}	t_{WHEL}	t_{WHGL}	Write Enable Set-up	5		ns
34	t_{ELNL}	t_{GLEL}		Chip Enable Set-up	5		ns
35	t_{NLQZ}			$\overline{NE}$ Fall to Outputs Inactive		25	ns
36	$t_{RESTORE}$			Power-up Recall Duration		550	µs

Note r: Measured with $\overline{W}$ and $\overline{NE}$ both high, and $\overline{G}$ and $\overline{E}$ low.

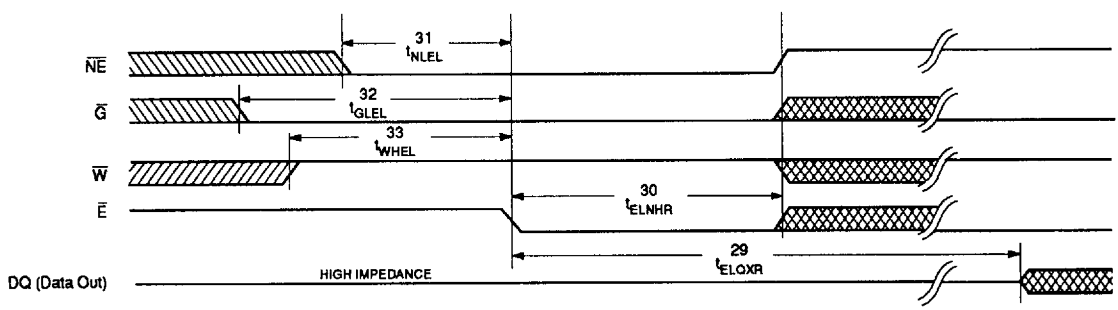
Note s: Once t_{NLNH} has been satisfied by $\overline{NE}$, $\overline{G}$, $\overline{W}$ and $\overline{E}$, the *RECALL* cycle is completed automatically. Any of $\overline{NE}$, $\overline{G}$ or $\overline{E}$ may be used to terminate the *RECALL* initiation cycle.

Note t: If $\overline{W}$ is low at any point in which both $\overline{E}$ and $\overline{NE}$ are low and $\overline{G}$ is high, then a *STORE* cycle will be initiated instead of a *RECALL*.

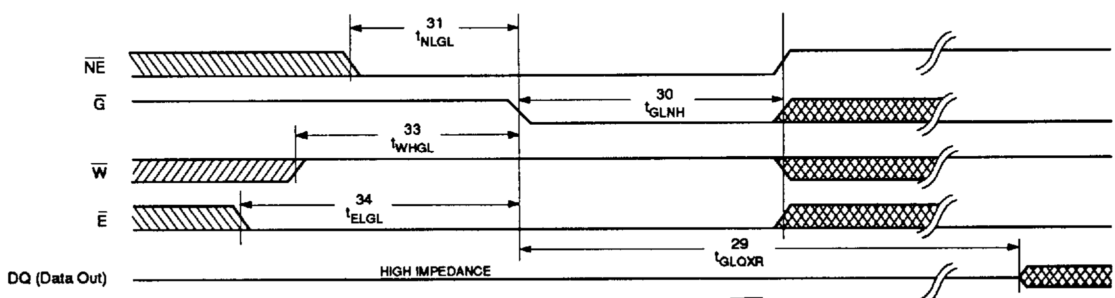
RECALL CYCLE #1: $\overline{NE}$ CONTROLLED[o]



RECALL CYCLE #2: $\overline{E}$ CONTROLLED[o]



RECALL CYCLE #3: $\overline{G}$ CONTROLLED[o,t]



DEVICE OPERATION

The STK10C68 has two modes of operation: SRAM mode and nonvolatile mode, determined by the state of the $\overline{NE}$ pin. When in SRAM mode, the memory operates as a standard fast static RAM. While in nonvolatile mode, data is transferred in parallel from SRAM to EEPROM or from EEPROM to SRAM.

SRAM READ

The STK10C68 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are LOW and $\overline{NE}$ and $\overline{W}$ are HIGH. The address specified on pins A_{0-12} determines which of the 8192 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ CYCLE #1). If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV} whichever is later (READ CYCLE #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought HIGH or $\overline{W}$ or $\overline{NE}$ is brought LOW.

NOISE CONSIDERATIONS

The STK10C68 is a high speed memory and therefore must have a high frequency bypass capacitor of approximately 0.1µF connected between DUT V_{CC} and V_{SS} using leads and traces that are as short as possible. As with all high speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM WRITE

A write cycle is performed whenever $\overline{E}$ and $\overline{W}$ are LOW and $\overline{NE}$ is HIGH. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ go HIGH at the end of the cycle. The data on pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept HIGH during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\overline{G}$ is left LOW, internal circuitry will turn off the output buffers t_{WLQZ} after W goes LOW.

Keeping $\overline{G}$ high during write cycles also enables use of the faster write specifications.

NONVOLATILE STORE

A *STORE* cycle is performed when $\overline{NE}$, $\overline{E}$ and $\overline{W}$ are LOW and $\overline{G}$ is HIGH. While any sequence to achieve this state will initiate a *STORE*, only W initiation (*STORE* CYCLE #1) and $\overline{E}$ initiation (*STORE* CYCLE #2) are practical without risking an unintentional SRAM WRITE that would disturb SRAM data. During a *STORE* cycle, previous nonvolatile data is erased and the SRAM contents are then programmed into nonvolatile elements. Once a *STORE* cycle is initiated, further input and output is disabled and the DQ_{0-7} pins are tri-stated until the cycle is completed.

If $\overline{E}$ and $\overline{G}$ are LOW and $\overline{W}$ and $\overline{NE}$ are HIGH at the end of the cycle, a READ will be performed and the outputs will go active, signaling the end of the *STORE*.

HARDWARE PROTECT

The STK10C68 offers two levels of protection to suppress inadvertent *STORE* cycles. If the control signals ($\overline{E}$, $\overline{G}$, $\overline{W}$, and $\overline{NE}$) remain in the *STORE* condition at the end of a *STORE* cycle, a second *STORE* cycle will *not* be started. The *STORE* (or *RECALL*) will be initiated only after a transition on any one of these signals to the required state. In addition to multi-trigger protection, the STK10C68 offers hardware protection through V_{CC} Sense. A *STORE* cycle will not be initiated, and one in progress will discontinue if V_{CC} goes below 4.0V. 4.0V is a typical, characterized value. The datasheet specifications are guaranteed only for V_{CC} = 5.0 ±10%.

NONVOLATILE RECALL

A *RECALL* cycle is performed when $\overline{E}$, $\overline{G}$, and $\overline{NE}$ are LOW and $\overline{W}$ is HIGH. Like the *STORE* cycle, *RECALL* is initiated when the last of the four clock signals goes to the *RECALL* state. Once initiated, the *RECALL* cycle will take t_{NLQX} to complete, during which all inputs are ignored. When the *RECALL* completes, any READ or WRITE state on the input pins will take effect.

Internally, *RECALL* is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. The *RECALL* operation in no way alters the data in the nonvolatile cells. The nonvolatile data can be recalled an unlimited number of times.

Like the *STORE* cycle, a transition must occur on some control pin to cause a recall, preventing inadvertent multi-triggering. On power-up, once V_{CC} exceeds the V_{CC} sense voltage of 4.0V, a *RECALL* cycle is automatically initiated. The voltage on the V_{CC} pin must not drop below 4.0V once it has risen above it in order for the *RECALL* to operate properly. Due to this automatic *RECALL*, SRAM operation cannot commence until $t_{RESTORE}$ after V_{CC} exceeds 4.0V. 4.0V is a typical, characterized value.

If the STK10C68 is in a WRITE state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected between $\overline{W}$ and system V_{CC}.

ORDERING INFORMATION

STK10C68 - P 30 I

Temperature Range (I)
- blank = Commercial (0 to 70 degrees C)
- I = Industrial (–40 to 85 degrees C)

Access Time (30)
- 25 = 25ns
- 30 = 30ns
- 35 = 35ns
- 45 = 45ns

Package (P)
- P = Plastic 28 pin 300 mil DIP
- S = Plastic 28 pin 350 mil SOIC
- C = Ceramic 28 pin 300 mil DIP