CY54/74FCT2652T
8-BIT REGISTERED TRANSCEIVER

FEATURES

- **Function and Drive Compatible with the FCT and F Logic**
- **FCT-C speed at 5.4ns max. (Com'l) FCT-A speed at 6.3ns max. (Com'l)**
- **R25Ω output series resistors to reduce transmission line reflection noise**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **12 mA Sink Current (Com'l), 12 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**
- **Independent Register for A and B Buses**
- **Multiplexed Real-Time and Stored Data Transfer**
- **Bidirectional Bus Transceiver and Registers**

DESCRIPTION

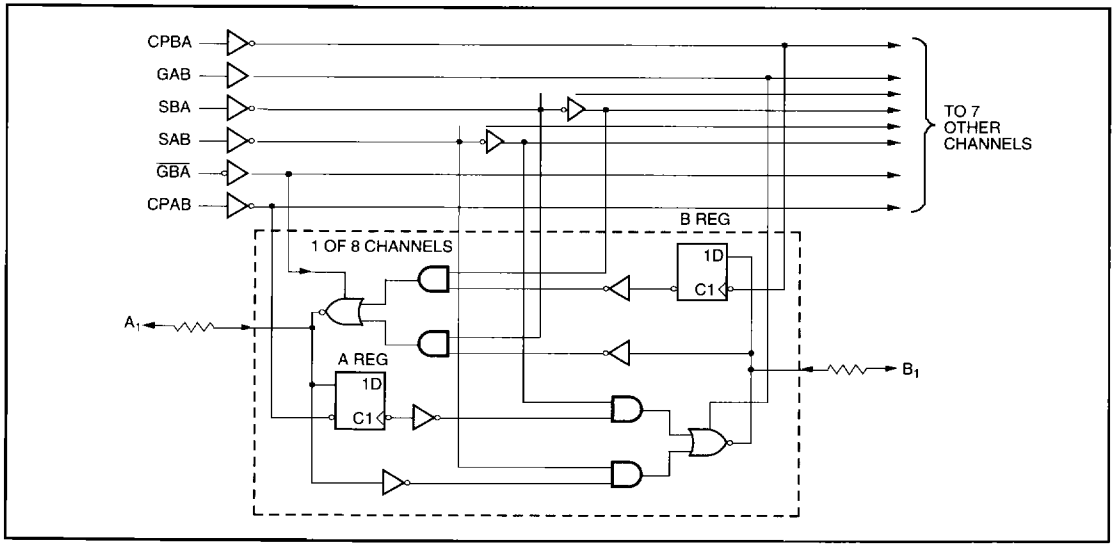
The 'FCT2652T consists of bus tranciever circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal storage registers. GAB and $\overline{GBA}$ control pins are provided to control the transceiver functions. SAB and SBA control pins are provided to select either real-time or stored data transfer.

On-chip termination resistors are added to the outputs to reduce system noise caused by reflections. The 'FCT2652T can replace the 'FCT652T to reduce noise in an existing design.

The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during transition between stored and real-time data. A low input level selects real-time data and a high selects stored data.

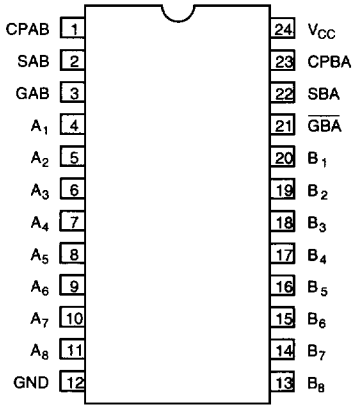
Data on the A or B data bus, or both, can be stored in internal D flip-flops by low-to-high transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins. By simultaneously enabling GAB and $\overline{GBA}$ when SAB and SBA are in real-time transfer mode, it is possible to store data without using internal D-type flip-flops. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

FUNCTIONAL BLOCK DIAGRAM



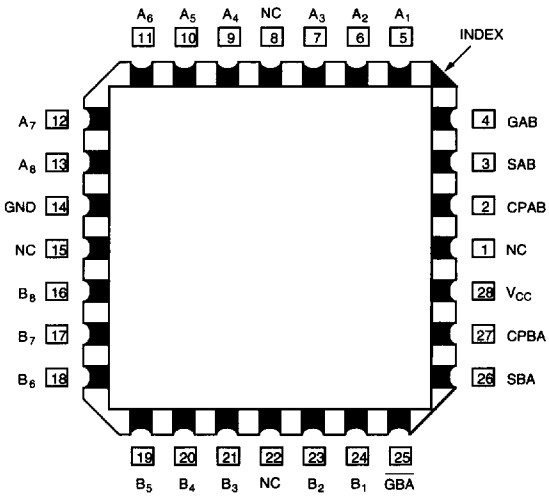
PIN CONFIGURATIONS

Top View



DIP (D14, P13/13A) SOIC (S13), QSOP(Q13)

Top View



LCC (L64)

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

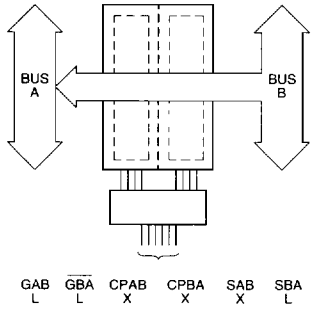
Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

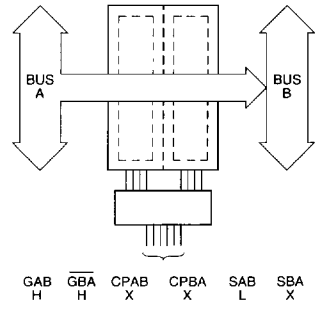
Symbol	Parameter		Min	Typ[3]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis[3]			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.55	V	MIN	I_{OL} = 12mA
		Commercial		0.3	0.55	V	MIN	I_{OL} = 12mA
R_{OUT}	Output Resistance	Military		25		Ω	MIN	I_{OL} = 12mA
		Commercial	20	25	40	Ω	MIN	I_{OL} = 12mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current (Except I/O Pins)				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current (Except I/O Pins)				–5	µA	MAX	V_{IN} = 0.5V
I_{IH}	Input HIGH Current (I/O Pins only)				15	µA	MAX	V_{OUT} = 2.7V
I_{IL}	Input LOW Current (I/O Pins only)				–15	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[4]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[5]			5	10	pF	MAX	All inputs
$C_{I/O}$	I/O Capacitance[5]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} > V_{CC} - 0.2V$

Notes:

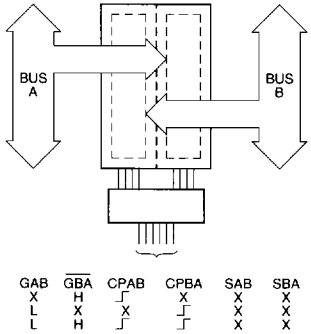
1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
3. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
4. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
5. This parameter is guaranteed but not tested.



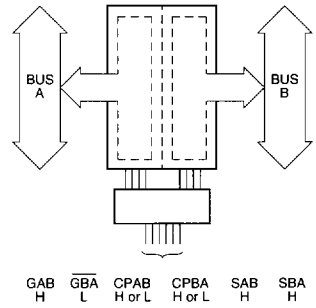
REAL-TIME TRANSFER BUS B TO BUS A



REAL-TIME TRANSFER BUS A TO BUS B



STORAGE FROM A AND/OR B



TRANSFER STORED DATA TO A AND/OR B

Note: Cannot transfer data to A bus and B bus simultaneously.

FUNCTION TABLES

Inputs						Data I/O		Operation or Function
GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA	A_1 thru A_8	B_1 thru B_8	'FCT2652T
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↓	↓	X	X			Store A and B Data
X	H	↓	H or L	X	X	Input	Unspecified[6]	Store A, Hold B
H	H	↓	↓	X[7]	X	Input	Output	Store A in both registers
L	X	H or L	↓	X	X	Unspecified[1]	Input	Hold A, Store B
L	L	↓	↓	X	X[7]	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

Notes:

6. The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
7. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered in order to load both registers.
   H = HIGH, L = LOW, X = Don't Care, ↓ LOW-to-HIGH Transition

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[8], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[9]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open GAB = GND, $\overline{GBA}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[11]	1.7	4.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, GAB = GND, $\overline{GBA}$ = GND, SAB = CPAB = GND, SBA = V_{CC}, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.2	6.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, GAB = GND, $\overline{GBA}$ = GND, SAB = CPAB = GND, SBA = V_{CC}, V_{IN} = 3.4V or V_{IN} = GND
		7.0	12.8[10]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 5MHz, GAB = $\overline{GBA}$ = GND, SAB = CPAB = GND, SBA = V_{CC}, $V_{IN} = 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		9.2	21.8[10]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 5MHz, GAB = $\overline{GBA}$ = GND, SAB = CPAB = GND, SBA = V_{CC}, V_{IN} = 3.4V or V_{IN} = GND

Notes:

8. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
11. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} \bullet D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_1 = Input Frequency
    N_1 = Number of Inputs at f_1
    All currents are in milliamps and all frequencies are in megahertz.

AC CHARACTERISTICS

Symbol	Parameter	'FCT2652T				'FCT2652AT				'FCT2652CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	2.0	11.0	2.0	9.0	2.0	7.7	2.0	6.3	1.5	6.0	1.5	5.4	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time Enable to Bus	2.0	15.0	2.0	14.0	2.0	10.5	2.0	9.8	1.5	8.9	1.5	7.8	ns	1, 5
t_{PHZ} t_{PLZ}	Output Disable Time Enable to Bus	2.0	11.0	2.0	9.0	2.0	7.7	2.0	6.3	1.5	7.7	1.5	6.3	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	2.0	10.0	2.0	9.0	2.0	7.0	2.0	6.3	1.5	6.3	1.5	5.7	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	2.0	12.0	2.0	11.0	2.0	8.4	2.0	7.7	1.5	7.0	1.5	6.2	ns	1, 7, 8

Notes:

* AC Characteristics guaranteed with C_L = 50pF as shown in Figure 1.

* See "Parameter Measurement Information" in the General Information Section.

AC OPERATING REQUIREMENTS

Symbol	Parameter	'FCT2652T				'FCT2652AT				'FCT2652CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW Bus to Clock	4.5	—	4.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns	1, 4
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW Bus to Clock	2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	1, 4
$t_w(H)$ $t_w(L)$	Clock Pulse Width, HIGH or LOW	6.0	—	6.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns	1, 5

Notes:

12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. With one data channel toggling, $t_w(L) = t_w(H) = 4.0$ns and $t_r = t_f = 1.0$ns.

*Refer to the 'Parameter Measurement Information' section of this book.

ORDERING INFORMATION