PARADIGM®

T-46-23-10

1 Megabit Static RAM 256K x 4-Bit

PDM41028S
PDM41028L

Features

- ☐ High speed access times
  Com'l: 20, 25, 35 and 45ns
  Mil : 20, 25, 35, 45, and 55ns
- ☐ Low power operation
  - PDM41028S
    Active: 400mW (typ.)
    Standby: 150 mW (typ.)
  - PDM41028L
    Active: 350mW (typ.)
    Standby: 100 mW (typ.)
- ☐ Single +5V (±10%) power supply
- ☐ TTL compatible inputs and outputs
- ☐ Military product MIL-STD-883, Rev. C
- ☐ Packages
  Sidebraze dip (400 mil) - TC,
  Plastic SOJ (300 mil) - TSO,
  Plastic SOJ (400 mil) - SO.

Description

The PDM41028 is a high performance CMOS static RAM organized as 262,144 x4 bits. This product is produced in Paradigm's proprietary CMOS technology which offers the designer the highest speed parts. Writing to this device is accomplished when the write enable ($\overline{WE}$) and the chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ are both LOW.

The PDM41028 operates from a single +5V power supply and all the inputs and outputs are fully TTL compatible. The PDM41028 comes in two versions, the standard power version PDM41028S and a low power version the PDM41028L. The two versions are functionally the same and only differ in their power consumption.

The Paradigm 41 (static ram) family of products are functionally equivalent to manufacturers products meeting JEDEC standards. These products are manufactured and quality controlled in the U.S.A.

The PDM41028 is available in a 28-pin 400 mil DIP. The PDM41028 is also available in a 28-pin 300 mil SOJ and a 28-pin 400 mil SOJ for surface mount applications.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Rev. C, making the PDM41028 ideally suited for military temperature applications.

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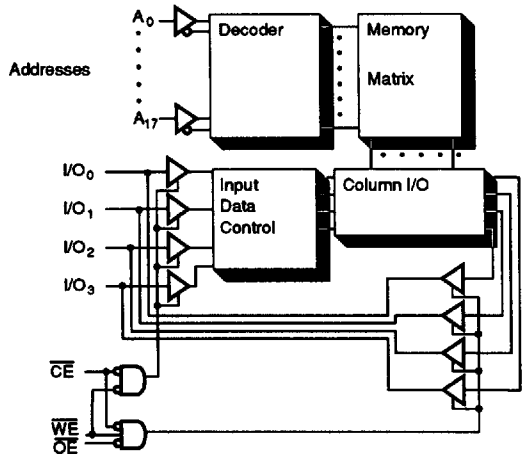
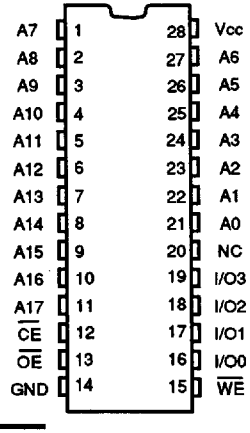
Functional Block Diagram



Pin Configuration

400 DIP
400 SOJ
300 SOJ



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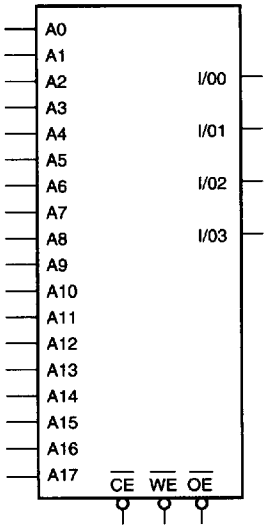
Logic Symbol



Recommended Operating Temperature and Supply Voltage

Grade	Ambient Temperature	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

Truth Table(1)

$\overline{OE}$	$\overline{WE}$	$\overline{CE}$	I/O	MODE
X	X	H	Hi-Z	Standby
L	H	L	D_{OUT}	Read
X	L	L	D_{IN}	Write
H	H	L	Hi-Z	Output Disable

NOTE:
1. H = V_{IH}, L = V_{IL}, X = DON'T CARE.

DC Electrical Characteristics V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions		PDM41028S Min.	PDM41028S Max.	PDM41028L Min.	PDM41028L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	—	10	—	5	µA
			Com'l	—	5	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max.	MIL.	—	10	—	5	µA
		$\overline{CE}$ = V_{IH}, V_{OUT} = GND to V_{CC}	Com'l	—	5	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	V
		I_{OL} = 10mA, V_{CC} = Min.		—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	2.4	—	V

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE:
1. V_{IL} (min) = -3.0V for pulse width less than 20ns.

DC Electrical Characteristics[1] (V_{CC} = 5.0V ± 10%, $V_{LC} \leq 0.2V$, $V_{HC} \geq V_{CC} - 0.2$)

Symbol	Parameter	Power	20, Com'l., Mil.	25, Com'l., Mil.	35, 45, 55 [4]ns Com'l., Mil.	Unit
I_{CC}	Dynamic Operating Current $\overline{CE} = V_{IL}$,	S	175	165	155	mA
	V_{CC} = Max., f = f_{MAX}[3] I_{OUT} = 0mA	L	175	165	155	mA
I_{SB}	Standby Power Supply Current (TTL Level)	S	60	60	60	mA
	$\overline{CE} \geq V_{IH}$, V_{CC} = Max., f = f_{MAX}[3]	L	50	50	50	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level)	S	10	10	10	mA
	$\overline{CE} \geq V_{HC}$, V_{CC} = Max., f = 0[3], $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	L	5	5	5	mA

NOTES:
1. All values are maximum guaranteed values.
2. Write cycle current specifications are included to aid in the design of extremely sensitive applications. It should be noted that in most systems the ratio of read cycles to write cycles is extremely high. When comparing these figures to those on other data sheets, we recommend that the read cycle data is used (especially where "Average" current consumption figures are specified).
3. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.
4. This speed grade is available in -55°C to +125°C temperature range only.

Capacitance[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

AC Test Conditions

Input pulse levels	GND to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

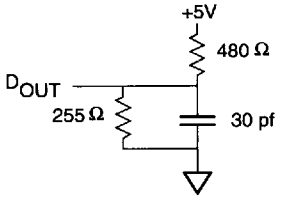


Fig. 1 Output Load Eqivalent

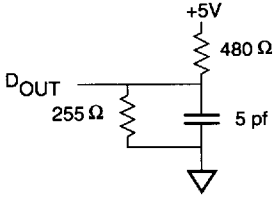
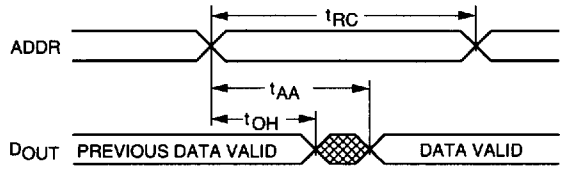
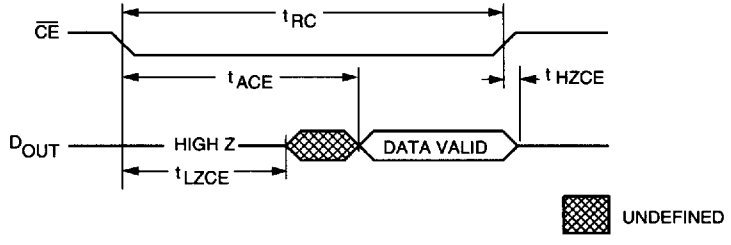


Fig. 2 Output Load Equivalent
(for t_{LZCE}, t_{HZCE}, t_{LZWE}, t_{HZWE}, t_{LZOE}, t_{HZOE})

Read Cycle No. 1[6, 7]



Read Cycle No. 2[3, 6, 8]



AC Electrical Characteristics V_{CC} = 5V ± 10%, All Temperature Ranges

Description		-20		-25		-35		-45		-55		
READ Cycle	**Sym**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
READ cycle time	t_{RC}	20		25		35		45		55		ns
Address access time	t_{AA}		20		25		35		45		55	ns
Chip enable access time	t_{ACE}		20		25		35		45		55	ns
Output hold from address change	t_{OH}	3		3		3		3		3		ns
Chip enable to output in low Z[2, 4]	t_{LZCE}	5		5		5		5		5		ns
Chip disable to output in high Z[2, 3, 4]	t_{HZCE}		10		10		15		18		20	ns
Chip enable to power up time[4]	t_{PU}	0		0		0		0		0		ns
Chip disable to power down time[4]	t_{PD}		20		25		30		40		50	ns
Output enable access time	t_{AOE}		8		8		12		15		20	ns
Output Enable to output in low Z[2, 4]	t_{LZOE}	0		0		0		0		0		ns
Output disable to output in high Z[2, 4]	t_{HZOE}		8		9		12		15		20	ns

Notes referenced are after Data Retention Table.

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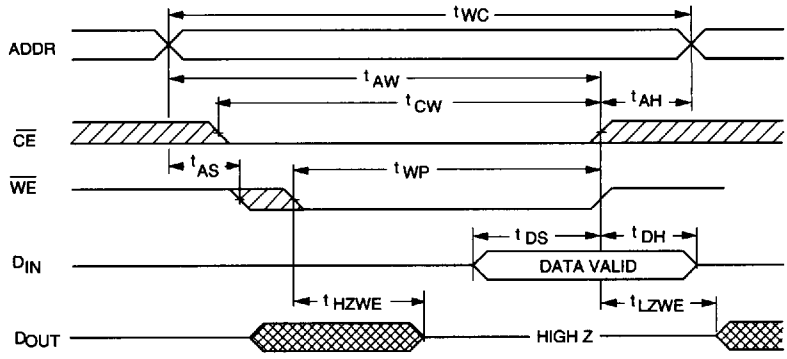
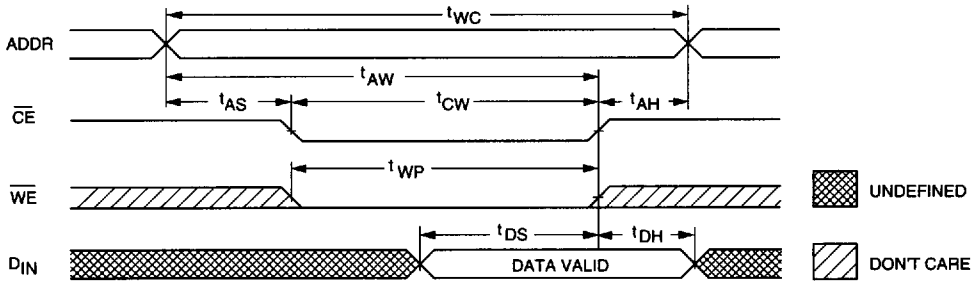
Write Cycle No. 1 (Write Enable Controlled)



Write Cycle No. 2 (Chip Enable Controlled)



AC Electrical Characteristics V_{CC} = 5V ± 10%, All Temperature Ranges

Description		-20		-25		-35		-45		-55[1]		
WRITE Cycle	**Sym**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
WRITE cycle time	t_{WC}	20		25		35		45		55		ns
Chip enable to end of write	t_{CW}	16		16		20		25		30		ns
Address Valid to end of write	t_{AW}	16		16		20		25		30		ns
Address set-up time	t_{AS}	0		0		0		0		0		ns
Address hold from end of write	t_{AH}	0		0		0		0		0		ns
Write pulse width	t_{WP}	16		16		20		25		30		ns
Data set-up time	t_{DS}	10		10		13		15		20		ns
Data hold time	t_{DH}	0		0		0		0		0		ns
Write disable to output in low Z[2, 4]	t_{LZWE}	0		0		0		0		0		ns
Write enable to output in high Z[2, 4]	t_{HZWE}		8		9		13		15		20	ns

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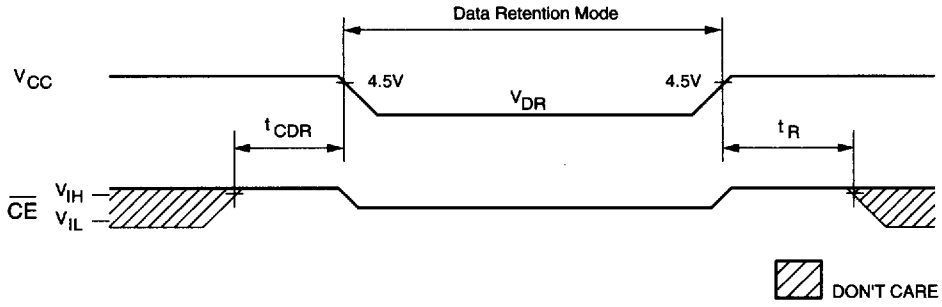
Low V_{CC} Data Retention Waveform



Data Retention Electrical Characteristics (L Version Only)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{DR}	V_{CC} for Retention Data			2	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{CC} - 0.2V$	$V_{CC} = 2V$	—	95	500	µA
		$V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	$V_{CC} = 3V$	—	350	750	µA
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(4)	Operation Recovery Time			t_{RC}(5)	—	—	ns

NOTES: (For 3 previous Electrical Characteristics tables)
1. -55°C to +125°C temperature range only.
2. The parameter is tested with CL = 5pF as shown in Fig. #2. Transition is measured ±200mV from steady state voltage.
3. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}.
4. This parameter is sampled.
5. t_{RC} = Read cycle time.
6. $\overline{WE}$ is high for a READ cycle.
7. The device is continuously selected. All the Chip Enables are held in their active state.
8. The address is valid prior to or coincident with the latest occuring Chip Enable.

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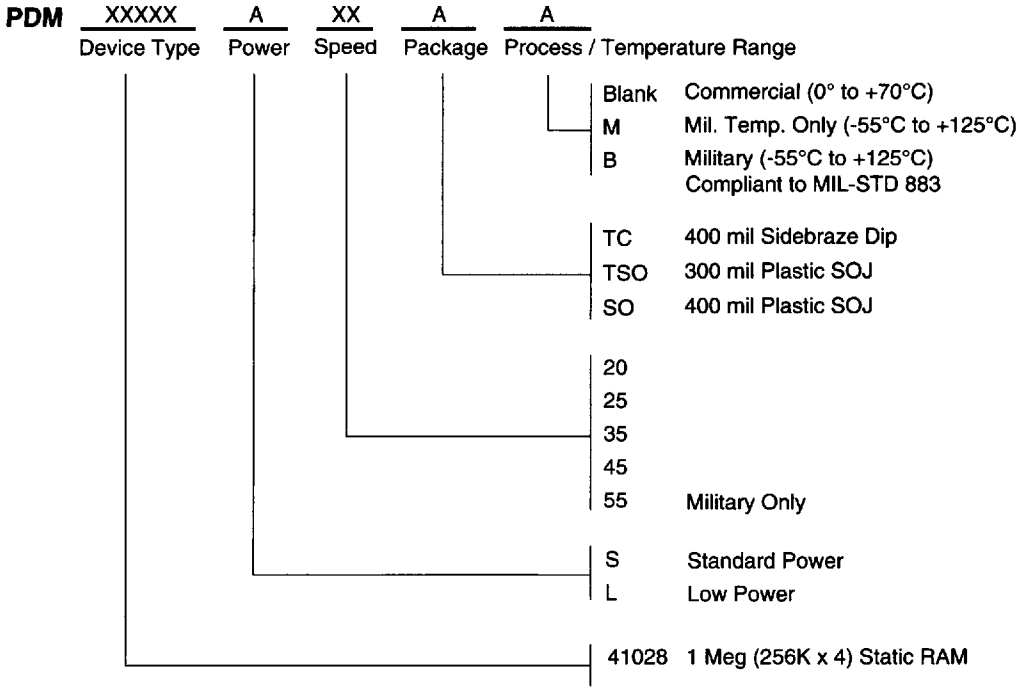
Ordering Information



Chip	Package Type	Page
PDM41028	28 pin Plastic SOJ 300 mil	6-10
	28 pin Plastic SOJ 400 mil	6-11
	28 pin Sidebraze DIP	6-13