TC74AC161/163
Synchronous Presettable 4-bit Counter

161: Binary, Asynchronous Clear
163: Binary, Synchronous Clear

Features:

- **High Speed:** f_{max} = 170MHz (typ.) at V_{CC} = 5V
- **Low Power Dissipation:** I_{CC} = 8μA (max.) at Ta = 25°C
- **High Noise Immunity:** $V_{NIH}=V_{NIL}$=28% V_{CC} (min.)
- **Symmetrical Output Impedance:** $|I_{OH}| = I_{OL}$ = 24mA (min.). Capability of driving 50Ω transmission lines.
- **Balanced Propagation Delays:** $t_{pLH} = t_{pHL}$
- **Wide Operating Voltage Range:** V_{CC}(opr)=2V~5.5V
- **Pin and Function Compatible with 74F161/163**
- **AC161 and AC163 Available in DIP, SOIC, and SSOP Packages**

The TC74AC161, and 163 are advanced high speed CMOS SYNCHRONOUS PRESETTABLE COUNTERs fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL, while maintaining the CMOS low power dissipation.

The TC74AC161/163 are 4 bit binary counters.

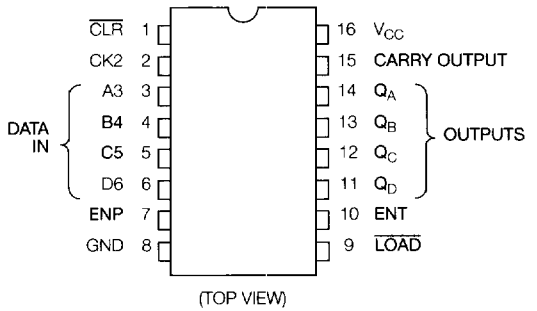
The CK input is active on the rising edge. Both $\overline{LOAD}$ and $\overline{CLR}$ inputs are active on low logic level. Presetting of all four ICs is synchronous to the rising edge of CK.

The clear function of the TC74AC163 is synchronous to CK, while the TC74AC161 is cleared asynchronously.

Two enable inputs (ENP and ENT) and CARRY OUTPUT are provided to enable easy cascading of counters, which facilitates easy implementation of n-bit counters without using external gates.

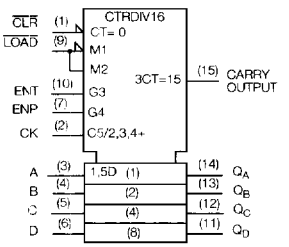
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Pin Assignment

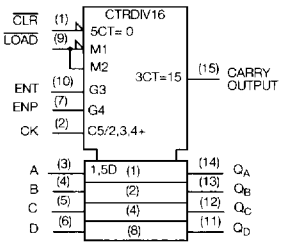


IEC Logic Symbol

TC74ACT161



TC74ACT163



Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±125	mA
Power Dissipation	P_D	500 (DIP) */180 (SOP)	mW
Storage Temperature	T_{stg}	-65~150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta = -40°C~65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C should be applied up to 300mW.

Recommended Operating Conditions

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	dt/dv	0~100 (V_{CC} = 3.3 ± 0.3V) 0~20 (V_{CC} = 5 ± 0.5V)	ns/v

DC Electrical Characteristics

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta = 25°C Min.	Ta = 25°C Typ.	Ta = 25°C Max.	Ta = -40~85°C Min.	Ta = -40~85°C Max.	UNIT
High-Level Input Voltage	V_{IH}	—		2.0	1.50	—	—	1.50	—	V
				3.0	2.10	—	—	2.10	—	
				5.5	3.85	—	—	3.85	—	
Low-Level Input Voltage	V_{IL}	—		2.0	—	—	0.50	—	0.50	V
				3.0	—	—	0.90	—	0.90	
				5.5	—	—	1.65	—	1.65	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I_{OH} = -4mA	3.0	2.58	—	—	2.48	—	
			I_{OH} = -24mA	4.5	3.94	—	—	3.80	—	
			I_{OH} = -75mA*	5.5	—	—	—	3.85	—	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I_{OL} = 12mA	3.0	—	—	0.36	—	0.44	
			I_{OL} = 24mA	4.5	—	—	0.36	—	0.44	
			I_{OL} = 75mA*	5.5	—	—	—	—	1.65	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	8.0	—	80.0	

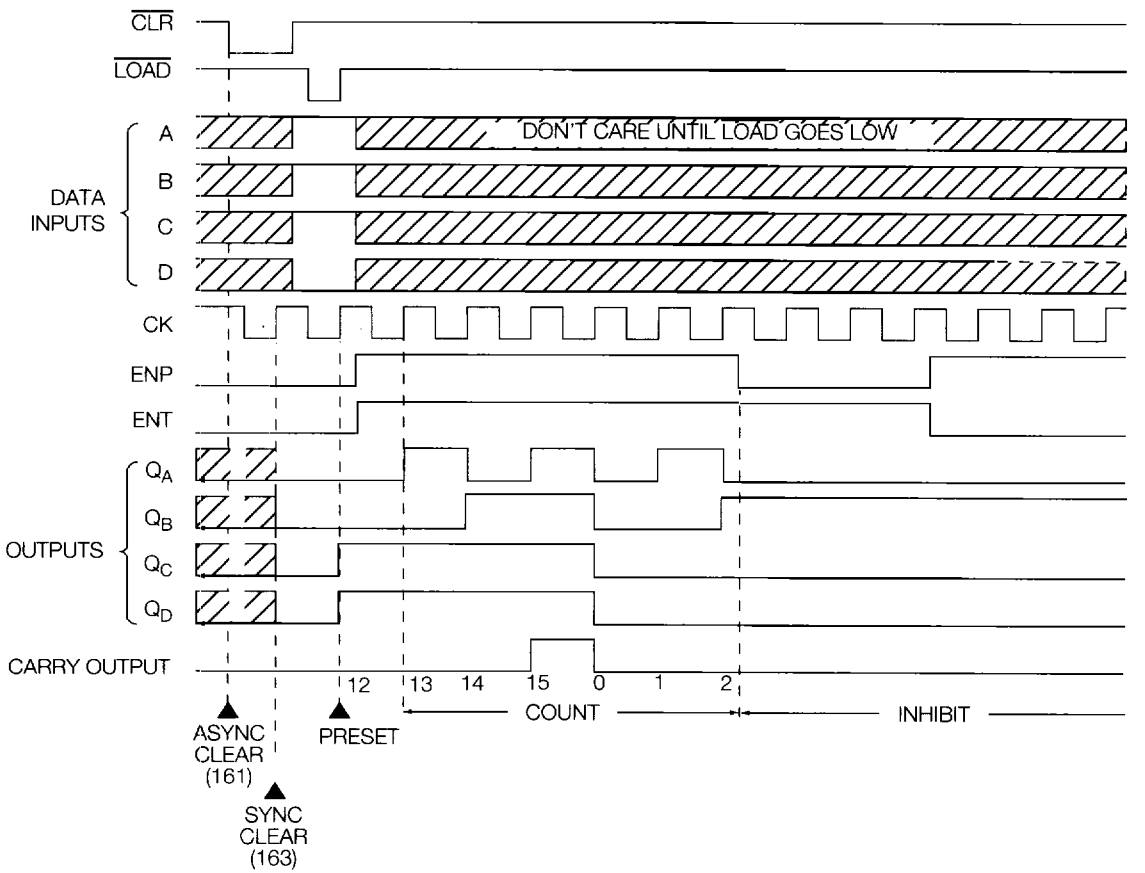
* This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

Truth Table

TC74AC161 INPUTS					TC74AC163 INPUTS					OUTPUTS				FUNCTION
CLR	LD	ENP	ENT	CK	CLR	LD	ENP	ENT	CK	Q_A	Q_B	Q_C	Q_D	
L	X	X	X	X	L	X	X	X	↑	L	L	L	L	RESET TO "0"
H	L	X	X	↑	H	L	X	X	↑	A	B	C	D	PRESET DATA
H	H	X	L	↑	H	H	X	L	↑	NO CHANGE				NO COUNT
H	H	L	X	↑	H	H	L	X	↑	NO CHANGE				NO COUNT
H	H	H	H	↑	H	H	H	H	↑	COUNT UP				COUNT
H	X	X	X	↑	X	X	X	X	↑	NO CHANGE				NO COUNT

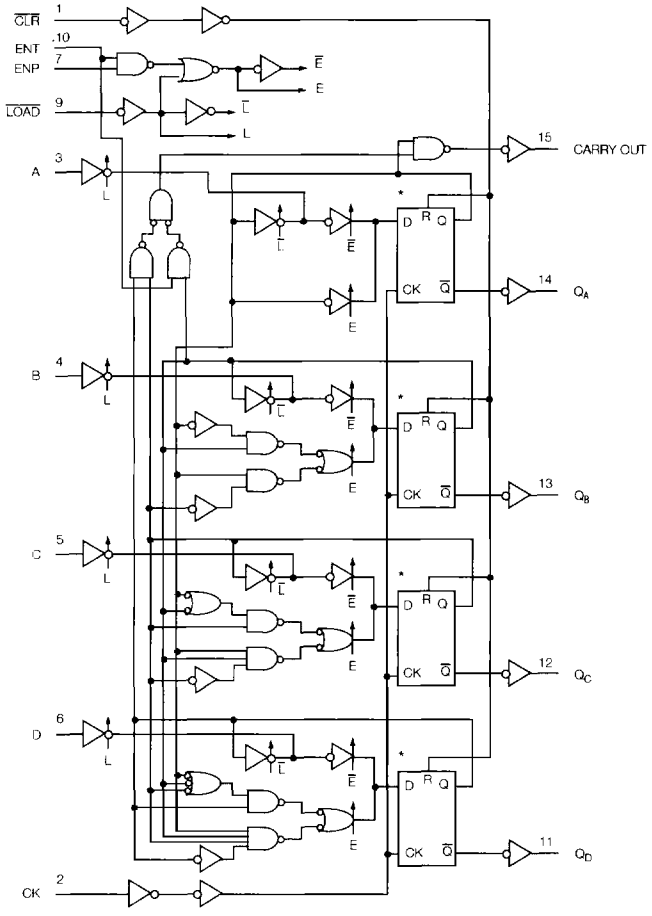
X : Don't care
A, B, C, D : Logic Level of Data Inputs
Carry : CARRY=ENT•Q_A•$\overline{Q}_B$•$\overline{Q}_C$•Q_D•••••(TC74AC160/162)
CARRY=ENT•Q_A•Q_B•Q_C•Q_D•••••(TC74AC161/163)

Timing Chart (TC74AC161/163: Binary Counter)



System Diagram

TC74AC161/TC74AC163



* Truth Table of Internal F/F

TC74AC161					TC74AC163				
D	CK	R	Q	$\overline{Q}$	D	CK	R	Q	$\overline{Q}$
X	X	H	L	H	X	↑	H	L	H
L	↑	L	L	H	L	↑	L	L	H
H	↑	L	H	L	H	↑	L	H	L
X	↓	L	NO CHANGE		L	↓	L	NO CHANGE	

X : Don't Care

Timing Requirements (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		Ta = -40~85°C	UNIT
			V_{CC}	Typ.	Max.	Max.	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$	Fig. 1	3.3±0.3	—	7.0	7.0	ns
			5.0±0.5	—	5.0	5.0	
Minimum Pulse Width ($\overline{CLR}$) *	$t_{W(L)}$	Fig. 4	3.3±0.3	—	7.0	7.0	
			5.0±0.5	—	5.0	5.0	
Minimum Set-up Time ($\overline{LOAD}$, ENP, ENT)	t_s	Fig. 2, 3	3.3±0.3	—	11.0	13.0	
			5.0±0.5	—	7.0	7.0	
Minimum Set-up Time (A, B, C, D)	t_s	Fig. 2	3.3±0.3	—	8.0	8.0	
			5.0±0.5	—	4.0	4.0	
Minimum Set-up Time ($\overline{CLR}$) * *	t_s	Fig. 5	3.3±0.3	—	6.0	6.0	
			5.0±0.5	—	4.0	4.0	
Minimum Hold Time	t_h	Fig. 2, 3, 5	3.3±0.3	—	1.0	1.0	
			5.0±0.5	—	1.0	1.0	
Minimum Removal Time ($\overline{CLR}$)*	t_{rem}	Fig. 4	3.3±0.3	—	6.0	6.0	
			5.0±0.5	—	4.0	4.0	

AC Electrical Characteristics (C_L = 50pF, R_L = 500Ω, Input $t_r = t_f$ = 3ns)

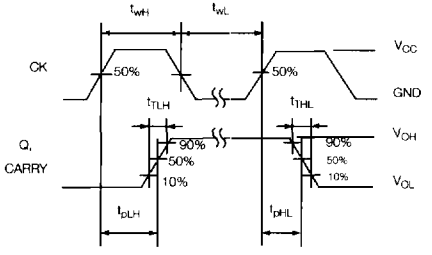
PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = -40~85°C		UNIT
			V_{CC}	Min.	Typ.	Max.	Min.	Max.	
Propagation Delay Time (CK–Q)	t_{pLH} t_{pHL}	Fig. 1	3.3±0.3	—	8.8	15.8	1.0	18.0	ns
			5.0±0.5	—	6.5	9.6	1.0	11.0	
Propagation Delay Time (CK–CARRY, Count Mode)	t_{pLH} t_{pHL}	Fig. 1	3.3±0.3	—	10.4	18.4	1.0	21.0	
			5.0±0.5	—	8.1	11.8	1.0	13.5	
Propagation Delay Time (CK–CARRY, Preset MODE)	t_{pLH} t_{pHL}	Fig. 2	3.3±0.3	—	12.9	22.4	1.0	25.5	
			5.0±0.5	—	9.1	13.2	1.0	15.0	
Propagation Delay Time (ENT–CARRY)	t_{pLH} t_{pHL}	Fig. 6	3.3±0.3	—	7.5	13.2	1.0	15.0	
			5.0±0.5	—	5.8	8.3	1.0	9.5	
Propagation Delay Time ($\overline{CLR}$–Q) *	t_{pHL}	Fig. 4	3.3±0.3	—	10.6	18.4	1.0	21.0	
			5.0±0.5	—	7.7	11.4	1.0	13.0	
Propagation Delay Time ($\overline{CLR}$–CARRY) *	t_{pHL}	Fig. 4	3.3±0.3	—	12.0	21.0	1.0	24.0	
			5.0±0.5	—	8.6	12.7	1.0	14.5	
Maximum Clock Frequency	f_{MAX}	—	3.3±0.3	50	110	—	50	—	MHz
			5.0±0.5	90	140	—	90	—	
Input Capacitance	C_{IN}	—	—	—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD} [1]	—	—	—	85	—	—	—	

Note (1): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC\ (opr)} = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}$.

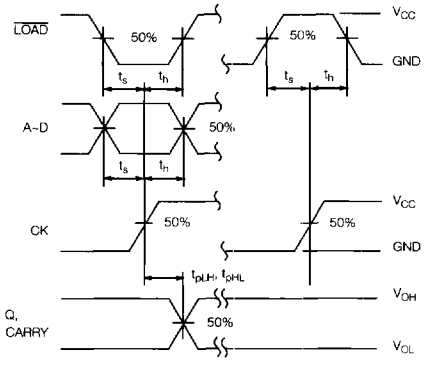
(2): *For TC74ACT161 only.
* *For TC74 ACT163 only.

Switching Characteristics Test Waveform

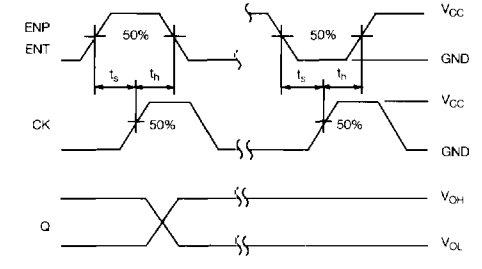
Count Mode (Fig. 1)



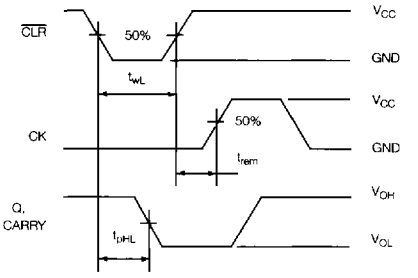
Preset Mode (Fig. 2)



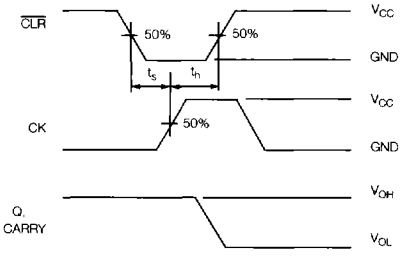
Count Enable Mode (Fig. 3)



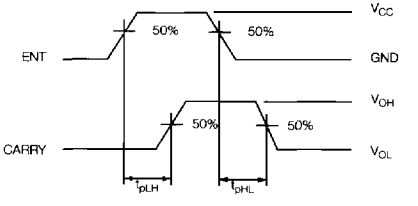
Clear Mode (TC74AC160/161) (Fig. 4)



Clear Mode (TC74AC162/163) (Fig. 5)



Cascade Mode (Fix Maximum Count) (Fig. 6)



Typical Application

Parallel Carry N-bit Counter