Signetics

FAST 74F8960, 74F8961
Futurebus Transceivers

FAST Products

Preliminary Specification for
74F8960-Octal Latched Bidirectional Futurebus Transceiver, INV (OC)
Product Specification for
74F8961-Octal Latched Bidirectional Futurebus Transceiver, NINV (OC)

TYPE	TYPICAL PROPAGATION DELAY	MAX SUPPLY CURRENT (TOTAL)
74F8960	7.5ns	85mA
74F8961	7.5ns	85mA

FEATURES

- Octal Latched Transceiver
- Drives heavily loaded backplanes with equivalent load impedances down to 10 ohms
- High drive (100mA) open collector drivers on B-port
- Reduced voltage swing (1 volt) produces less noise and reduces power consumption
- High speed operation enhances performance of backplane buses and facilitates incident wave switching
- Compatible with IEEE 896 Futurebus Standard
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Controlled output ramp and multiple GND pins minimize ground bounce
- Glitch-free power up / power down operation

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic DIP (600 mil)[1]	N74F8960N, N74F8961N
28-Pin PLCC[1]	N74F8960A, N74F8961A

NOTE:
1. Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	PNP latched inputs	3.5/0.0117	70µA/70µA
B_0 - B_7	Data inputs with threshold circuitry	5.0/0.167	100µA/100µA
OEA	A Output Enable input (active High)	1.0/0.033	20µA/20µA
$\overline{OEB}_0$, $\overline{OEB}_1$	B Output Enable inputs (active Low)	1.0//0.033	20µA/20µA
$\overline{LE}$	Latch Enable input (active Low)	1.0//0.033	20µA/20µA
A_0 - A_7	3-State outputs	150/40	3mA/24mA
B_0 - B_7	Open Collector outputs	OC*/166.7	OC*/100mA

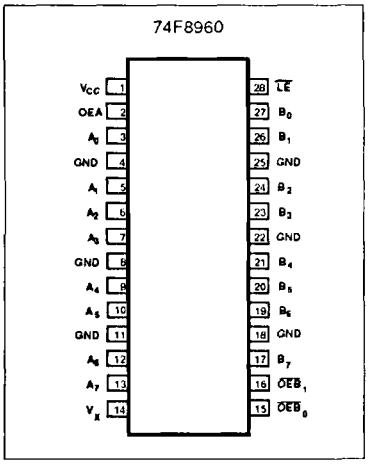
NOTES:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
* OC = Open Collector

DESCRIPTION

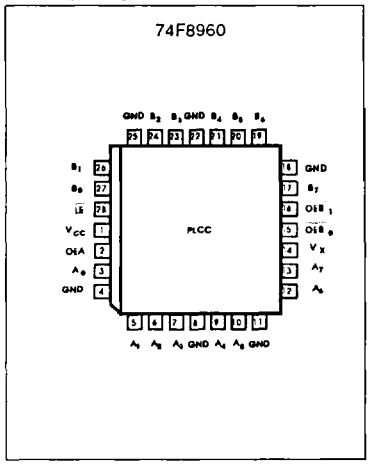
The 74F8960 and 74F8961 are octal bidirectional latched transceivers and are intended to provide the electrical interface to a high performance wired-OR bus. The B port inverting drivers are low-capacitance open collector with controlled ramp and are designed to sink 100 mA from 2 volts. The B port receivers have a 100 mV threshold region and a 4 ns glitch filter.

The B port interfaces to 'Backplane Transceiver Logic' (BTL). BTL features a reduced (1V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive loading (<5 pF).

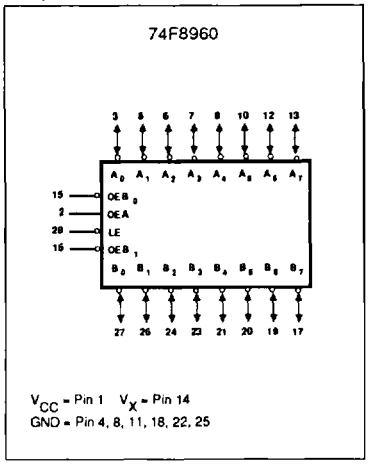
PIN CONFIGURATION DIP



PIN CONFIGURATION PLCC



LOGIC SYMBOL



Futurebus Transceivers

FAST 74F8960, 74F8961

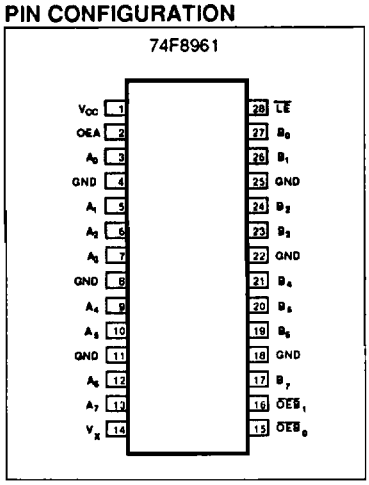
DESCRIPTION (Continued)

Incident wave switching is employed, therefore BTL propagation delays are short. Although the voltage swing is much less for BTL, so is its receiver threshold region, therefore noise margins are excellent.

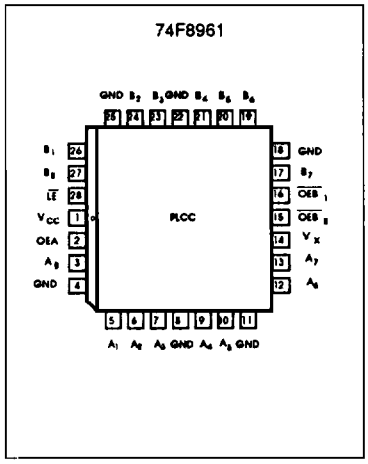
BTL offers low power consumption, low ground bounce, EMI and crosstalk, low capacitive loading, superior noise margin and low propagation delays. This results in a high bandwidth, reliable backplane. The 74F8960 and 74F8961 A ports have TTL 3-State drivers and TTL receivers with a latch function. A separate High level control input (V_X) is provided to limit the A port output level to a given voltage level (such as 3.3V). For 5.0V systems, V_x is simply tied to V_{CC}.

74F8961 is the non-inverting version of 74F8960.

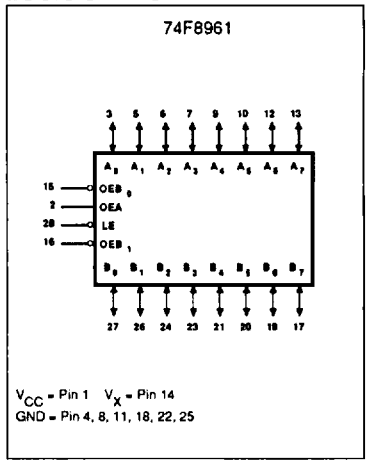
PIN CONFIGURATION



PIN CONFIGURATION PLCC



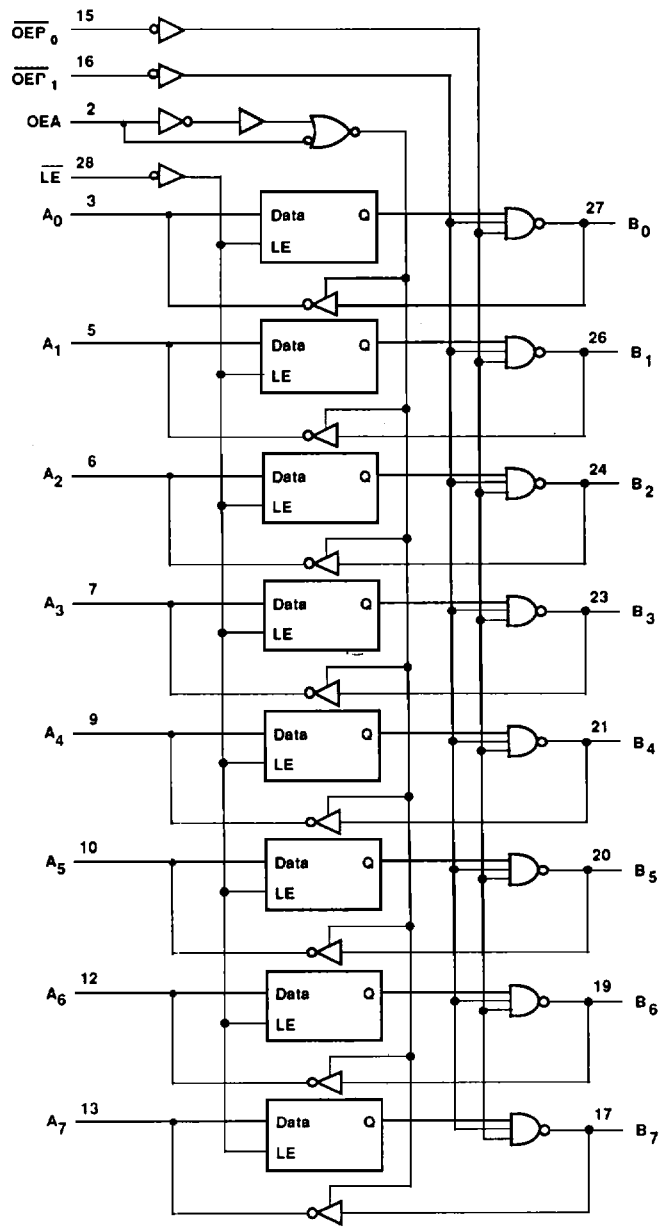
LOGIC SYMBOL



PIN DESCRIPTION

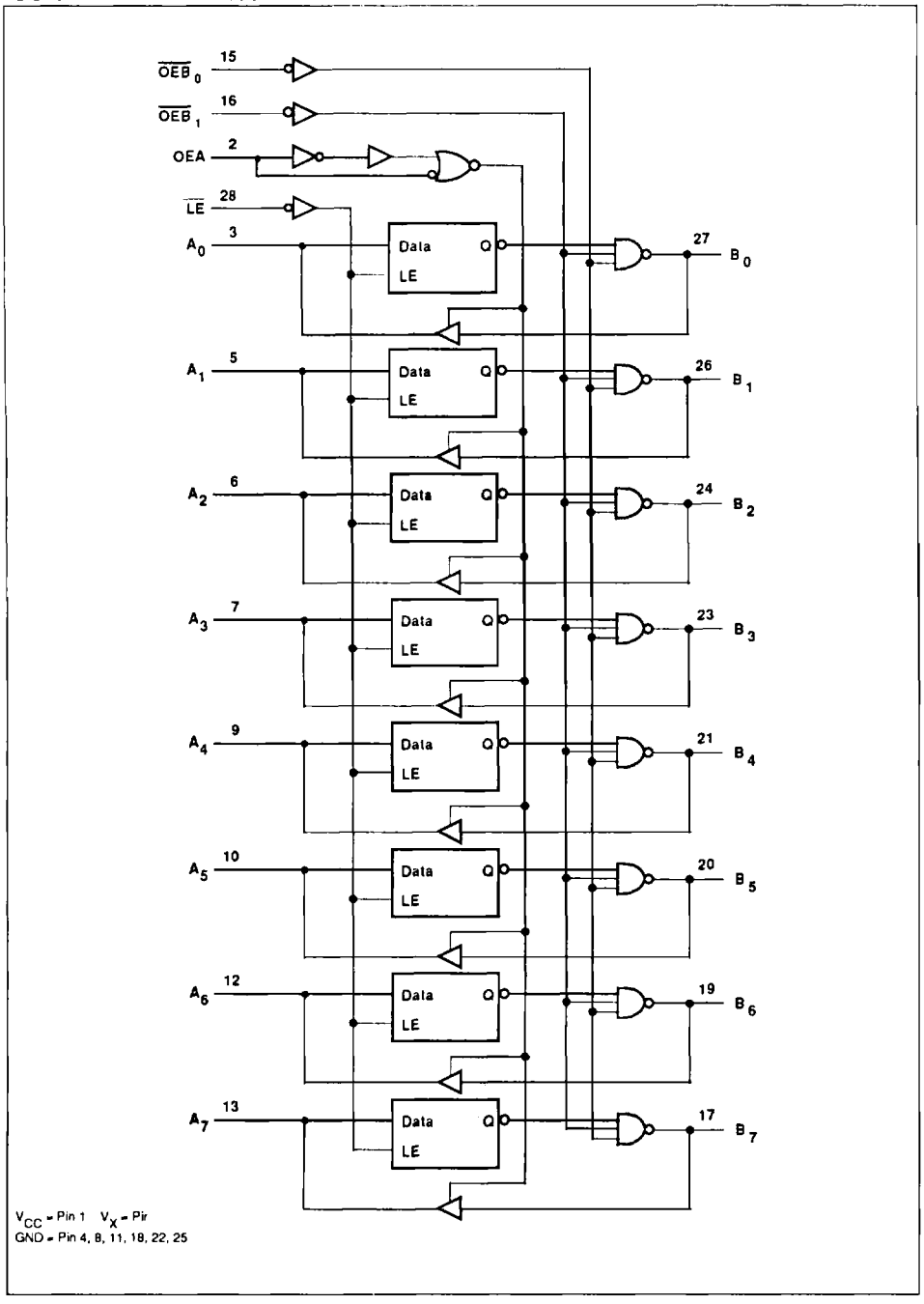
SYMBOL	PINS	TYPE	NAME AND FUNCTION
A_0	3	I/O	PNP latched input / 3-state output (with V_X control option)
A_1	5	I/O	
A_2	6	I/O	
A_3	7	I/O	
A_4	9	I/O	
A_5	10	I/O	
A_6	12	I/O	
A_7	13	I/O	
B_0	27	I/O	Data input with special threshold circuitry to reject noise / Open Collector output, High current drive
B_1	26	I/O	
B_2	24	I/O	
B_3	23	I/O	
B_4	21	I/O	
B_5	20	I/O	
B_6	19	I/O	
B_7	17	I/O	
$\overline{OEB}_0$	15	I	Enables the B outputs when both pins are Low
$\overline{OEB}_1$	16	I	
OEA	2	I	Enables the A outputs when High
$\overline{LE}$	28	I	Latched when High (a special delay feature is built in for proper enabling times)
V_X	14	I	Clamping voltage keeping V_{OH} from rising above V_X ($V_X = V_{CC}$ for normal use)

LOGIC DIAGRAM 74F8960



V_{CC} = Pin 1 V_X = Pin 14
GND = Pin 4, 8, 11, 18, 22, 25

LOGIC DIAGRAM 74F8961



FUNCTION TABLE 74F8960

INPUTS						LATCH	OUTPUTS		MODE
A_n	B_n*	$\overline{LE}$	OEA	$\overline{OEB_0}$	$\overline{OEB_1}$	STATE	A_n	B_n	
H	X	L	L	L	L	H	Z	L	A 3-state, Data from A to B
L	X	L	L	L	L	L	Z	H**	
X	X	H	L	L	L	Q_n	Z	$\overline{Q}_n$	A 3-state, Latched data to B
–	–	L	H	L	L	(1)	(1)	(1)	Feedback: A to B, B to A
–	H	H	H	L	L	L(2)	L	Z(2)	Preconditioned Latch enabling data transfer from B to A
–	L	H	H	L	L	L(2)	H	Z(2)	
–	–	H	H	L	L	Q_n	$\overline{Q}_n$	$\overline{Q}_n$	Latch state to A and B
H	X	L	L	H	X	H	Z	Z	B and A 3-state
L	X	L	L	H	X	L	Z	Z	
X	X	H	L	H	X	Q_n	Z	Z	
–	H	L	H	H	X	H	L	Z	B 3-state, Data from B to A
–	L	L	H	H	X	L	H	Z	
–	H	H	H	H	X	Q_n	L	Z	
–	L	H	H	H	X	Q_n	H	Z	
H	X	L	L	X	H	H	Z	Z	B and A 3-state
L	X	L	L	X	H	L	Z	Z	
X	X	H	L	X	H	Q_n	Z	Z	
–	H	L	H	X	H	H	L	Z	B 3-state, Data from B to A
–	L	L	H	X	H	L	H	Z	
–	H	H	H	X	H	Q_n	L	Z	
–	L	H	H	X	H	Q_n	H	Z	

H = High voltage level
L = Low voltage level
X = Don't care
– = Input not externally driven
Z = High Impedance (off) state
Q_n = High or Low voltage level one setup time prior to the Low-to-High $\overline{LE}$ transition
(1) = Condition will cause a feedback loop path; A to B and B to A
(2) = The latch must be preconditioned such that B inputs may assume a High or Low level while $\overline{OEB}_0$ and $\overline{OEB}_1$ are Low and $\overline{LE}$ is High.
H** = Goes to level of pullup voltage.
B* = Precaution should be taken to insure B inputs do not float. If they do they are equal to Low state.

FUNCTION TABLE. 74F8961

INPUTS						LATCH	OUTPUTS		MODE
A_n	B_n*	$\overline{LE}$	OEA	$\overline{OEB}_0$	$\overline{OEB}_1$	STATE	A_n	B_n	
H	X	L	L	L	L	H	Z	H**	A 3-state, Data from A to B
L	X	L	L	L	L	L	Z	L	
X	X	H	L	L	L	Q_n	Z	Q_n	A 3-state, Latched data to B
–	–	L	H	L	L	(1)	(1)	(1)	Feedback: A to B, B to A
–	H	H	H	L	L	H(2)	H	Z(2)	Preconditioned Latch enabling data transfer from B to A
–	L	H	H	L	L	H(2)	L	Z(2)	
–	–	H	H	L	L	Q_n	Q_n	Q_n	Latch state to A and B
H	X	L	L	H	X	H	Z	Z	B and A 3-state
L	X	L	L	H	X	L	Z	Z	
X	X	H	L	H	X	Q_n	Z	Z	
–	H	L	H	H	X	H	H	Z	B 3-state, Data from B to A
–	L	L	H	H	X	L	L	Z	
–	H	H	H	H	X	Q_n	H	Z	
–	L	H	H	H	X	Q_n	L	Z	
H	X	L	L	X	H	H	Z	Z	B and A 3-state
L	X	L	L	X	H	L	Z	Z	
X	X	H	L	X	H	Q_n	Z	Z	
–	H	L	H	X	H	H	H	Z	B 3-state, Data from B to A
–	L	L	H	X	H	L	L	Z	
–	H	H	H	X	H	Q_n	H	Z	
–	L	H	H	X	H	Q_n	L	Z	

H = High voltage level
L = Low voltage level
X = Don't care
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Q_n = High or Low voltage level one setup time prior to the Low-to-High $\overline{LE}$ transition
(1) = Condition will cause a feedback loop path; A to B and B to A
(2) = The latch must be preconditioned such that B inputs may assume a High or Low level while $\overline{OEB}_0$ and $\overline{OEB}_1$ are Low and $\overline{LE}$ is High.
H** = Goes to level of pullup voltage.
B* = Precaution should be taken to insure B inputs do not float. If they do they are equal to Low state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_X	Threshold control		-0.5 to +7.0	V
V_{IN}	Input voltage	$\overline{OEB}_0$, OEA, $\overline{LE}$	-0.5 to +7.0	V
		A_0 - A_7, B_0 - B_7	-0.5 to 5.5	
I_{IN}	Input current		-40 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	A_0 - A_7	48	mA
		B_0 - B_7	200	
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage	Except B_0 - B_7	2.0			V
		B_0 - B_7	1.625			
V_{IL}	Low-level input voltage	Except B_0 - B_7			0.8	V
		B_0 - B_7			1.475	
I_{IK}	Input clamp current	Except A_0 - A_7			-18	mA
		A_0 - A_7			-40	
I_{OH}	High-level output current	A_0 - A_7			-3	mA
I_{OL}	Low-level output current	A_0 -A_7			24	mA
		B_0 - B_7			100	
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
I_{OH}	High level output current	B_0 - B_7	V_{CC} = MAX, V_{IL} =MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
I_{OFF}	Power-off output current	B_0 - B_7	V_{CC} = 0.0V, V_{IL} =MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
V_{OH}	High-level output voltage	A_0 - A_7[4]	V_{CC} = MIN, V_{IL} = MAX,	I_{OH} = -3mA, V_X = V_{CC}	2.5		V_{CC}	V
			V_{IH} = MIN	I_{OH} = -0.4mA, V_X = 3.13V & 3.47V	2.5		V_X	V
V_{OL}	Low-level output voltage	A_0 - A_7[4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 20mA, V_X = V_{CC}			0.5	V
		B_0 - B_7	V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = 100mA			1.15	V
			V_{IH} = MIN	I_{OL} = 4mA	0.40			V
V_{IK}	Input clamp voltage	A_0 - A_7	V_{CC} = MIN, I_I = I_{IK}				-0.5	V
		Except A_0 - A_7	V_{CC} = MIN, I_I = I_{IK}				-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEB}_n$, OEA, $\overline{LE}$	V_{CC} = 0.0V, V_I = 7.0V				100	µA
		A_0 - A_7, B_0 - B_7	V_{CC} = MAX, V_I = 5.5V				1	mA
I_{IH}	High-level input current	$\overline{OEB}_n$, OEA, $\overline{LE}$	V_{CC} = MAX, V_I = 2.7V, B_n - A_n = 0V				20	µA
		B_0 - B_7	V_{CC} = MAX, V_I = 2.1V				100	µA
I_{IL}	Low-level input current	$\overline{OEB}_n$, OEA, $\overline{LE}$	V_{CC} = MAX, V_I = 0.5V				-20	µA
		B_0 - B_7	V_{CC} = MAX, V_I = 0.3V				-100	µA
I_{OZH} + I_{IH}	Off-state output current, High-level voltage applied	A_0 - A_7	V_{CC} = MAX, V_O =2.7V				70	µA
I_{OZL} + I_{IL}	Off-state output current, Low-level voltage applied	A_0 - A_7	V_{CC} = MAX, V_O =0.5V				-70	µA
I_X	High-level control current		V_{CC} = MAX, V_X = V_{CC}, $\overline{LE}$ = OEA = $\overline{OEB}_n$ = 2.7V, A_0 - A_7 = 2.7V, B_0 - B_7 = 2.0V		-100		100	µA
			V_{CC} = MAX, V_X = 3.13V & 3.47 V, $\overline{LE}$ = OEA = 2.7V, $\overline{OEB}_n$ =A_0 - A_7 = 2.7V, B_0 - B_7 = 2.0V		-10		10	mA
I_{OS}	Short-circuit output current[3]	A_0 - A_7 only	V_{CC} = MAX, B_n = 1.6V, OEA = 2.0V, $\overline{OEB}_n$ = 2.7V		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			70	100	mA
		I_{CCL}	V_{CC} = MAX, V_{IL} = 0.5V			100	145	mA
		I_{CCZ}	V_{CC} = MAX, V_{IL} = 0.5V			80	100	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type. Unless otherwise specified, V_X = V_{CC} for all test conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are for V_{IH}=1.6V and V_{IL}=1.3V.

AC ELECTRICAL CHARACTERISTICS for 74F8960

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay B to A	Waveform 1, 2	5.5 6.0	7.5 7.5	12.0 10.5	5.0 6.0	12.0 11.0	ns
t_{PZH} t_{PZL}	Output Enable time from High or Low OEA to A	Waveform 4.5	8.0 8.5	10.5 12.0	14.5 14.5	7.5 8.5	15.5 17.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low OEA to A	Waveform 4.5	2.0 2.0	4.5 4.5	7.0 7.5	2.0 2.0	7.5 8.0	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_D = 30pF, R_U = 9Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_D = 30pF, R_U = 9Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A to B	Waveform 1, 2	2.0 3.5	4.0 6.0	7.0 8.0	2.0 3.0	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}$ to B	Waveform 1, 2	3.0 4.0	5.0 6.0	8.5 9.0	2.5 3.0	10.0 9.5	ns
t_{PLH} t_{PHL}	Enable/disable time $\overline{OEB_n}$ to B	Waveform 1, 2	2.5 4.5	4.5 7.5	7.5 10.5	1.5 3.5	8.5 10.5	ns
t_{TLH} t_{THL}	Transition time, B Port 1.3V to 1.7 V, 1.7V to 1.3V	Test Circuit and Waveforms	0.5 0.5	2.0 2.0	4.5 4.5	0.5 0.5	4.5 4.5	ns

AC SETUP REQUIREMENTS for 74F8960

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time A to $\overline{LE}$	Waveform 3	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time A to $\overline{LE}$	Waveform 3	0.0 0.0			0.0 0.0		ns
$t_w(L)$	$\overline{LE}$ Pulse width, Low	Waveform 3	6.0			6.0		ns

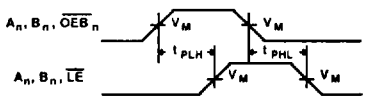
AC ELECTRICAL CHARACTERISTICS for 74F8961

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay B to A	Waveform 1, 2	5.5 6.0	7.5 7.5	12.0 10.5	5.0 6.0	12.0 11.0	ns
t_{PZH} t_{PZL}	Output Enable time from High or Low OEA to A	Waveform 4.5	8.0 8.5	10.5 12.0	14.5 14.5	7.5 8.5	15.5 17.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low OEA to A	Waveform 4.5	2.0 2.0	4.5 4.5	7.0 7.5	2.0 2.0	7.5 8.0	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_D = 30pF, R_U = 9Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_D = 30pF, R_U = 9Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A to B	Waveform 1, 2	2.0 3.5	4.0 6.0	7.0 8.0	2.0 3.0	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}$ to B	Waveform 1, 2	3.0 4.0	5.0 6.0	8.5 9.0	2.5 3.0	10.0 9.5	ns
t_{PLH} t_{PHL}	Enable/disable time $\overline{OEB}_n$ to B	Waveform 1, 2	2.5 4.5	4.5 7.5	7.5 10.5	1.5 3.5	8.5 10.5	ns
t_{TLH} t_{THL}	Transition time, B Port 1.3V to 1.7 V, 1.7V to 1.3V	Test Circuit and Waveforms	0.5 0.5	2.0 2.0	4.5 4.5	0.5 0.5	4.5 4.5	ns

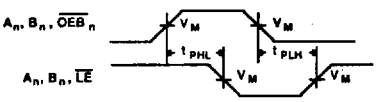
AC SETUP REQUIREMENTS for 74F8961

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time A to $\overline{LE}$	Waveform 3	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time A to $\overline{LE}$	Waveform 3	0.0 0.0			0.0 0.0		ns
$t_w(L)$	$\overline{LE}$ Pulse width, Low	Waveform 3	6.0			6.0		ns

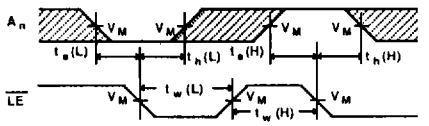
AC WAVEFORMS



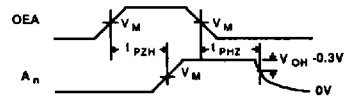
Waveform 1. Propagation Delay For Data To Output



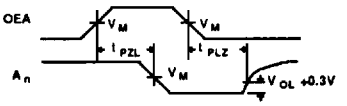
Waveform 2. Propagation Delay For Data To Output



Waveform 3. Data Setup And Hold Times And $\overline{LE}$ Pulse Widths



Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level

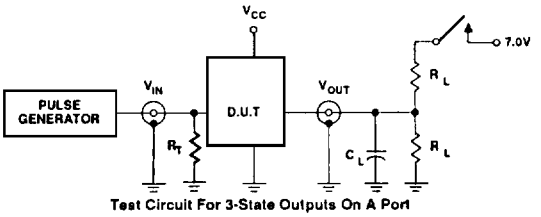


Waveform 5 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

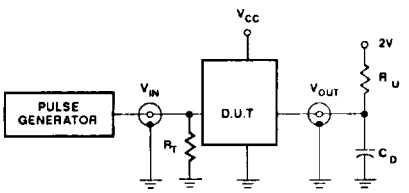
TEST CIRCUIT AND WAVEFORMS



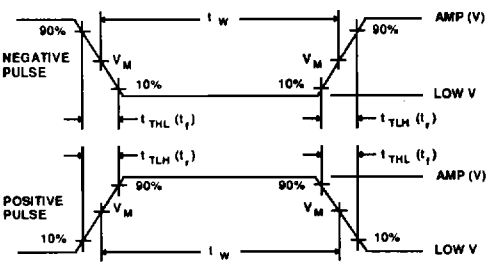
Test Circuit For 3-State Outputs On A Port

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test Circuit For Outputs On B Port



V_M = 1.5V

Input Pulse Definition

FAMILY 74F	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	4.0ns	4.0ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_U = Pull up resistor; see AC CHARACTERISTICS for value.