National Semiconductor

54ACTQ/74ACTQ16240
16-Bit Inverting Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'ACTQ16240 contains sixteen inverting buffers with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate TRI-STATE control inputs which can be shorted together for full 16-bit operation.

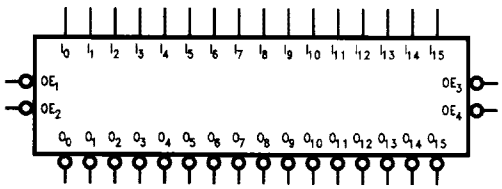
The 'ACTQ16240 utilizes NSC Quiet Series technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control for superior performance.

Features

- Utilizes NSC FACT Quiet Series technology
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin output skew
- Separate control logic for each byte
- 16-bit version of the 'ACTQ240
- Outputs source/sink 24 mA
- Additional specs for multiple output switching
- Output loading specs for both 50 pF and 250 pF loads

Ordering Code: See Section 8

Logic Symbol



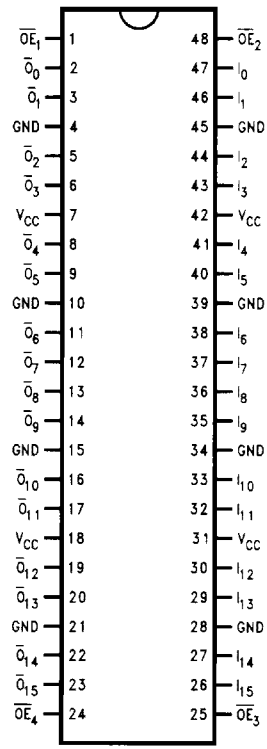
TL/F/10924–1

Pin Description

Pin Names	Description
$\overline{OE}_n$	Output Enable Inputs (Active Low)
I_0–I_{15}	Inputs
$\overline{O}_0$–$\overline{O}_{15}$	Outputs

Connection Diagram

Pin Assignment for SSOP and CERPAK

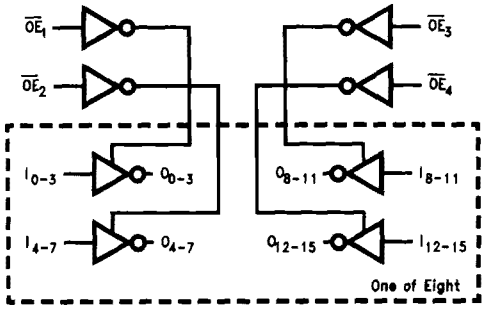


TL/F/10924–2

Functional Description

The 'ACTQ16240 contains sixteen inverting buffers with TRI-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins may be shorted together to obtain full 16-bit operation. The TRI-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input for each nibble. When $\overline{OE}_n$ is LOW, the outputs are in 2-state mode. When $\overline{OE}_n$ is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Logic Diagram



TL/F/10924-3

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_0–I_3	$\overline{O}_0$–$\overline{O}_3$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_4–I_7	$\overline{O}_4$–$\overline{O}_7$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I_8–I_{11}	$\overline{O}_8$–$\overline{O}_{11}$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	I_{12}–I_{15}	$\overline{O}_{12}$–$\overline{O}_{15}$
L	L	H
L	H	L
H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source/Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin	±50 mA
Junction Temperature	
CDIP	+175°C
PDIP/SOIC	+140°C
Storage Temperature	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACTQ	−40°C to +85°C
54ACTQ	−55°C to +125°C
Minimum Input Edge Rate (dV/dt)	
'ACTQ Devices	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

DC Electrical Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ T_A = +25°C		54ACTQ T_A = −55°C to +125°C	74ACTQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Output Voltage	4.5	4.49	4.4	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4	5.4		
								V_{IN}* = V_{IL} or V_{IH}
		4.5		3.86	3.70	3.76	V	I_{OH} −24 mA
		5.5		4.86	4.70	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1		
								V_{IN}* = V_{IL} or V_{IH}
		4.5		0.36	0.50	0.44	V	I_{OL} 24 mA
		5.5		0.36	0.50	0.44		I_{OL} 24 mA
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{CC}	Max Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND (Note 5)
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}					50	−75	mA	V_{OHD} = 3.85V Min

* All outputs loaded; thresholds associated with output under test.

† Maximum test duration 2.0 ms; one output loaded at a time.

DC Electrical Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$ Typ	74ACTQ $T_A = +25°C$ Guaranteed Limits	54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	0.5	0.8			V	*Figures 2-12, 13* (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.5	−1.0			V	*Figures 2-12, 13* (Notes 2, 3)
V_{OHP}	Maximum Overshoot	5.0	V_{OH} + 1.0	V_{OH} + 1.5			V	*Figures 2-12, 13* (Notes 1, 3)
V_{OHV}	Minimum V_{CC} Droop	5.0	V_{OH} − 1.0	V_{OH} − 1.8			V	*Figures 2-12, 13* (Notes 1, 3)
V_{IHD}	Minimum High Dynamic Input Voltage Level	5.0	1.7	2.0			V	(Notes 1, 4)
V_{ILD}	Maximum Low Dynamic Input Voltage Level	5.0	1.2	0.8			V	(Notes 1, 4)

Note 1: Worst case package.
Note 2: Maximum number of outputs that can switch simultaneously is n. (n − 1) outputs are switched LOW and one output held LOW.
Note 3: Maximum number of outputs that can switch simultaneously is n. (n − 1) outputs are switched HIGH and one output held HIGH.
Note 4: Maximum number of data inputs (n) switching. (n − 1) input switching 0V to 3V ('ACTQ). Input under test switching 3V to threshold (V_{ILD}).
Note 5: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF Min	Max	74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units	Fig. No.
t_{PLH}, t_{PHL}	Propagation Delay Data to Output	5.0	2.7 3.0	4.8 5.1	7.3 7.3	3.0 3.0	9.0 9.0	2.7 3.0	7.8 7.8	ns	2-3, 4
t_{PZH}, t_{PZL}	Output Enable Time	5.0	2.5 2.7	4.5 4.7	7.4 7.5	2.8 3.1	9.5 10.2	2.5 2.7	7.9 8.0	ns	2-5, 6
t_{PHZ}, t_{PLZ}	Output Disable Time	5.0	2.3 2.0	5.0 4.6	7.9 7.4	2.3 2.0	9.3 8.7	2.3 2.0	8.2 7.9	ns	2-5, 6

*Voltage Range 5.0 is 5.0V ±0.5V.

Extended AC Electrical Characteristics

Symbol	Parameter	74ACTQ $T_A = -40°C$ to $+85°C$, V_{CC} = Com, $C_L = 50$ pF, 16 Outputs Switching (Note 2) Min	Typ	Max	54ACTQ T_A = Mil, V_{CC} = Mil, $C_L = 50$ pF, 16 Outputs Switching (Note 2) Min	Max	74ACTQ $T_A = -40°C$ to $+85°C$, V_{CC} = Com, $C_L = 250$ pF (Note 3) Min	Max	54ACTQ T_A = Mil, V_{CC} = Mil, $C_L = 250$ pF (Note 3) Min	Max	Units	Fig. No.
t_{PLH}, t_{PHL}	Propagation Delay Data to Output	4.0 4.0		11.2 10.0	4.0 4.0	11.9 10.6	5.6 5.6	13.8 13.6	5.6 5.6	14.6 14.5	ns	2–3, 4
t_{PZH}, t_{PZL}	Output Enable Time	3.5 3.4		10.1 10.0	3.5 3.4	10.8 10.7	(Note 4)		(Note 4)		ns	2–5, 6

Extended AC Electrical Characteristics (Continued)

Symbol	Parameter	74ACTQ $T_A = -40°C$ to $+85°C$ V_{CC} = Com C_L = 50 pF 16 Outputs Switching (Note 2)			54ACTQ T_A = Mil V_{CC} = Mil C_L = 50 pF 16 Outputs Switching (Note 2)		74ACTQ $T_A = -40°C$ to $+85°C$ V_{CC} = Com C_L = 250 pF (Note 3)		54ACTQ T_A = Mil V_{CC} = Mil C_L = 250 pF (Note 3)		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max	Min	Max		
t_{PHZ} t_{PLZ}	Output Disable Time	3.6 3.1		8.9 8.1	3.6 3.1	9.3 8.7	(Note 5)		(Note 5)		ns	2–5, 6
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output			1.2							ns	
t_{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output			2.5							ns	
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Data to Output			4.3							ns	

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}).

Note 2: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 3: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 4: TRI-STATE delays are load dominated and have been excluded from the datasheet.

Note 5: The Output Disable Time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Capacitance

Symbol	Parameter		Typ	Units	Conditions
C_{IN}	Input Pin Capacitance		4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	54ACTQ	95	pF	V_{CC} = 5.0V
		74ACTQ	30	pF	V_{CC} = 5.0V