SYNCHRONOUS SRAM

128K x 36 SRAM

+3.3V SUPPLY, FLOW-THROUGH AND SELECTABLE BURST MODE

FEATURES

- Fast access times: 9, 10, 11, 12 and 14ns
- Fast $\overline{OE}$ access times: 5 and 6ns
- Single +3.3V ±5% power supply
- SNOOZE MODE for reduced power standby
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock controlled, registered, address, data and control
- Internally self-timed WRITE cycle
- Burst control pin (interleaved or linear burst)
- 100-lead TQFP package for high density, high speed
- Low capacitive bus loading
- High 30pF output drive capability at rated access time
- DIMMs also available

OPTIONS	MARKING
• Timing	
9ns access/15ns cycle	- 9
10ns access/15ns cycle	-10
11ns access/15ns cycle	-11
12ns access/20ns cycle	-12
14ns access/20ns cycle	-14
• Packages	
100-pin TQFP	LG
• Low power	P
• 2V data retention, low power	L

- Part Number Example: MT58LC128K36B2LG-12 P

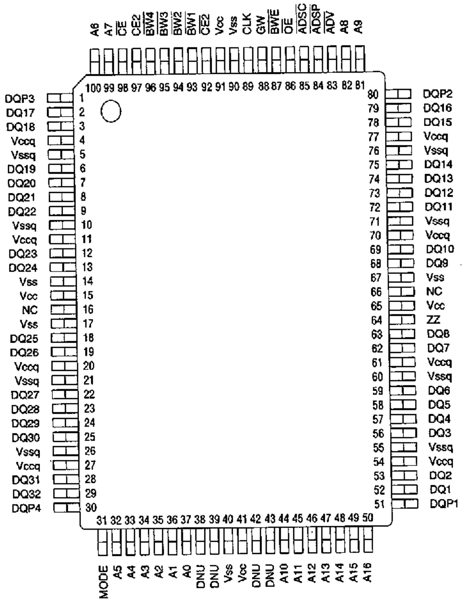
GENERAL DESCRIPTION

The Micron SyncBurst™ SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT58LC128K36B2 SRAM integrates a 128K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable ($\overline{CE}$), two additional chip enables for easy depth expansion (CE2, $\overline{CE2}$), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$), byte write enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$, $\overline{BWE}$) and global write ($\overline{GW}$).

PIN ASSIGNMENT (Top View)

100-Pin TQFP (SB-1)



Asynchronous inputs include the output enable ($\overline{OE}$), snooze enable (ZZ), clock (CLK) and burst mode (MODE). The data-out (Q), enabled by $\overline{OE}$, is also asynchronous. WRITE cycles can be from 1 to 4 bytes wide as controlled by the write control inputs.

Burst operation can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin ($\overline{ADV}$).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written.

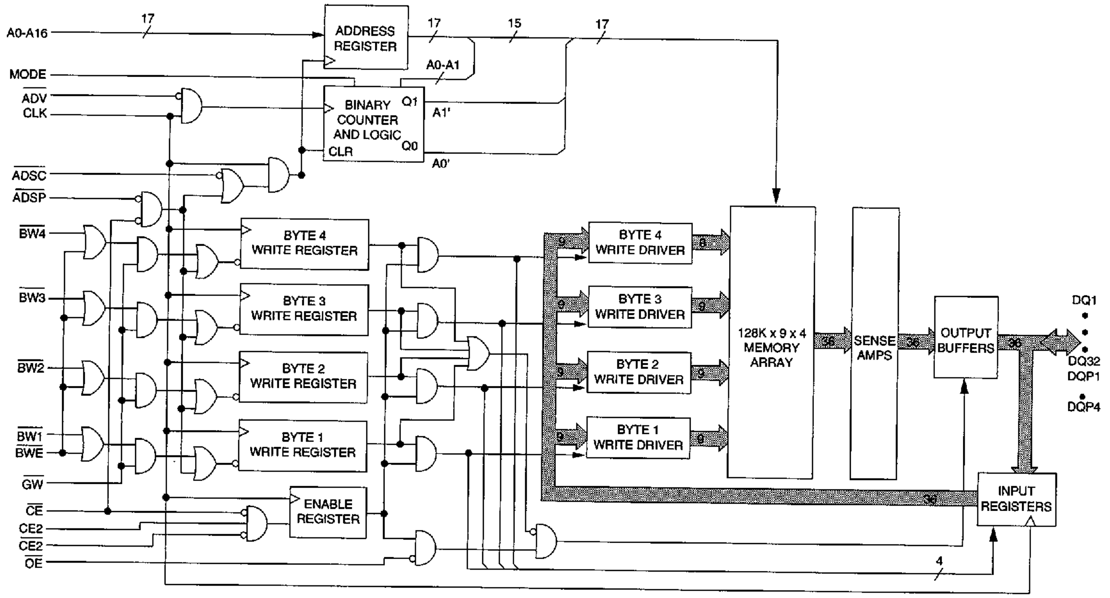
GENERAL DESCRIPTION (continued)

BW1 controls DQ1-DQ8 and DQP1, BW2 controls DQ9-DQ16 and DQP2, BW3 controls DQ17-DQ24 and DQP3, and BW4 controls DQ25-DQ32 and DQP4, conditioned by BWE being LOW. GW LOW causes all bytes to be written.

The "L" version of this device has a data retention option which is useful for battery backup mode of operation. Although the part is not guaranteed to operate functionally below Vcc MIN (3.1V), it will retain data with a minimum of power dissipation.

The MT58LC128K36B2 operates from a +3.3V power supply and all inputs and outputs are TTL-compatible and 5V-tolerant. The device is ideally suited for 486, Pentium™, 680X0 and PowerPC™ systems and systems that benefit from a very wide data bus. The device is also ideal in generic 36- and 72-bit-wide applications.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. The Functional Block Diagram illustrates simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

PIN DESCRIPTIONS

TQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49, 50	A0-A16	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
93, 94, 95, 96	$\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written when $\overline{BWE}$ is LOW and must meet the setup and hold times around the rising edge of CLK. A Byte Write Enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW1}$ controls DQ1-DQ8 and DQP1. $\overline{BW2}$ controls DQ9-DQ16 and DQP2. $\overline{BW3}$ controls DQ17-DQ24 and DQP3. $\overline{BW4}$ controls DQ25-DQ32 and DQP4. Data I/O are tristated if any of these four inputs are LOW.
89	CLK	Input	Clock: This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	$\overline{CE}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
92	$\overline{CE2}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
86	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
83	$\overline{ADV}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$ but dependent upon CE2 and $\overline{CE2}$. $\overline{ADSP}$ is ignored if $\overline{CE}$ is HIGH. Power-down state is entered if CE2 is LOW or $\overline{CE2}$ is HIGH.
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst and causes a new external address to be registered. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive.

PIN DESCRIPTIONS (continued)

TQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
87	$\overline{BWE}$	Input	Byte Write Enable: This active LOW input permits byte write operations and must meet the setup and hold times around the rising edge of CLK.
88	$\overline{GW}$	Input	Global Write: This active LOW input allows a full 36-bit WRITE to occur independent of the $\overline{BWE}$ and $\overline{BWn}$ lines and must meet the setup and hold times around the rising edge of CLK.
64	ZZ	Input	Snooze Enable: This active HIGH asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained.
16, 50, 66	NC	-	No Connect: These signals are not internally connected. These signals may be connected to ground to improve package heat dissipation.
38, 39, 42, 43	DNU	-	Do Not Connect: These signals must not be connected.
52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29	DQ1-DQ32	Input/ Output	SRAM Data I/O: Byte 1 is DQ1-DQ8; Byte 2 is DQ9-DQ16; Byte 3 is DQ17-DQ24; Byte 4 is DQ25-DQ32. Input data must meet setup and hold times around the rising edge of CLK.
51, 80, 1, 30	DQP1-DQP4	Input/ Output	Parity Data I/O: Byte 1 Parity is DQP1; Byte 2 Parity is DQP2; Byte 3 Parity is DQP3; Byte 4 Parity is DQP4.
31	MODE	Input	Mode: This input selects the burst sequence. A LOW on this pin selects LINEAR BURST. A NC or HIGH on this pin selects INTERLEAVED BURST. Do not alter input state while device is operating.
4, 11, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91	Vcc	Supply	Power Supply: +3.3V ±5%
5, 10, 14, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	Vss	Supply	Ground: GND

INTERLEAVED BURST ADDRESS TABLE (MODE = NC OR HIGH)

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

LINEAR BURST ADDRESS TABLE (MODE = GND)

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

PARTIAL TRUTH TABLE FOR WRITE COMMANDS

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE Byte 1	H	L	L	H	H	H
WRITE all bytes	H	L	L	L	L	L
WRITE all bytes	L	X	X	X	X	X

NOTE: Using $\overline{BWE}$ and $\overline{BW1}$ through $\overline{BW4}$, any one or more bytes may be written.

TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{\text{CE}}$	$\overline{\text{CE2}}$	CE2	ZZ	$\overline{\text{ADSP}}$	$\overline{\text{ADSC}}$	$\overline{\text{ADV}}$	$\overline{\text{WRITE}}$	$\overline{\text{OE}}$	CLK	DQ
Deselected Cycle, Power-down	None	H	X	X	L	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	L	H	L	X	X	X	L-H	High-Z
SNOOZE MODE, Power-down	None	X	X	X	H	X	X	X	X	X	X	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

NOTE:

1. X means "don't care." H means logic HIGH. L means logic LOW. $\overline{\text{WRITE}}$=L means any one or more byte write enable signals ($\overline{\text{BW1}}$, $\overline{\text{BW2}}$, $\overline{\text{BW3}}$ or $\overline{\text{BW4}}$) and $\overline{\text{BWE}}$ are LOW or $\overline{\text{GW}}$ is LOW. $\overline{\text{WRITE}}$=H means all byte write enable signals are HIGH.
2. $\overline{\text{BW1}}$ enables WRITEs to Byte 1 (DQ1-DQ8, DQP1). $\overline{\text{BW2}}$ enables WRITEs to Byte 2 (DQ9-DQ16, DQP2). $\overline{\text{BW3}}$ enables WRITEs to Byte 3 (DQ17-DQ24, DQP3). $\overline{\text{BW4}}$ enables WRITEs to Byte 4 (DQ25-DQ32, DQP4).
3. All inputs except $\overline{\text{OE}}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a WRITE operation following a READ operation, $\overline{\text{OE}}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. $\overline{\text{ADSP}}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and $\overline{\text{BWE}}$ LOW or $\overline{\text{GW}}$ LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -0.5V to +4.6V
VIN .... -0.5V to Vcc +0.5V
Storage Temperature (plastic) .... -55°C to +150°C
Junction Temperature** .... +150°C
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See technical note TN-05-14 for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$; Vcc = +3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	Vcc +0.3	V	1, 2
Input High (Logic 1) Voltage	For MODE and ZZ	V_{IH}	2.4	Vcc +0.3	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$	IL_I	-1	1	µA	14
Output Leakage Current	Output(s) disabled, $0V \leq V_{OUT} \leq V_{CC}$	IL_O	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1, 11
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1, 11
Supply Voltage		V_{CC}	3.135	3.465	V	1

					MAX						
DESCRIPTION	CONDITIONS	SYM	VER	TYP	-9	-10	-11	-12	-14	UNITS	NOTES
Power Supply Current: Operating	Device selected; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ ^tKC MIN; Vcc = MAX; outputs open	I_{CC}	ALL	200	300	300	300	250	250	mA	3, 12 13
Power Supply Current: Idle	Device selected; Vcc = MAX; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$, $\overline{GW}$, $\overline{BW}$ ≥ V_{IH}; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; cycle time ≥ ^tKC MIN	I_{CC1}	ALL	28	50	50	50	45	45	mA	12, 13
CMOS Standby	Device deselected; Vcc = MAX; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; all inputs static; CLK frequency = 0	I_{SB2}	STD	0.5	5	5	5	5	5	mA	12, 13
			P	0.2	2	2	2	2	2	mA	
TTL Standby	Device deselected; Vcc = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; CLK frequency = 0	I_{SB3}	STD	15	25	25	25	25	25	mA	12, 13
			P	8	18	18	18	18	18	mA	
Clock Running	Device deselected; Vcc = MAX; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; CLK cycle time ≥ ^tKC MIN	I_{SB4}	ALL	30	50	50	50	45	45	mA	12, 13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Control Input Capacitance	T_A = 25°C; f = 1 MHz Vcc = 3.3V	C_I	3	4	pF	4
Input/Output Capacitance (DQ)		C_O	6	8	pF	4
Address and Clock Input Capacitance		C_A	2.5	3	pF	4

THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Thermal resistance - Junction to Ambient	Still Air, Soldered on 4.25 x 1.125 inch 4-layer circuit board	θ_{JA}	20	°C/W	
Thermal resistance - Junction to Case		θ_{JC}	1	°C/W	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = +3.3V ±5%)

DESCRIPTION		-9		-10		-11		-12		-14			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Clock													
Clock cycle time	^{t}KC	15		15		15		20		20		ns	
Clock HIGH time	^{t}KH	4		5		5		6		6		ns	
Clock LOW time	^{t}KL	4		5		5		6		6		ns	
Output Times													
Clock to output valid	^{t}KQ		9		10		11		12		14	ns	
Clock to output invalid	^{t}KQX	3		3		3		3		3		ns	
Clock to output in Low-Z	^{t}KQLZ	4		4		4		5		5		ns	4, 6, 7
Clock to output in High-Z	^{t}KQHZ		5		5		5		6		6	ns	4, 6, 7
$\overline{OE}$ to output valid	^{t}OEQ		5		5		5		6		6	ns	9
$\overline{OE}$ to output in Low-Z	^{t}OELZ	0		0		0		0		0		ns	4, 6, 7
$\overline{OE}$ to output in High-Z	^{t}OEHZ		5		5		5		6		6	ns	4, 6, 7
Setup Times													
Address	^{t}AS	2.5		2.5		2.5		3		3.5		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	^{t}ADSS	2.5		3		3		3		3.5		ns	8, 10
Address Advance ($\overline{ADV}$)	^{t}AAS	2.5		3		3		3		3.5		ns	8, 10
Write Signals ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$, $\overline{BWE}$, $\overline{GW}$)	^{t}WS	2.5		3		3		3		3.5		ns	8, 10
Data-in	^{t}DS	2.5		3		3		3		3.5		ns	8, 10
Chip Enables ($\overline{CE}$, $\overline{CE2}$, CE2)	^{t}CES	2.5		3		3		3		3.5		ns	8, 10
Hold Times													
Address	^{t}AH	0.5		0.5		0.5		0.5		0.8		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	^{t}ADSH	0.5		0.5		0.5		0.5		0.8		ns	8, 10
Address Advance ($\overline{ADV}$)	^{t}AAH	0.5		0.5		0.5		0.5		0.8		ns	8, 10
Write Signals ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$, $\overline{BWE}$, $\overline{GW}$)	^{t}WH	0.5		0.5		0.5		0.5		0.8		ns	8, 10
Data-in	^{t}DH	0.5		0.5		0.5		0.5		0.8		ns	8, 10
Chip Enables ($\overline{CE}$, $\overline{CE2}$, CE2)	^{t}CEH	0.5		0.5		0.5		0.5		0.8		ns	8, 10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	2.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

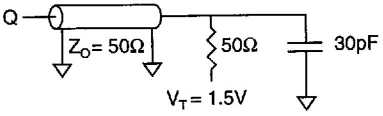


Fig. 1 OUTPUT LOAD
EQUIVALENT

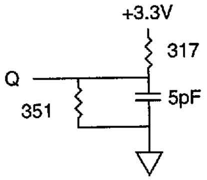


Fig. 2 OUTPUT LOAD
EQUIVALENT

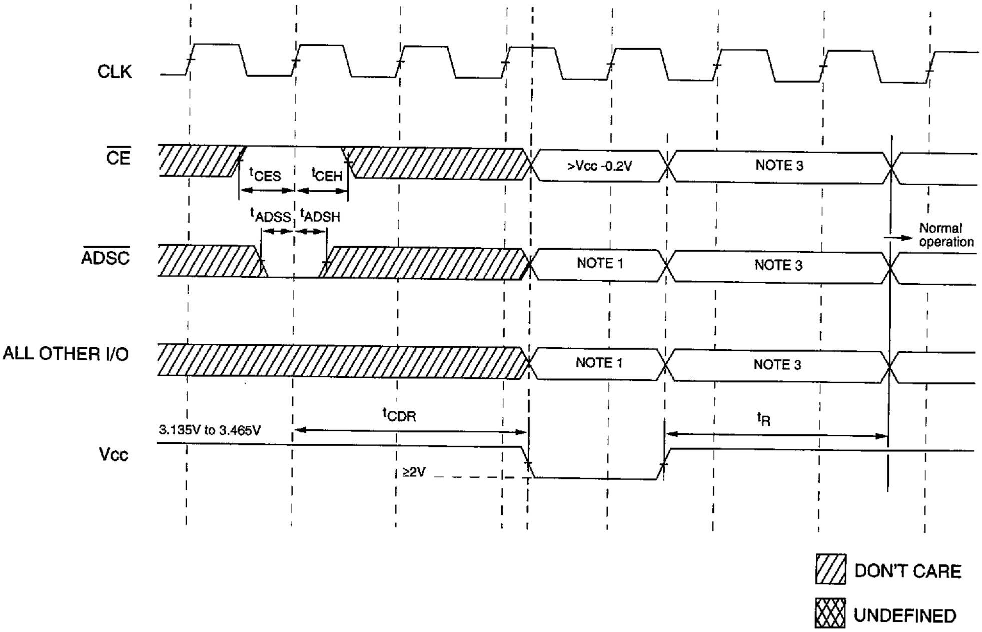
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \le +4.6V$ for $t \le {}^tKC/2$ for $I \le 20mA$.
   Undershoot: $V_{IL} \ge -0.7V$ for $t \le {}^tKC/2$ for $I \le 20mA$.
   Power-up: $V_{IH} \le +3.465V$ and $V_{CC} \le 3.135V$ for $t \le 200ms$.
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with $C_L = 5pF$ as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$ and ${}^tOEHZ$ is less than ${}^tOELZ$.
8. A WRITE cycle is defined by at least one byte write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times. A READ cycle is defined by all byte write enables HIGH and ($\overline{ADSC}$ or $\overline{ADV}$ LOW) or $\overline{ADSP}$ LOW for the required setup and hold times.
9. $\overline{OE}$ is a "don't care" when a byte write enable is sampled LOW.
10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.
11. The load used for V_{OH}, V_{OL} testing is shown in Fig. 2. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
12. "Device Deselected" means device is in POWER-DOWN mode as defined in the Truth Table. "Device Selected" means device is active (not in POWER-DOWN mode).
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
14. MODE pin has an internal pull-up and exhibits an input leakage current of ±10µA.
15. Typical values are measured at 25°C.
16. The device must have a deselect cycle applied at least one clock cycle before data retention mode is entered.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2		V	
Data Retention Current Method 1	$\overline{CE}$, $\overline{CE2} \geq$ (Vcc -0.2V), CE2 $\leq$ 0.2V $V_{IN} \geq$ (Vcc -0.2V) or $\leq$ 0.2V Vcc = 2V	I_{CCDR}		TBD	µA	15
Data Retention Current Method 2	ZZ $\geq$ Vcc -0.2V, Vcc = 2V	I_{CCDR}		TBD	µA	15
Chip Deselect to Data Retention Time		^{t}CDR	^{t}KC		ns	4, 16
Operation Recovery Time		^{t}R		^{t}KC	ns	4

LOW Vcc DATA RETENTION WAVEFORM



NOTE:
1. If ZZ is inactive (ZZ $\leq$ 0.2V), $\overline{CE}$ > Vcc -0.2V and other inputs must be $\geq$ Vcc -0.2V or $\leq$ 0.2V to guarantee I_{CCDR} in data retention mode. If inputs are between these levels or left floating, I_{CCDR} may be exceeded. If ZZ is active (ZZ $\geq$ Vcc -0.2V), then this restriction may be ignored.
2. Only one of the available deselect cycle sequences is shown above ($\overline{CE}$ = HIGH, $\overline{ADSC}$ = LOW). Any of the other deselect cycle sequences may also be used.
3. The device control signals should be in a deselect state between the rising edge of Vcc and until ^{t}R is met.
4. All inputs must be $\leq$ Vcc +0.3V while the device is in data retention mode.

SNOOZE MODE

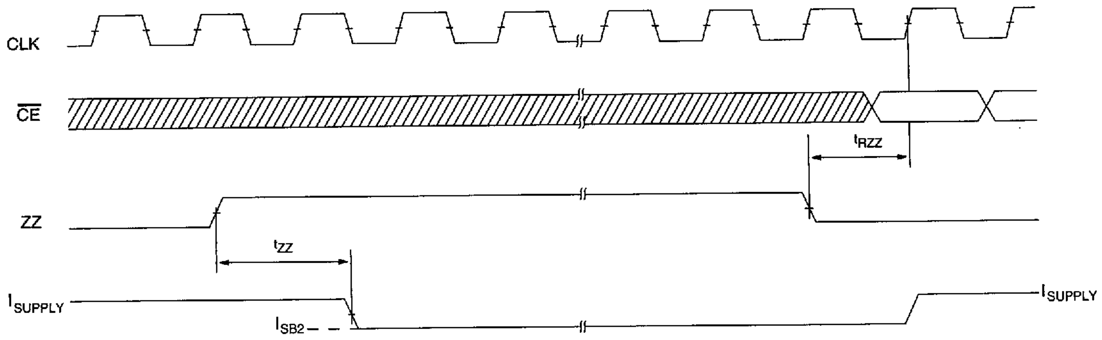
SNOOZE MODE is a low current, "power down" mode in which the device is deselected and current is reduced to I_{SB2}. The duration of SNOOZE MODE is dictated by the length of time the ZZ pin is in a HIGH state. After entering SNOOZE MODE, the clock and all other inputs are ignored.

The ZZ pin (pin 64) is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE. When the ZZ pin becomes a logic HIGH, I_{SB2} is guaranteed after the setup time ^tZZ is met. Any access pending when entering SNOOZE MODE is not guaranteed to successfully complete. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed.

SNOOZE MODE ELECTRICAL CHARACTERISTICS

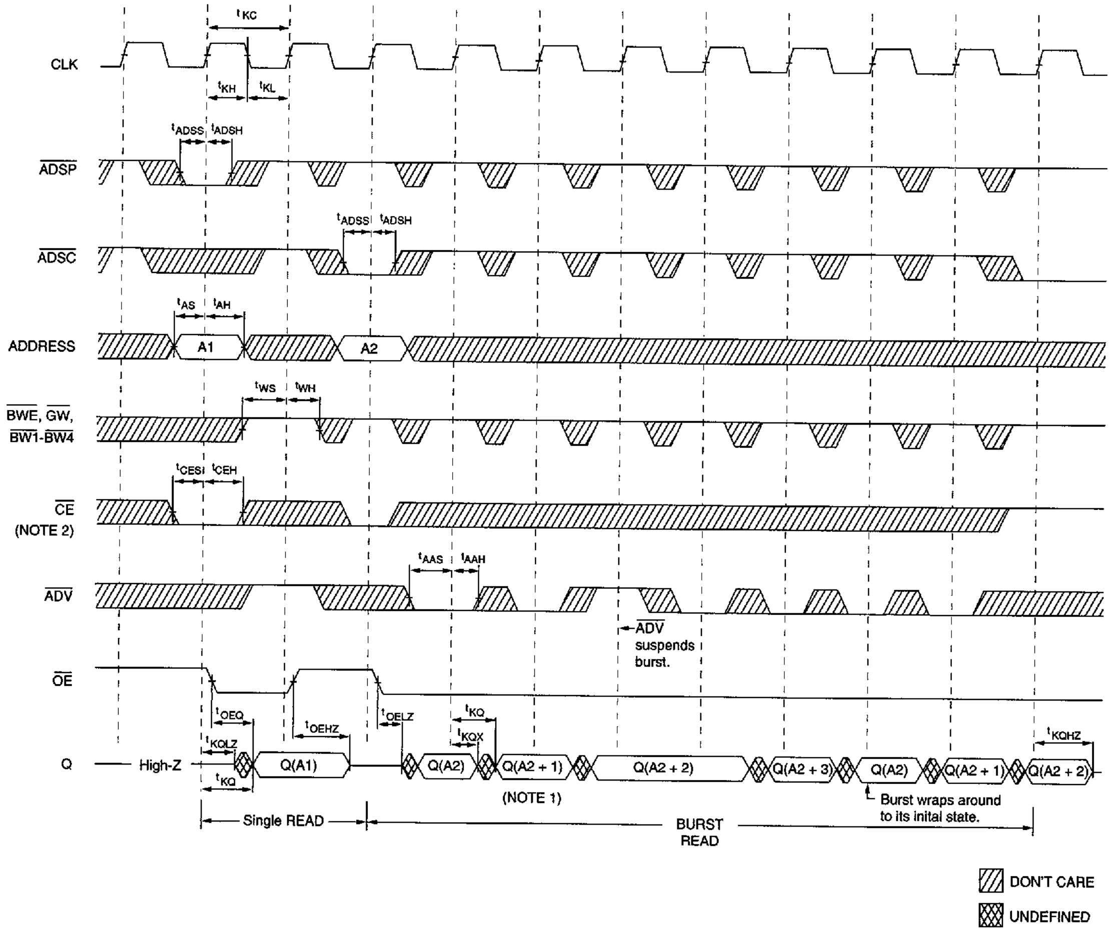
DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Current during SNOOZE MODE	$ZZ \geq V_{IH}$	I_{SB2}		5	mA	
Current during SNOOZE MODE (P Version)	$ZZ \geq V_{IH}$	I_{SB2}		2	mA	
ZZ HIGH to SNOOZE MODE time		^tZZ	^tKC		ns	4
SNOOZE MODE Operation Recovery Time		^tRZZ		^tKC	ns	4

SNOOZE MODE WAVEFORM



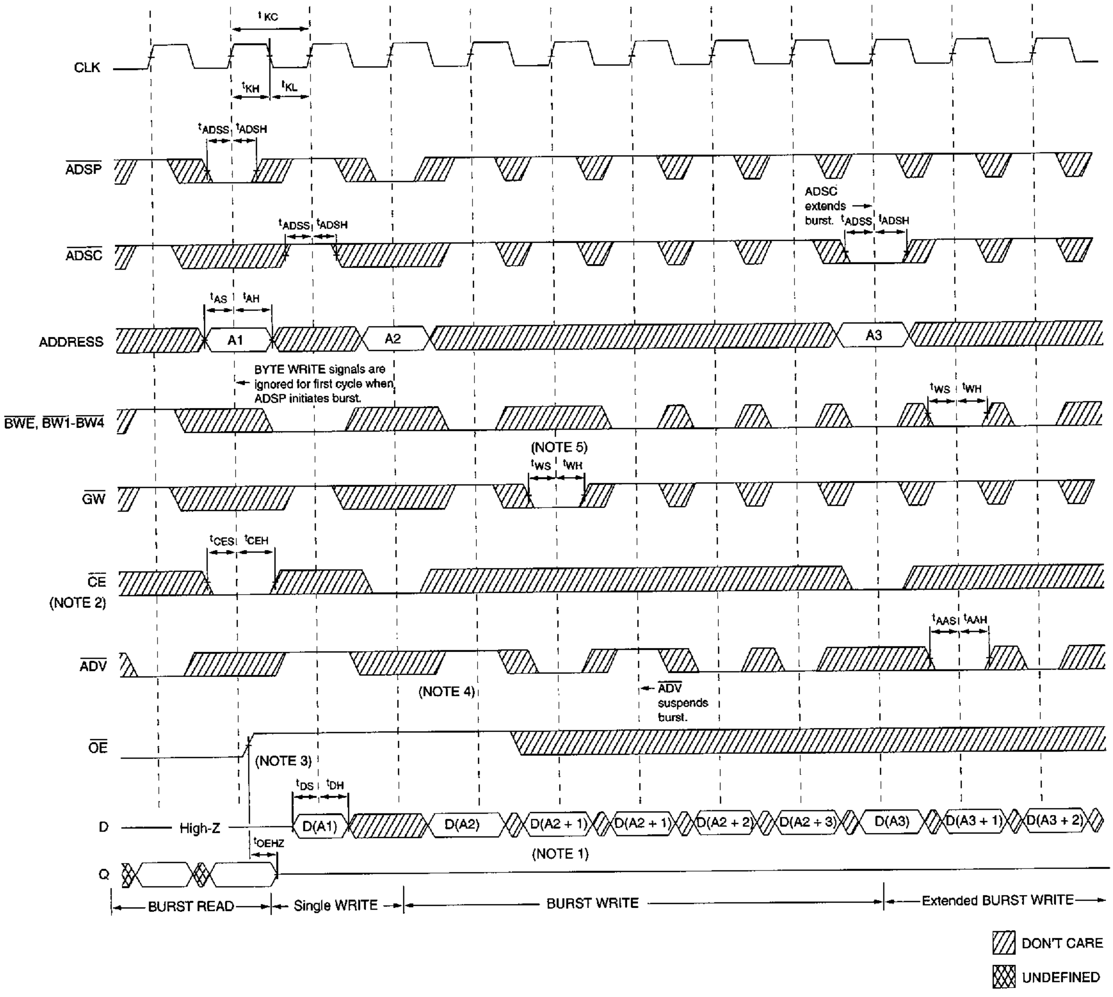
NOTE: 1. The $\overline{CE}$ signal shown above refers to a TRUE state on all chip selects for the device.

READ TIMING



NOTE:
1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. Timing is shown assuming that the device was not enabled before entering into this sequence. $\overline{OE}$ does not cause Q to be driven until after the following clock rising edge.

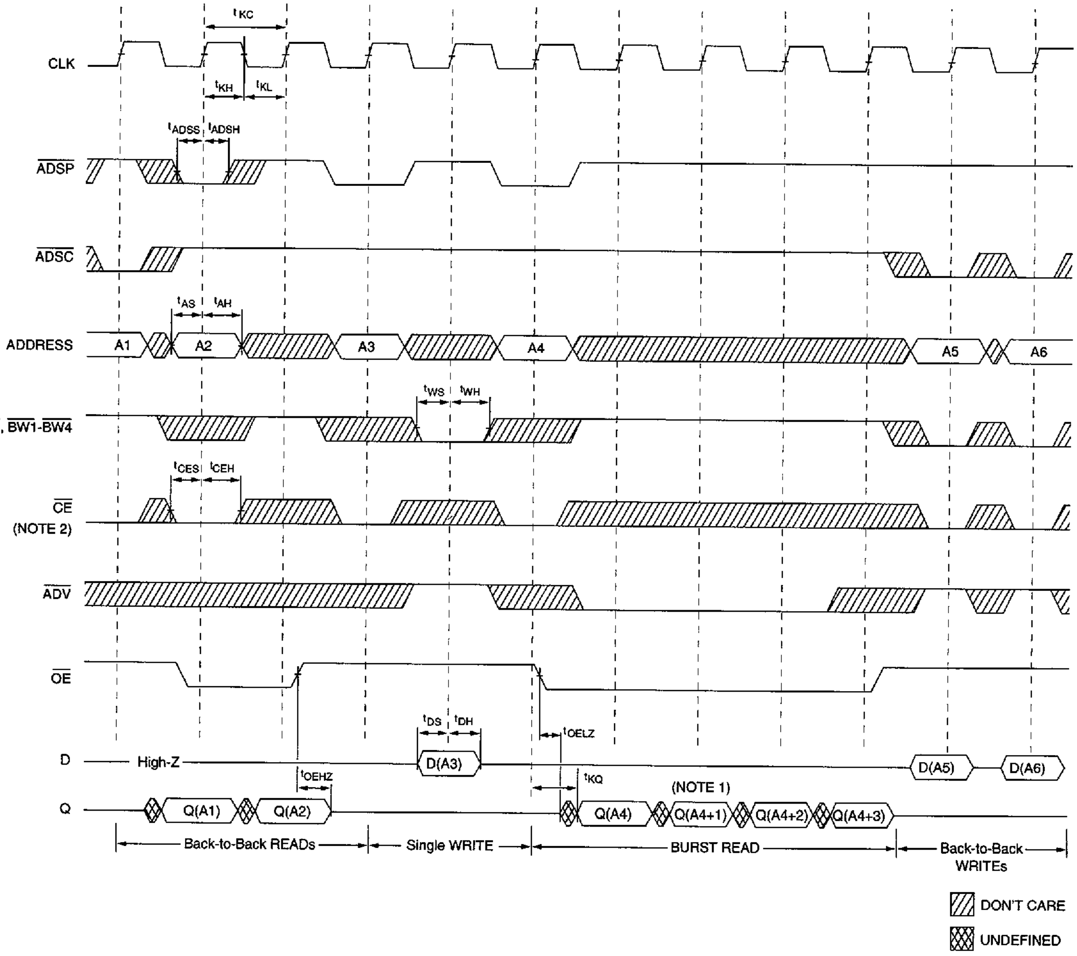
WRITE TIMING



NOTE:

1. D(A2) refers to input for address A2. D(A2+1) refers to input for the next internal burst address following A2.
2. $\overline{\text{CE2}}$ and CE2 have timing identical to $\overline{\text{CE}}$. On this diagram, when $\overline{\text{CE}}$ is LOW, $\overline{\text{CE2}}$ is LOW and CE2 is HIGH. When $\overline{\text{CE}}$ is HIGH, $\overline{\text{CE2}}$ is HIGH and CE2 is LOW.
3. $\overline{\text{OE}}$ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
4. $\overline{\text{ADV}}$ must be HIGH to permit a WRITE to the loaded address.
5. Full width WRITE can be initiated by $\overline{\text{GW}}$ LOW or $\overline{\text{GW}}$ HIGH and $\overline{\text{BWE}}$, $\overline{\text{BW1}}$- $\overline{\text{BW4}}$ LOW.

READ/WRITE TIMING



NOTE:

1. Q(A4) refers to output from address A4. Q(A4+1) refers to output from the next internal burst address following A4.
2. $\overline{\text{CE2}}$ and CE2 have timing identical to $\overline{\text{CE}}$. On this diagram, when $\overline{\text{CE}}$ is LOW, $\overline{\text{CE2}}$ is LOW and CE2 is HIGH. When $\overline{\text{CE}}$ is HIGH, $\overline{\text{CE2}}$ is HIGH and CE2 is LOW.
3. The data bus (Q) remains in High-Z following a WRITE cycle unless an $\overline{\text{ADSP}}$, $\overline{\text{ADSC}}$ or $\overline{\text{ADV}}$ cycle is performed.
4. $\overline{\text{GW}}$ is HIGH.
5. Back-to-back READs may be controlled by either $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$.

APPLICATION INFORMATION

LOAD DERATING CURVES

The Micron 128K x 36 Synchronous SRAM timing is dependent upon the capacitive loading on the outputs. The data sheet is written assuming a load of 30pF. Access time changes with load capacitance as follows:

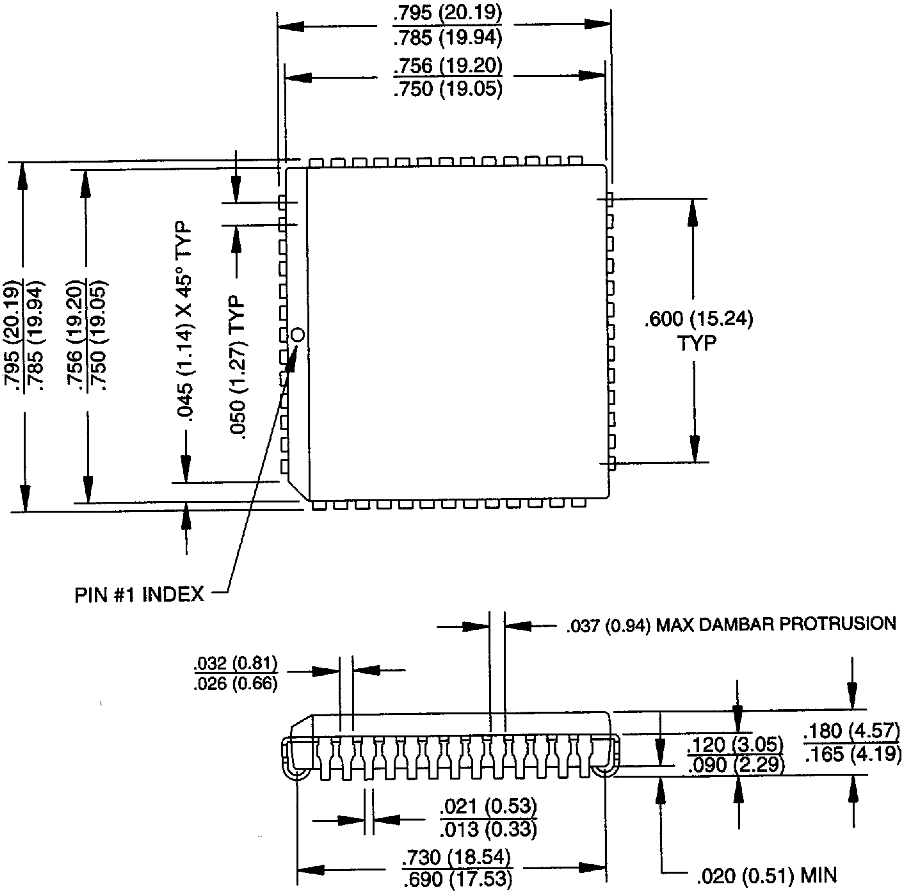
$\Delta {}^{t}KQ = 0.016$ ns/pF x ΔC_L pF.
(Note: this is preliminary information subject to change.)

For example, if the SRAM loading is 22pF, ΔC_L is -8pF (8pF less than rated load). The clock to valid output time of the SRAM is reduced by 0.016 x 8 = 0.128ns. If the device is a 12ns part, the worst case ${}^{t}KQ$ becomes 11.87ns (approximately).

Consult the factory for copies of I/O current versus voltage curves. For capacitive loading derating curves see technical note TN-05-20, "3.3V SRAM Capacitive Loading."

52-PIN PLCC

SA-1

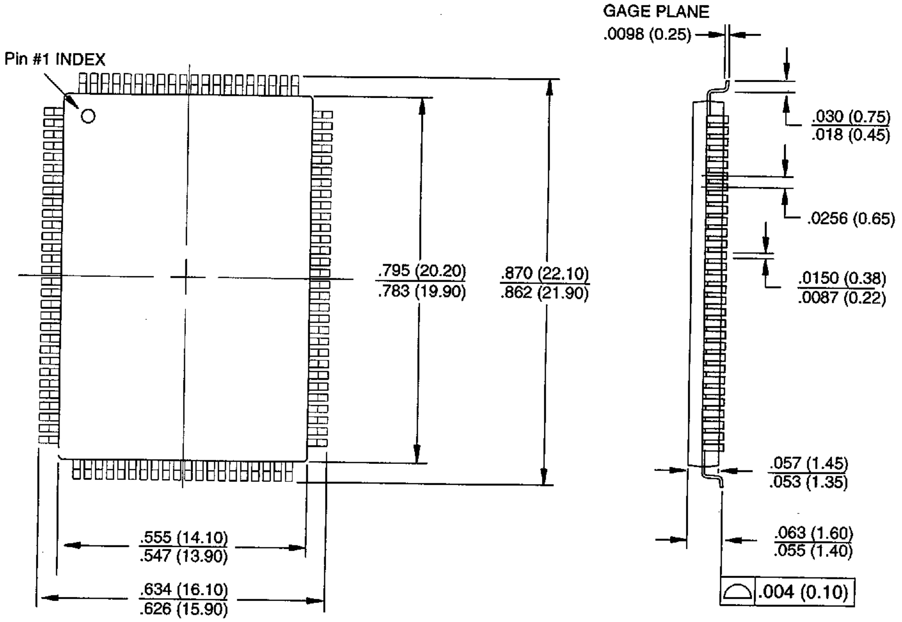


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

100-PIN TQFP

SB-1



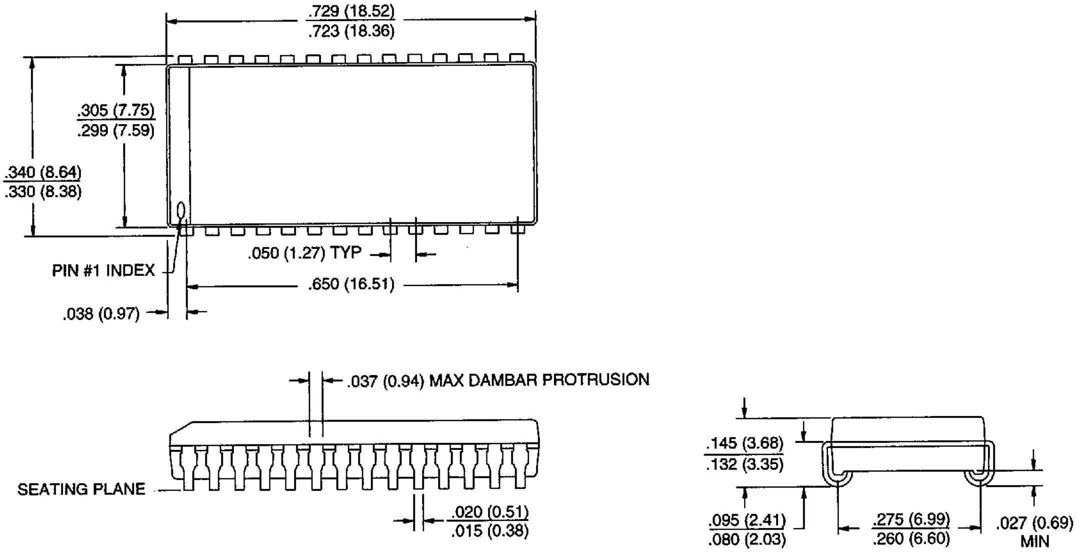
PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

28-PIN PLASTIC SOJ

SC-1

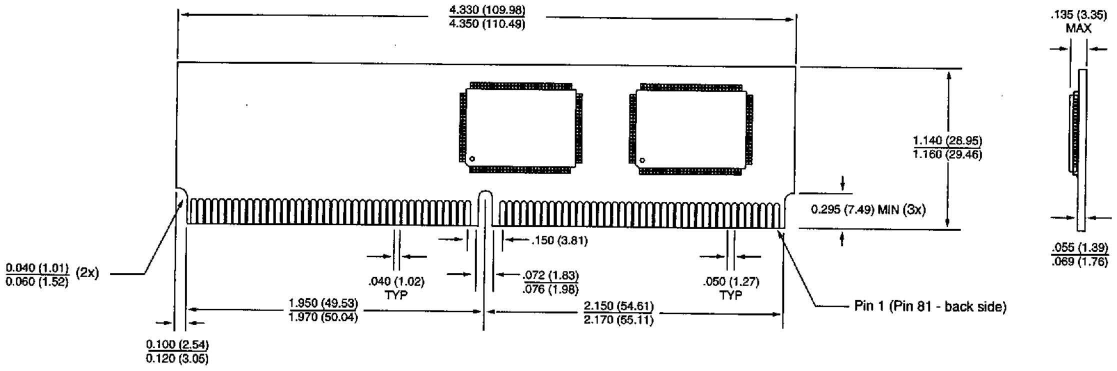


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

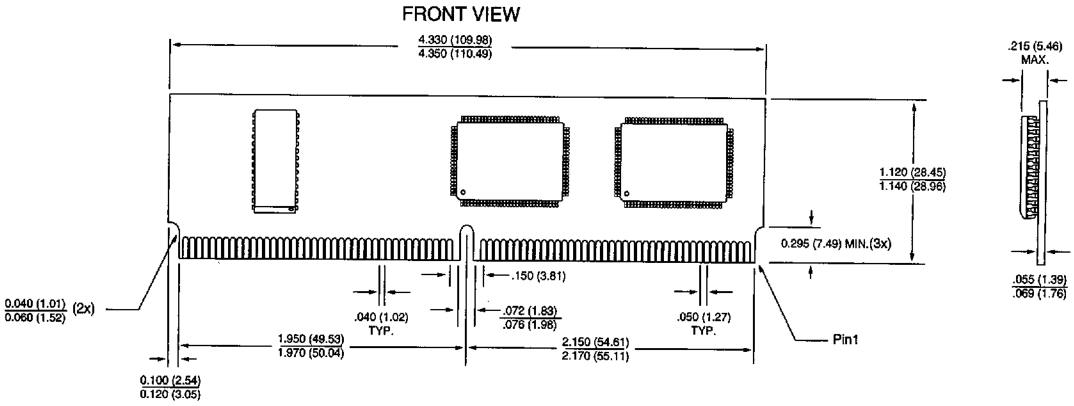
160-PIN MODULE DIMM

SD-1



160-PIN MODULE DIMM

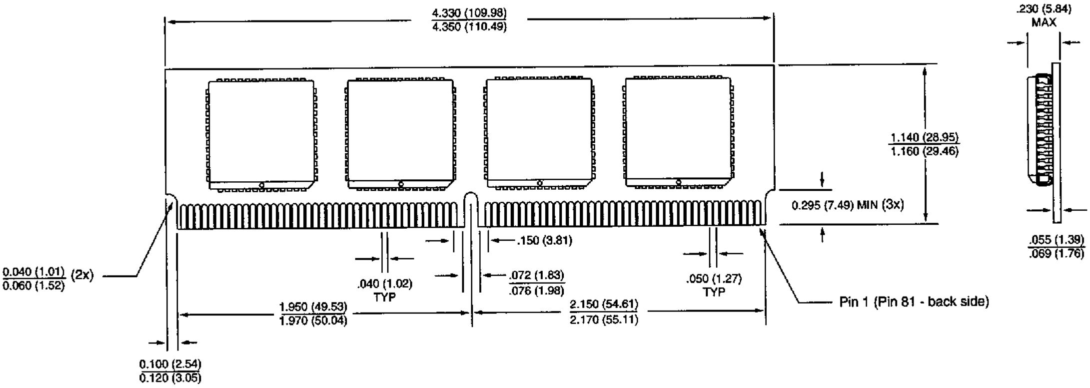
SD-2



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

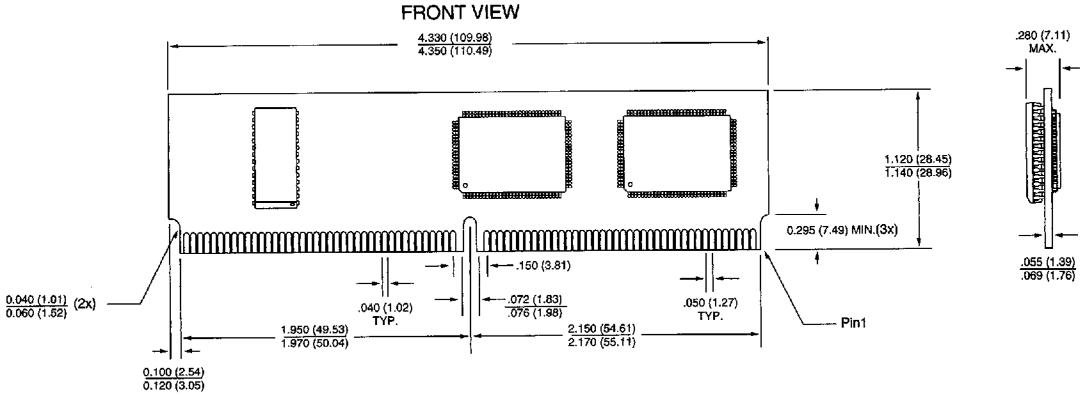
160-PIN MODULE DIMM

SD-3



160-PIN MODULE DIMM

SD-4



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.