PI6C410B-01

Clock Generator for Intel PCI-Express Server Chipset

Features

- 14.318 MHz Crystal Input
- Selectable of 100, 133, 166, 200, 266, 333, and 400MHz CPU Output Frequencies
- SMBus: Power Management Control
- Spread Spectrum support (-0.5% down spread)
- Packaging (Pb-free & Green available):
  - 56-Pin SSOP (V)
  - 56-Pin TSSOP (A)

Output Features

- Four Pairs of Differential CPU Clocks
- Five Pairs of SRC Clocks
- Seven PCI Clocks
- One 48 MHz USB clock
- Two REF clocks

Description

PI6C410B-01 is a high-speed, low-noise clock generator designed to work with Intel Server PCI-Express Chipset. Spread Spectrum PLL based clock generator reduce EMI emission and support a wide range of frequencies.

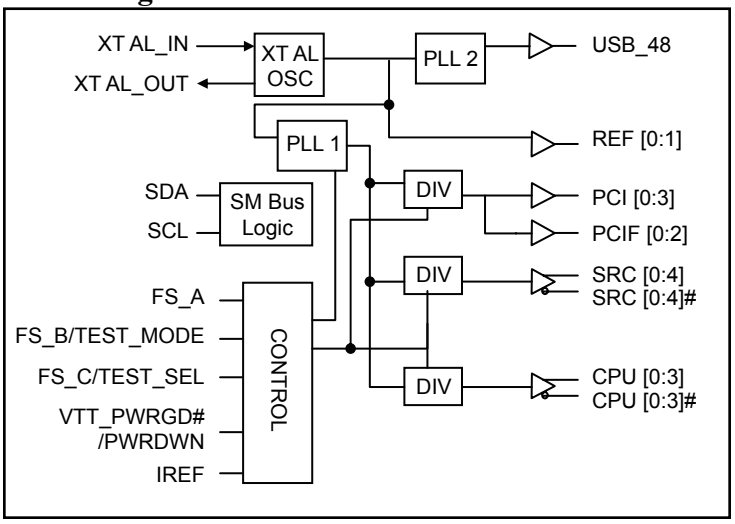
Jitter Performance

- < 85ps Cycle-to-Cycle CPU clock jitter
- < 350ps Cycle-to-Cycle 48 MHz clock jitter
- < 500ps Cycle-to-Cycle PCI clock jitter
- < 125ps Cycle-to-Cycle SRC clock jitter
- < 1000ps Cycle-to-Cycle REF clock jitter

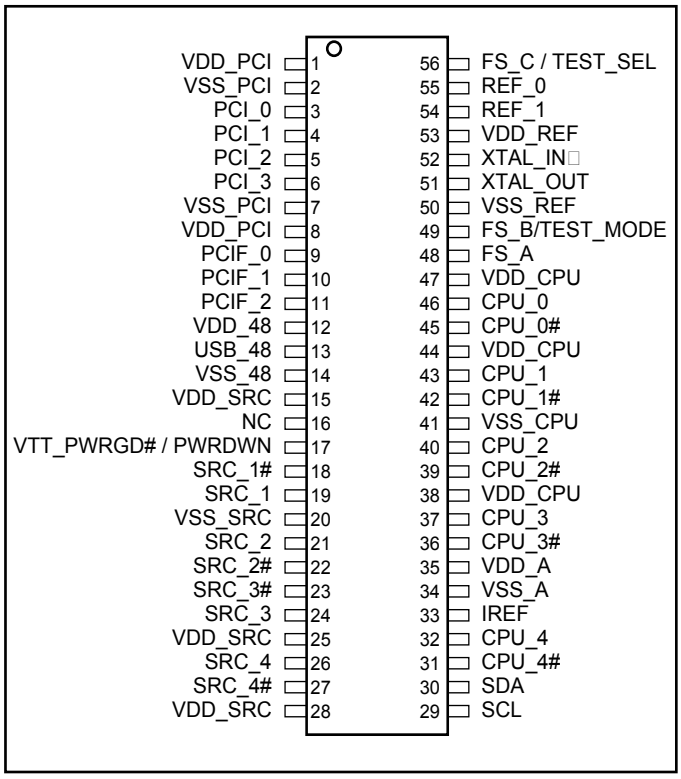
Skew Performance

- < 100ps Output to output CPU clock skew
- < 500ps Output to output PCI clock skew
- < 250ps Output to output SRC clock skew

Block Diagram



Pin Configuration



Pin Descriptions

Pin Name	Type	Pin Number	Description
REF[0:1]	Output	54, 55	3.3V 14.31818 MHz outputs
XTAL_IN	Input	52	14.31818 MHz crystal input
XTAL_OUT	Output	51	14.31818 MHz crystal output
CPU[0:4] & CPU[0:4]#	Output	46,45; 43,42; 40,39; 37,36	Differential CPU outputs
SRC[1:4] & SRC[1:4]#	Output	19,18; 21,22; 24,23; 26,27	Differential Serial Reference Clock outputs
PCIF[0:2]	Output	9, 10, 11	33 MHz clocks outputs (free running)
PCI[0:3]	Output	3, 4, 5, 6	33 MHz clocks outputs
USB_48	Output	13	48 MHz clock output
FS_A	Input	48	3.3V LVTTL inputs for CPU frequency selection
FS_B / TEST_MODE	Input	49	3.3V LVTTL inputs for CPU frequency selection / Test Mode select: 1 = Hi-Z, 0 = Ref/N
FS_C / TEST_SEL	Input	56	3.3V LVTTL inputs for CPU frequency selection / Test Mode select if pulled to 3.3V when Vtt_Pwrgd# is asserted LOW
IREF	Input	33	External resistor connection for internal current reference
VTT_PWRGD# / PWRDWN	Input	31	3.3V LVTTL Level sensitive strobe used to determine to latch the FS_A, FS_B/TEST_MODE, FS_C/TEST_SEL and PCIF0/ ITP_EN inputs (active low) / 3.3V LVTTL active high input for Power Down operation.
SDA	I/O	30	SMBus compatible SDATA
SCL	Input	29	SMBus compatible SCLOCK
V_{DD_PCI}	Power	1, 8	3.3V Power Supply for Outputs
V_{DD_48}	Power	12	3.3V Power Supply for Outputs
V_{DD_SRC}	Power	15, 25, 28	3.3V Power Supply for Outputs
V_{DD_CPU}	Power	38, 44, 47	3.3V Power Supply for Outputs
V_{DD_REF}	Power	53	3.3V Power Supply for Outputs
V_{SS_PCI}	Ground	2, 7	Ground for Outputs
V_{SS_48}	Ground	14	Ground for Outputs
V_{SS_SRC}	Ground	20	Ground for Outputs
V_{SS_CPU}	Ground	41	Ground for Outputs
V_{SS_REF}	Ground	50	Ground for Outputs
V_{DD_A}	Power	35	3.3V Power Supply for PLL
V_{SS_A}	Ground	34	Ground for PLL

Functionality

Frequency Selection

FS_C	FS_B	FS_A	CPU	SRC	PCIF / PCI	REF	USB_48	Note
1	0	1	100MHz	100MHz	33MHz	14.318MHz	48MHz	1
0	0	1	133MHz	100MHz	33MHz	14.318MHz	48MHz	1
0	1	1	166MHz	100MHz	33MHz	14.318MHz	48MHz	1
0	1	0	200MHz	100MHz	33MHz	14.318MHz	48MHz	1
0	0	0	266MHz	100MHz	33MHz	14.318MHz	48MHz	1
1	0	0	333MHz	100MHz	33MHz	14.318MHz	48MHz	1
1	1	0	400MHz	100MHz	33MHz	14.318MHz	48MHz	1
1	1	1	Reserved	100MHz	33MHz	14.318MHz	48MHz	1

Notes:

1. Refer to DC Electrical Characteristics for FS_A, FS_B and FS_C (Vih_FS, Vil_FS) threshold levels

Test Mode Selection

TEST MODE	CPU	SRC	PCIF / PCI	REF	USB 48	Note
1	REF/N	REF/N	REF/N	REF	REF/N	2
0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	2

Notes:

2. Test mode will occur where the SMBus Bit 6 of Byte 6 = 1, or FS_C/TEST_SEL is set to logic high level.

PWRDWN Functionality

PWRDWN	CPU	CPU#	SRC	SRC#	PCIF / PCI	REF	USB 48
0	Normal	Normal	Normal	Normal	33MHz	14.318MHz	48MHz
1	Iref × 2 or Float	Float	Iref × 2 or Float	Float	Low	Low	Low

Serial Data Interface (SMBus)

PI6C410B-01 is a slave only SMBus device that supports indexed block read and indexed block write protocol using a single 7-bit address and read/write bit as shown below.

Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	0/1

Data Protocol

1 bit	7 bits	1	1	8 bits	1	8 bits	1	8 bits	1		8 bits	1	1 bit
Start bit	Slave Addr	R/W	Ack	Register offset	Ack	Byte Count = N	Ack	Data Byte 0	Ack	…	Data Byte N - 1	Ack	Stop bit

Note:
1. Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

Data Byte 0: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin	Source Pin
0	CPU_4 Output Enable 1 = Enabled, 0 = Disabled (Hi-Z)	RW	1 = Enabled	CPU_4, CPU_4#	32, 31	NA
1	SRC_1 Output Enable 1 = Enabled, 0 = Disabled (Hi-Z)	RW	1 = Enabled	SRC_1	19, 18	NA
2	SRC_2 Output Enable 1 = Enabled, 0 = Disabled (Hi-Z)	RW	1 = Enabled	SRC_2	21, 22	NA
3	SRC_3 Output Enable 1 = Enabled, 0 = Disabled (Hi-Z)	RW	1 = Enabled	SRC_3	24, 23	NA
4	SRC_4 Output Enable 1 = Enabled, 0 = Disabled (Hi-Z)	RW	1 = Enabled	SRC_4	26, 27	NA
5	Reserved	RW				
6	Reserved	RW				
7	Reserved	RW				

Data Byte 1: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin	Source Pin
0	Spread Spectrum 1 = On, 0 = Off	RW	0 = Spread off	CPU[0:3], SRC[1:4], PCI[0:3], PCIF[0:2]	3, 4, 5, 6, 9, 10, 11, 18, 19, 21, 22, 23, 24, 26, 27, 31, 32, 36, 37, 39, 40, 42, 43, 45, 46	NA
1	CPU_0 Output Enable 1 = Enabled, 0 = Disabled (Hi-Z)	RW	1 = Enabled	CPU_0, CPU_0#	45, 46	NA
2	CPU_1 Output Enable 1 = Enabled, 0 = Disabled (Hi-Z)	RW	1 = Enabled	CPU_1, CPU_1#	42, 43	NA
3	Reserved	RW				
4	CPU_2 Output Enable 1 = Enabled, 0 = Disabled (Hi-Z)	RW	1 = Enabled	CPU_2, CPU_2#	39, 40	NA
5	CPU_3 Output Enable 1 = Enabled, 0 = Disabled (Hi-Z)	RW	1 = Enabled	CPU_3, CPU_3#	36, 37	NA
6	REF0 Output Enable 1 = Enabled, 0 = Disabled	RW	1 = Enabled	REF_0	55	NA
7	REF1 Output Enable 1 = Enabled, 0 = Disabled	RW	1 = Enabled	REF_1	54	NA

Data Byte 2: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin	Source Pin
0	USB_48 Output Enable 1 = Enabled, 0 = Disabled	RW	1 = Enabled	USB_48	13	NA
1	PCIF_0 Output Enable 1 = Enabled, 0 = Disabled	RW	1 = Enabled	PCIF_0	9	NA
2	PCIF_1 Output Enable 1 = Enabled, 0 = Disabled	RW	1 = Enabled	PCIF_1	10	NA
3	PCIF_2 Output Enable 1 = Enabled, 0 = Disabled	RW	1 = Enabled	PCIF_2	11	NA
4	PCI_0 Output Enable 1 = Enabled, 0 = Disabled	RW	1 = Enabled	PCI_0	3	NA
5	PCI_1 Output Enable 1 = Enabled, 0 = Disabled	RW	1 = Enabled	PCI_1	4	NA
6	PCI _2 Output Enable 1 = Enabled, 0 = Disabled	RW	1 = Enabled	PCI_2	5	NA
7	PCI _3 Output Enable 1 = Enabled, 0 = Disabled	RW	1 = Enabled	PCI_3	6	NA

Data Byte 3: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin	Source Pin
0	CPU_4 Output Control 0 = Free Running 1 = Stopped with CPU_STOP#	RW	Stopped with 1 = CPU_STOP# Assertion	CPU_4, CPU_4#	32, 31	NA
1	SRC_1 Output Control 0 = Free Running 1 = Stopped with PCI_STOP#	RW	0 = Free running	SRC_1, SRC_1#	18, 19	NA
2	SRC_2 Output Control 0 = Free Running 1 = Stopped with PCI_STOP#	RW	0 = Free running	SRC_2, SRC_2#	21, 22	NA
3	SRC_3 Output Control 0 = Free Running 1 = Stopped with PCI_STOP#	RW	0 = Free running	SRC_3, SRC_3#	23, 24	NA
4	SRC_4 Output Control 0 = Free Running 1 = Stopped with PCI_STOP#	RW	0 = Free running	SRC_4, SRC_4#	26, 27	NA
5	PCIF0 Output Control 0 = Free Running 1 = Stopped with PCI_STOP#	RW	0 = Free running	PCIF_0	9	NA
6	PCIF1 Output Control 0 = Free Running 1 = Stopped with PCI_STOP#	RW	0 = Free running	PCIF_1	10	NA
7	PCIF2 Output Control 0 = Free Running 1 = Stopped with PCI_STOP#	RW	0 = Free running	PCIF_2	11	NA

Data Byte 4: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin	Source Pin
0	CPU_0 Output Control 0 = Free Running 1 = Stopped with CPU_STOP#	RW	1 = Stopped with CPU_STOP# assertion	CPU_0, CPU0#	45, 46	NA
1	CPU_1 Output Control 0 = Free Running 1 = Stopped with CPU_STOP#	RW	1 = Stopped with CPU_STOP# assertion	CPU_1, CPU1#	42, 43	NA
2	CPU_2 Output Control 0 = Free Running 1 = Stopped with CPU_STOP#	RW	1 = Stopped with CPU_STOP# assertion	CPU_2, CPU2#	39, 40	NA
3	CPU_3 Output Control 0 = Free Running 1 = Stopped with CPU_STOP#	RW	1 = Stopped with CPU_STOP# assertion	CPU_3, CPU3#	36, 37	NA
4	CPU_0 Pwrdwn drive mode 1 = Hi-Z, 0 = Driven in Pwrdwn	RW	0 = Driven in power down	CPU_0, CPU0#	45, 46	NA
5	CPU_1 Pwrdwn drive mode 1 = Hi-Z, 0 = Driven in Pwrdwn	RW	0 = Driven in power down	CPU_1, CPU1#	42, 43	NA
6	CPU_2 Pwrdwn drive mode 1 = Hi-Z, 0 = Driven in Pwrdwn	RW	0 = Driven in power down	CPU_2, CPU2#	39, 40	NA
7	CPU_3 Pwrdwn drive mode 1 = Hi-Z, 0 = Driven in Pwrdwn	RW	0 = Driven in power down	CPU_3, CPU3#	36, 37	NA

Data Byte 5: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin	Source Pin
0	CPU_0 CPU_Stop drive mode 1 = Hi-Z, 0 = Driven in CPU Stop	RW	0 = Driven in CPU_Stop	CPU_0, CPU0#	45, 46	NA
1	CPU_1 CPU_Stop drive mode 1 = Hi-Z, 0 = Driven in CPU Stop	RW	0 = Driven in CPU_Stop	CPU_1, CPU1#	42, 43	NA
2	CPU_2 CPU_Stop drive mode 1 = Hi-Z, 0 = Driven in CPU Stop	RW	0 = Driven in CPU_Stop	CPU_2, CPU2#	39, 40	NA
3	CPU_3 CPU_Stop drive mode 1 = Hi-Z, 0 = Driven in CPU Stop	RW	0 = Driven in CPU_Stop	CPU_3, CPU3#	36, 37	NA
4	CPU_4 CPU_Stop drive mode 1 = Hi-Z, 0 = Driven in CPU Stop	RW	0 = Driven in CPU_Stop	CPU_4, CPU4#	32, 31	
5	SRC_Pwrdwn drive mode 1 = Hi-Z, 0 = Driven in Pwrdwn	RW	0 = Driven in power down	SRC[0:4] & SRC[0:4]#	16, 17, 18, 19, 21, 22, 23, 24, 26, 27	NA
6	SRC_Stop drive mode 1 = Hi-Z, 0 = Driven in PCI_STOP	RW	0 = Driven in PCI_STOP	SRC[0:4] & SRC[0:4]#	16, 17, 18, 19, 21, 22, 23, 24, 26, 27	NA
7	CPU_4 Pwrdwn drive mode 1 = Hi-Z, 0 = Driven in CPU Stop	RW	0 = Driven in Pwrdwn	CPU_4, CPU4#	32, 31	NA

Data Byte 6: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin	Source Pin
0	FS_A Reflects the value of the FS_A pin sampled on power up 0 = FS_A was low during Vtt_Pwrgd# assertion	R	Externally Selected	CPU[0:3]	36, 37, 39, 40, 42, 43, 45, 46	NA
1	FS_B Reflects the value of the FS_B pin sampled on power up 0 = FS_B was low during Vtt_Pwrgd# assertion	R	Externally Selected	CPU[0:3]	36, 37, 39, 40, 42, 43, 45, 46	NA
2	FS_C Reflects the value of the FS_C pin sampled on power up 0 = FS_C was low during Vtt_Pwrgd# assertion	R	Externally Selected	CPU[0:3]	36, 37, 39, 40, 42, 43, 45, 46	NA
3	PCI_Stop Output Control 0 = Enabled, all stoppable PCI and SRC clocks are stopped, 1 = Disabled	RW	1 = Disabled	All PCI & SRC clocks except PCIF and SRC clocks set to free-running	3, 4, 5, 6, 18, 19, 21, 22, 23, 24, 26, 27	NA
4	REF Output Drive Strength 0 = 1X, 1 = 2X	RW	1 = 2X	REF_0, REF_1	54, 55	NA
5	CPU_Stop# Control 0 = Stop non-free running PC and SRC clocks, 1 = Run	RW	Run			NA
6	Test Clock Mode Entry Control 0 = Normal, 1 = REF/N or Hi-Z	RW	0 = Disabled			
7	Test Clock Mode 0 = Hi-Z, 1 = REF/N	RW	0 = Hi-Z			NA

Data Byte 7: Pericom ID Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin
0	Vendor ID	R	0	NA	NA
1		R	0	NA	NA
2		R	0	NA	NA
3		R	0	NA	NA
4	Revision Code	R	0	NA	NA
5		R	0	NA	NA
6		R	0	NA	NA
7		R	0	NA	NA

Data Byte 8: Block Read Byte Count

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin
0	Block Read Byte Count	R	0	NA	NA
1	Block Read Byte Count	R	1	NA	NA
2	Block Read Byte Count	R	1	NA	NA
3	Block Read Byte Count	R	1	NA	NA
4	Block Read Byte Count	R	0	NA	NA
5	Block Read Byte Count	R	0	NA	NA
6	Block Read Byte Count	R	0	NA	NA
7	Block Read Byte Count	R	0	NA	NA

Power Down (PWRDWN assertion)

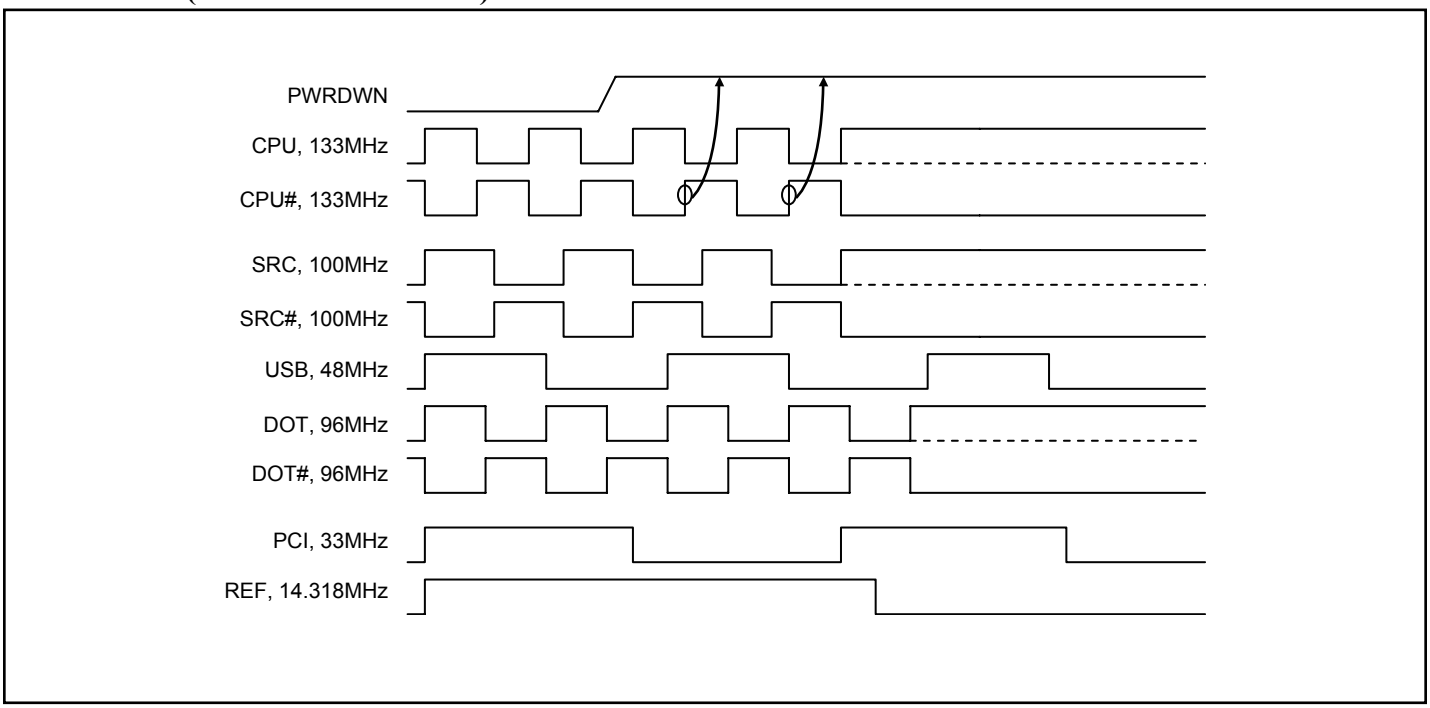


Figure 1. Power down sequence

Power Down (PWRDWN De-assertion)

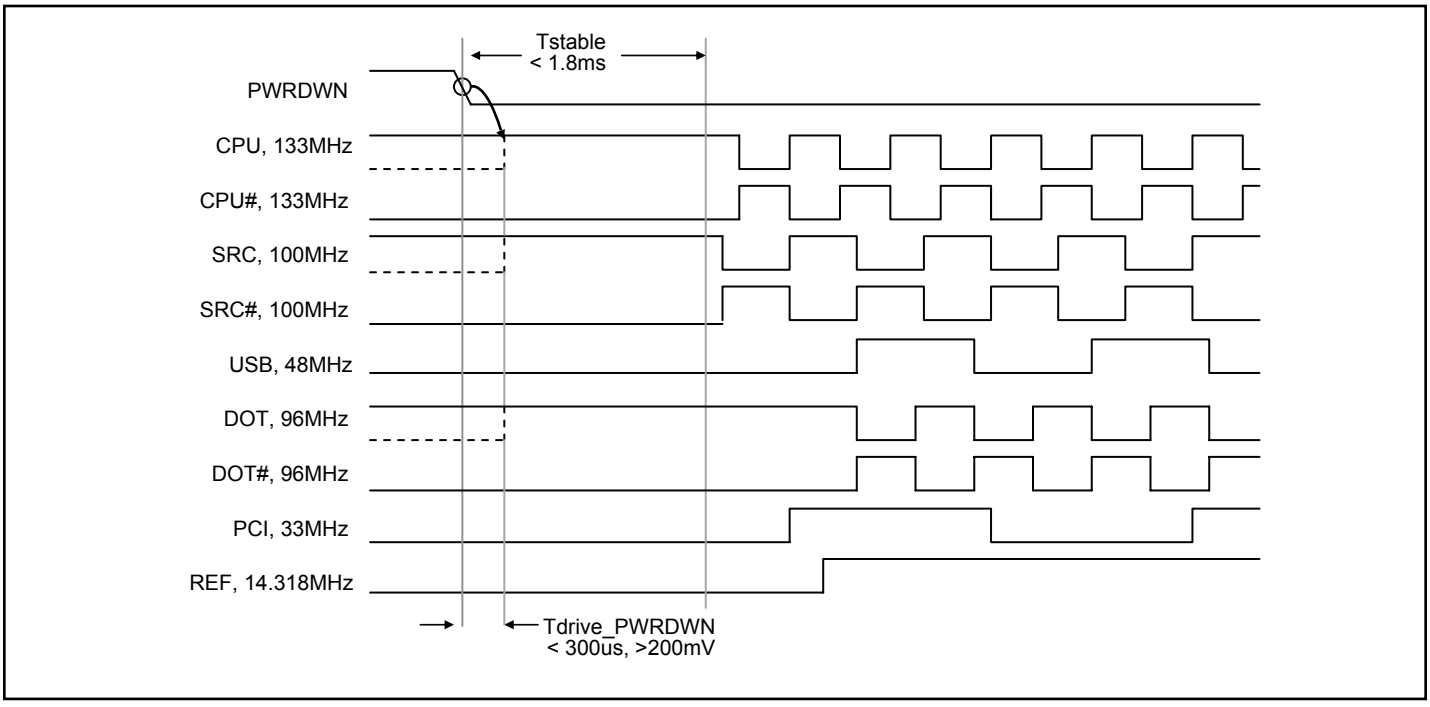


Figure 2. Power down de-assert sequence

Tristate Specifications

CPU & SRC Tristate clock truth table

Signal	Pwrdwn pin	Pwrdwn Tristate Bit	Stoppable Outputs	Non-stop Outputs
CPU[0:3], SRC[0:4],	0	X	Running	Running
	1	0	Driven @ Iref x 2	Driven @ Iref x 2
	1	1	Tristate	Tristate

Spread Spectrum Specifications

PI6C410B supports Spread Spectrum clocking and can be enabled and disabled via SMBus control. The maximum Spread Spectrum Modulation is –0.5% down spread with frequency from 30KHz to 33K Hz.

SSC ON	Tperiod		SSC OFF	Tperiod		Unit
	Min	Max		Min	Max	
CPU @ 399.000MHz	2.4993	2.5133	CPU @ 400.000MHz	2.4993	2.5008	ns
CPU @ 332.500MHz	2.9991	3.0160	CPU @ 333.333MHz	2.9991	3.0009	
CPU @ 266.000MHz	3.7489	3.7700	CPU @ 266.666MHz	3.7489	3.7511	
CPU @ 199.500MHz	4.9985	5.0266	CPU @ 200.000MHz	4.9985	5.0015	
CPU @ 166.250MHz	5.9982	6.0320	CPU @ 166.666MHz	5.9982	6.0018	
CPU @ 133.000MHz	7.4978	7.5400	CPU @ 133.333MHz	7.4978	7.5023	
CPU @ 99.750MHz	9.9970	10.0533	CPU @ 100.000MHz	9.9970	10.0030	
SRC @ 99.750MHz	9.9970	10.0533	SRC @ 100.000MHz	9.9970	10.0030	
PCIF / PCI @ 33.250MHz	29.9910	30.1598	PCIF / PCI @ 33.333MHz	29.9910	30.0090	

Crystal Recommendations

Frequency	Cut	Loading	Load Cap	Drive Max.	Shunt Cap Max.	Motional Cap Max.	Tolerance Max.	Stability Max.	Aging Max.
14.31818MHz	AT	Parallel	20pF	0.1mW	5pF	0.016pF	50ppm	50ppm	5ppm

Notes:

1. External trim capacitors (Ce) are required by using this formula $Ce = 2*C_L – (Cs + Ci)$. Typical Ce = 33pF when Crystal Load = 20pF, Trace capacitance (Cs) = 2.8pF and XTAL pins capacitance = 4.5pF.

Current-mode output buffer characteristics of CPU and SRC

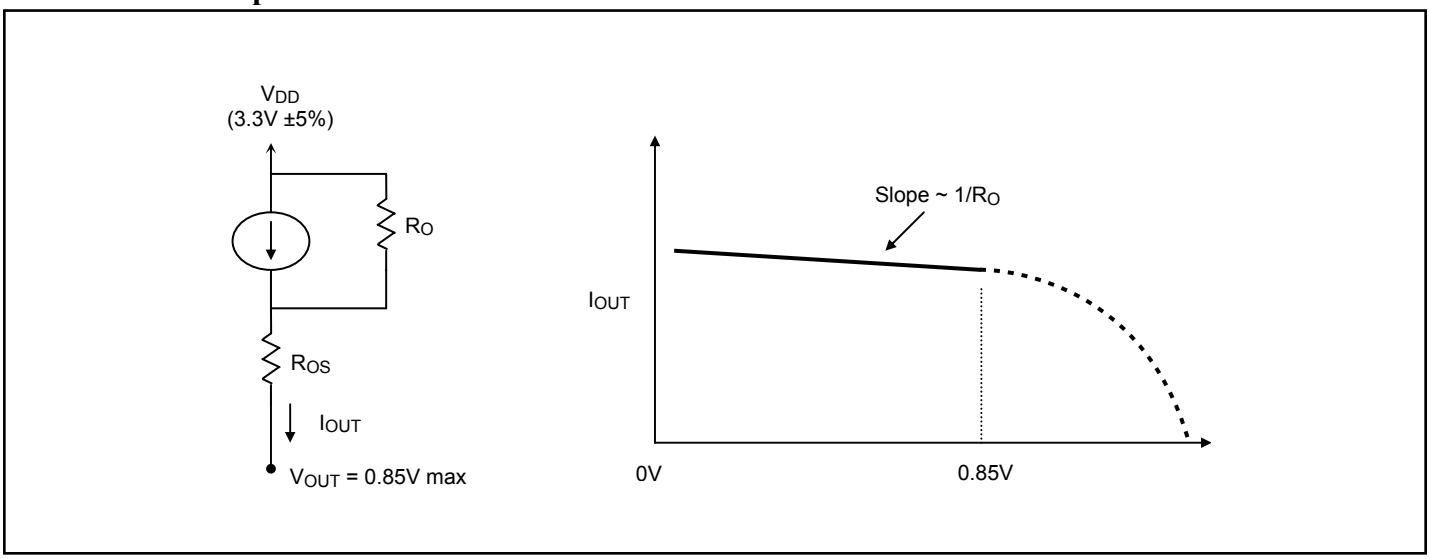


Figure 3. Simplified diagram of current-mode output buffer

Host Clock Buffer characteristics

Symbol	Minimum	Maximum
R_O	3000Ω	N/A
R_{OS}	unspecified	unspecified
V_{OUT}	N/A	850mV

Current Accuracy

Symbol	Conditions	Configuration	Load	Min.	Max.
I_{OUT}	V_{DD} = 3.30 ±5%	R_{REF} = 475Ω 1% I_{REF} = 2.32mA	Nominal test load for given configuration	-12% $I_{NOMINAL}$	+12% $I_{NOMINAL}$

Note:
1. $I_{NOMINAL}$ refers to the expected current based on the configuration of the device.

Host Clock Output Current

Board Target Trace/Term Z	Reference R, $I_{REF} = V_{DD}/(3xRr)$	Output Current	V_{OH} @ Z
100Ω (100Ω differential ≈ 8% coupling ratio)	R_{REF} = 475Ω 1%, I_{REF} = 2.32mA	I_{OH} = 6 x I_{REF}	0.7V @ 50

Absolute Maximum Ratings (Over operating free-air temperature range)

Symbol	Parameters	Min.	Max.	Units
V_{DD_A}	3.3V Core Supply Voltage	-0.5	4.6	V
V_{DD}	3.3V I/O Supply Voltage	-0.5	4.6	
V_{IH}	Input High Voltage		4.6	
V_{IL}	Input Low Voltage	-0.5		
Ts	Storage Temperature	-65	150	°C
V_{ESD}	ESD Protection	2000		V

Note:
1. Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

DC Electrical Characteristics (V_{DD} = 3.3±5%, V_{DD_A} = 3.3±5%)

Symbol	Parameters	Condition		Min.	Max.	Units
V_{DD_A}	3.3V Core Supply Voltage			3.135	3.465	V
V_{DD}	3.3V I/O Supply Voltage			3.135	3.465	
V_{IH}	3.3V Input High Voltage	V_{DD}		2.0	V_{DD} + 0.3	
V_{IL}	3.3V Input Low Voltage			V_{SS} – 0.3	0.8	
I_{IK}	Input Leakage Current	0 < V_{IN} < V_{DD}		-5	+5	µA
V_{IH_FS}	3.3V Input High Voltage			0.7	V_{DD} + 0.3	V
V_{IL_FS}	3.3V Input Low Voltage			V_{SS} – 0.3	0.35	V
V_{OH}	3.3V Output High Voltage	I_{OH} = -1mA		2.4		V
V_{OL}	3.3V Output Low Voltage	I_{OL} = 1mA			0.4	V
I_{OH}	Output High Current	CPU, SRC: I_{OH} = 6 x Iref, Iref = 2.32mA		12.2		mA
					15.6	
		USB	V_{OH} = 1.0V	-29		
			V_{OH} = 3.135V		-23	
		REF, PCI	V_{OH} = 1.0V	-33		
			V_{OH} = 3.135V		-33	
I_{OL}	Output Low Current	USB	V_{OL} = 1.95V	29		
			V_{OL} = 0.4V		27	
		REF, PCI	V_{OL} = 1.95V	30		
			V_{OL} = 0.4V		38	
Cin	Input Pin Capacitance			3	5	pF
Cxtal	Xtal Pin Capacitance			3	5	
Cout	Output Pin Capacitance				6	
Lpin	Pin Inductance				7	nH
I_{DD}	Power Supply Current	V_{DD} = 3.465V, F_{CPU} = 400MHz			500	mA
I_{SS}	Power Down Current	Driven outputs			70	
I_{SS}	Power Down Current	Tristate outputs			12	
Ta	Ambient Temperature			0	70	°C

AC Switching Characteristics (V_{DD} = 3.3±5%, V_{DD_A} = 3.3±5%)

Symbol	Outputs	Parameters	Min	Max.	Units	Notes
T_{rise} / T_{fall}	CPU, SRC	Rise and Fall Time (measured between 0.175V to 0.525V)	175	700	ps	3, 4
T_{rise} / T_{fall}	PCI/PCIF, REF	Rise and Fall Time (measured between 0.4V to 2.4V)	0.5	2.0	ns	6
T_{rise} / T_{fall}	USB	Rise and Fall Time (measured between 0.4V to 2.4V)	1.0	2.0		7
ΔT_{rise} / ΔT_{fall}	CPU, SRC	Rise and Fall Time Variation		125	ps	3, 4
	CPU, SRC	Rise/Fall Matching		20	%	3, 4
T_{skew}	CPU	CPU – CPU Skew		100	ps	3, 5
T_{skew}	SRC	SRC – SRC Skew		250		3, 5
T_{skew}	PCI/PCIF, REF	PCI – PCI Skew / REF - REF Skew (measured at 1.5V)		500		6
T_{jitter}	CPU	Cycle – Cycle Jitter		85		3, 5
T_{jitter}	SRC	Cycle – Cycle Jitter		125		3, 5
T_{jitter}	PCI/PCIF	Cycle – Cycle Jitter (measured at 1.5V)		500		6
T_{jitter}	USB	Cycle – Cycle Jitter (measured at 1.5V)		350		7
T_{jitter}	REF	Cycle – Cycle Jitter (measured at 1.5V)		1000		6
V_{HIGH}	CPU, SRC	Voltage High including overshoot	660	1150	mV	3, 4
V_{LOW}	CPU, SRC	Voltage Low including undershoot	-300			3, 4
V_{CROSS}	CPU, SRC	Absolute crossing poing voltages	250	550		3, 4
ΔV_{CROSS}	CPU, SRC	Total Variation of Vcross over all edges		140		3, 4
T_{DC}	CPU, SRC	Duty Cycle	45	55	%	3, 5
T_{DC}	REF, USB, PCI/PCIF	Duty Cycle (measured at 1.5V)	45	55		6, 7
T_{stable}		All clock stabilization from power-up		<1.8	ms	Fig 2
T_{drive} Pwrdwn		Differential output enable after PwrDwn de-assertion		300	µs	Fig 2
T_{rise} / T_{fall} Pwrdwn		PwrDwn rise and fall time		5.0	ns	

Notes:

3. Test configuration is Rs = 33.2Ω, Rp = 49.9Ω, and 2pF.
4. Measurement taken from Single Ended waveform.
5. Measurement taken from Differential waveform.
6. PCI, PCIF, and REF outputs minimum loading = 10pF, Maximum loading = 30pF.
7. USB output minimum loading = 10pF, Maximum loading = 20pF.

Configuration test load board termination

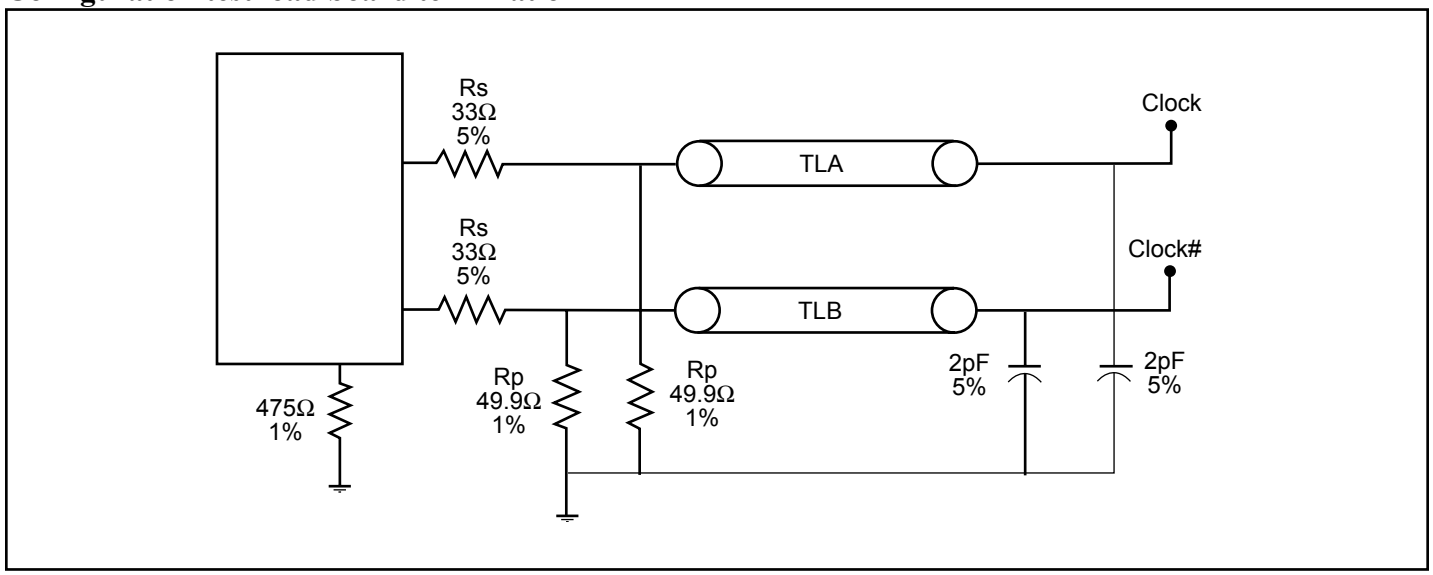
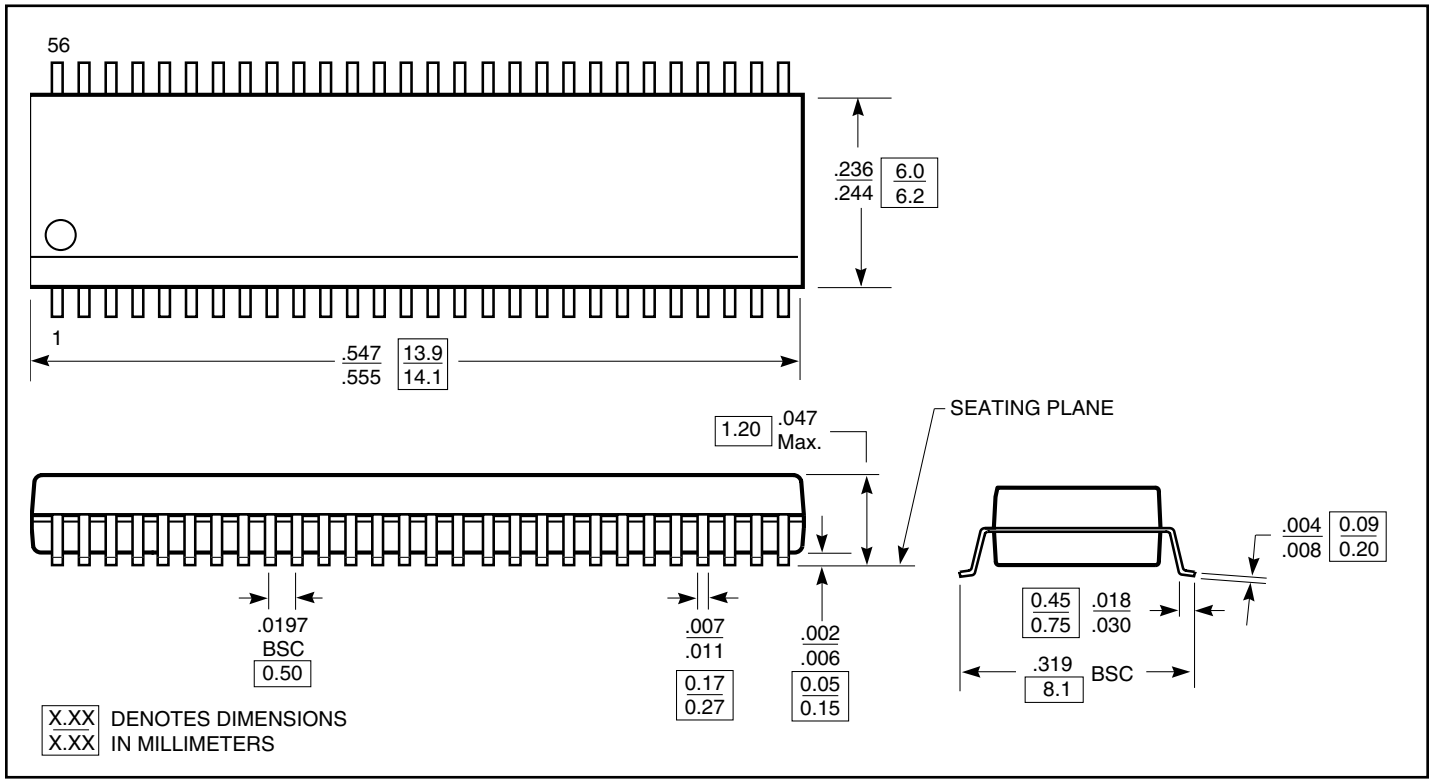


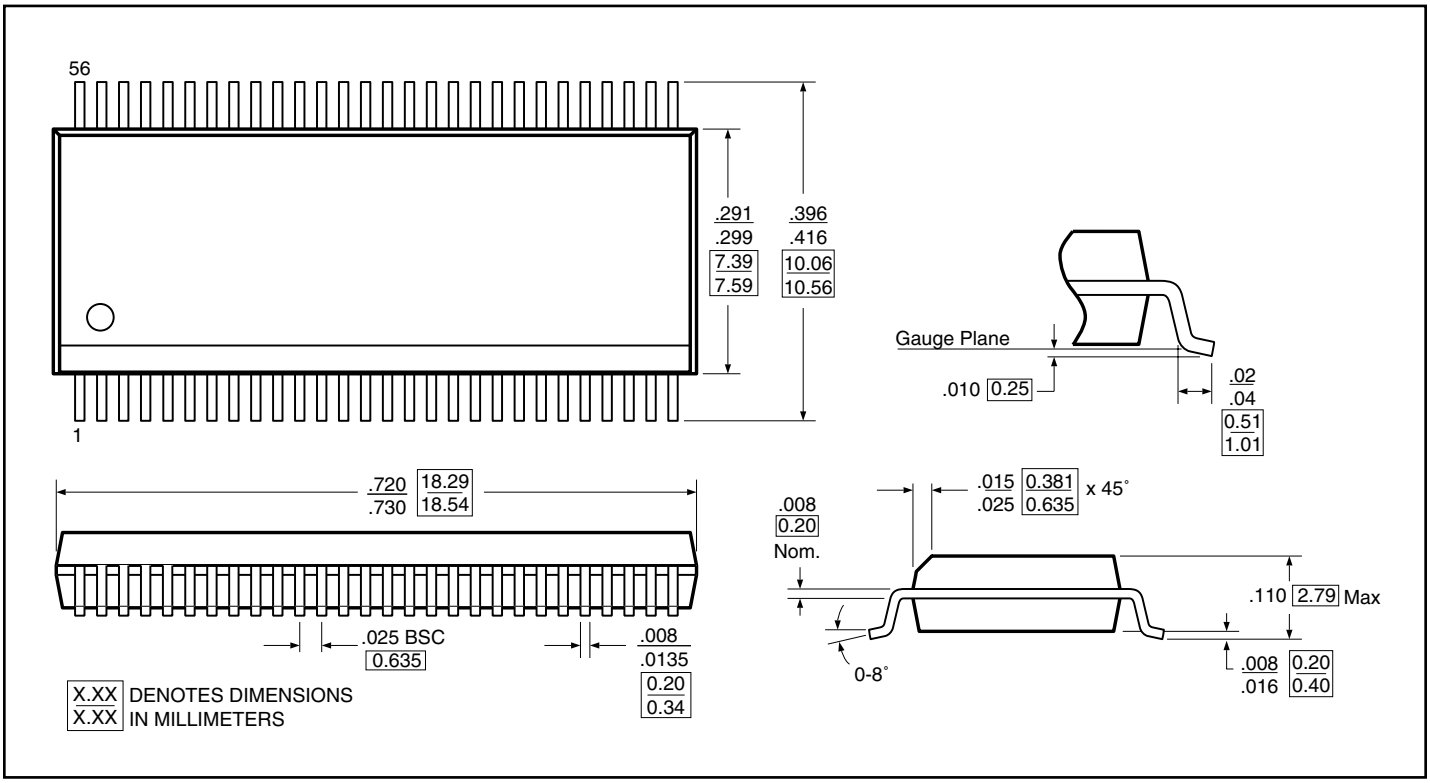
Figure 4. Configuration test load board termination

Note:
1. Maximum 10” trace length for CPU outputs at 200MHz. Maximum 16” trace length for SRC outputs at 100MHz.

Packaging Mechanical: 56-Pin, 240-mil wide TSSOP (A)



Packaging Mechanical: 56-Pin, 300-mil wide SSOP (V)



Ordering Information

Ordering Code	Package Code	Package Description
PI6C410B-01A	A	56-pin TSSOP
PI6C410B-01AE	A	Pb-free & Green, 56-pin TSSOP
PI6C410B-01V	V	56-pin SSOP
PI6C410B-01VE	V	Pb-free & Green, 56-pin SSOP

Notes:
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. Number of transistors = TBD