IXS839 / IXS839A / IXS839B

Synchronous Buck MOSFET Driver

Features:

- Logic Level Gate Drive Compatible
- 2A Source, 4A Sink Peak Drive Current
- Programmable High-Side Driver Turn-on Delay
- Supports Floating Voltage for Top Driver Up to 24V
- IXS839/839B: Undervoltage Lockout
- IXS839A/B: Output Shutdown, Low Side Shutdown Inputs
- 10µA Shut Down Current
- 2mA Quiescent Current (Non- Switching)
- Bootstrapped High Side Driver
- Cross-Conduction Protection

Applications:

- Multiphase Desktop CPU Supplies
- Mobile CPU Core Voltage supplies
- High Current / Low Voltage DC/DC Synchronous Buck Converters

General Description

The IXS839/IXS839A/IXS839B are 2A Source / 4A Sink Synchronous Buck MOSFET Drivers. These Synchronous Buck MOSFET Drivers are specifically designed to drive two N-channel power MOSFETs in a synchronous buck converter. The High-Side driver is powered via a bootstrapped power connection. The driver is capable of 20ns High-Side output, and 18ns Low-Side output transition times driving a 3000pF load.

The IXS839 and IXS839B incorporate an undervoltage lockout to prevent unintentional gate drive output during low voltage conditions. The IXS83A/B include External Shutdown and Low-Side Drive Shutdown features. Simultaneous shutdown of both outputs prevents rapid output capacitor discharge. The high-side turn-on delay is adjustable with an external capacitor added at the DLY pin.

The IXS839/839A/839B are designed to operate over a temperature range of -40°C to +85°C. The IXS839 is available in an 8-Lead SOIC, the IXS839A and the IXS839B in a 10-pin QFN.

Figure 1. IXS839 Functional Block Diagram and General Application Circuit

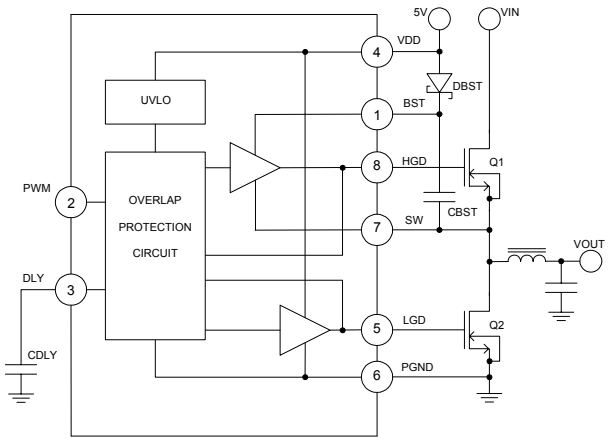


Figure 2. IXS839A Functional Block Diagram and General Application Circuit

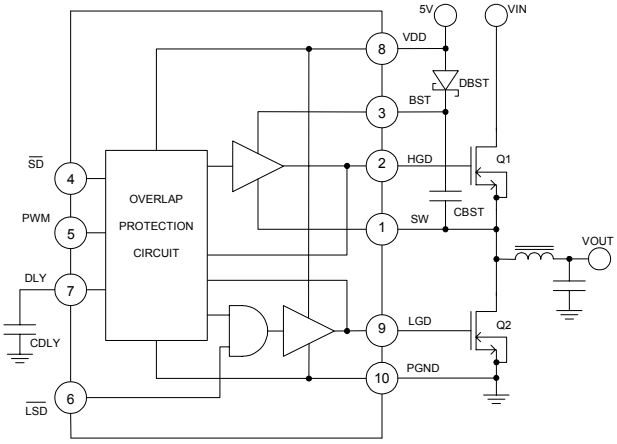
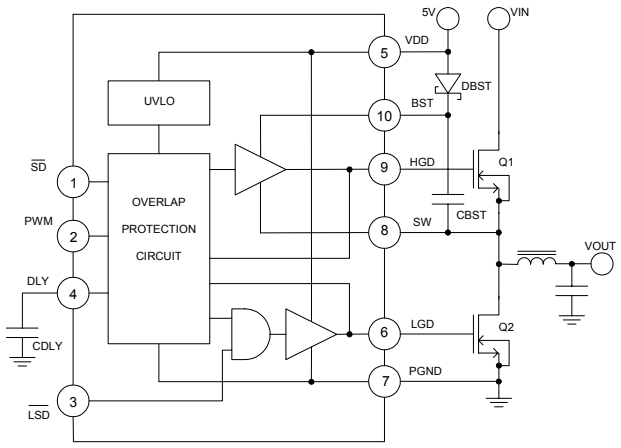


Figure 3. IXS839B Functional Block Diagram and General Application Circuit



Ordering Information

Part No.	Description	Package	Pack Quantity
IXS839S1	Under Voltage Lockout	8-Pin SOIC	98 (Tube)
IXS839S1T/R	Under Voltage Lockout	8-Pin SOIC	2500 (Tape & Reel)
IXS839D1	Under Voltage Lockout	Tested Die	
IXS839AQ2	Driver Shutdown, Low Side Shutdown	10-Pin QFN	121 (Tube)
IXS839AQ2T/R	Driver Shutdown, Low Side Shutdown	10-Pin QFN	2000 (Tape & Reel)
IXS839AD2	Driver Shutdown, Low Side Shutdown	Tested Die	
IXS839BQ2	Under Voltage Lockout , Driver Shutdown, Low Side Shutdown	10-Pin QFN	121 (Tube)
IXS839BQ2T/R	Under Voltage Lockout , Driver Shutdown, Low Side Shutdown	10-Pin QFN	2000 (Tape & Reel)
IXS839BD2	Under Voltage Lockout , Driver Shutdown, Low Side Shutdown	Tested Die	

Absolute Maximum Ratings

Parameter	Rating
V_{DD}	-0.3V to +7V
BST	-0.3V to +30V
BST to SW	-0.3V to +7V
SW	-0.2V to +24V
PWM	-0.3V to +7V
Operating Ambient Temp Range	-40°C to +85°C
Operating Junction Temp Range	-40°C to +125°C
θJA	150°C/W
θJC	40°C/W
Storage Temp Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied. Exposure of the device to the absolute maximum ratings for an extended period may degrade the device and affect its reliability.

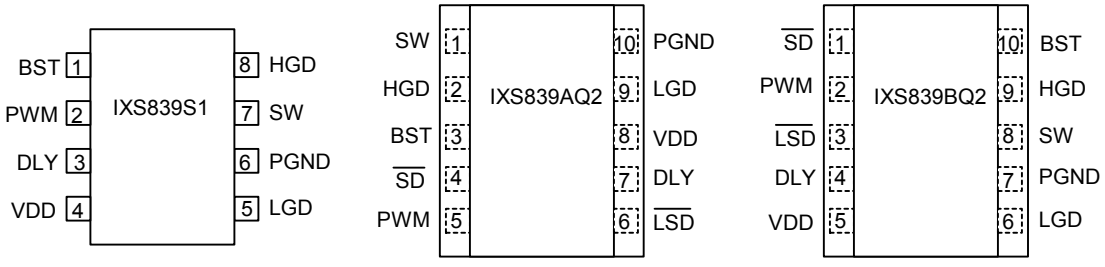
ESD Warning

ESD (electrostatic discharge) sensitive device. Electrostatic charges can readily accumulate on test equipment and the human body in excess of 4000 Volts. This energy can discharge without detection. Although the IXS839/839A/839B feature proprietary ESD protection circuitry, permanent damage may be sustained if subjected to high energy electrostatic discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Pin Description and Configurations

IXS839	IXS839A	IXS839B	Name	Description
1	3	10	BST	Upper Gate Driver Floating DC Power Terminal for Bootstrap Capacitor Connection.
2	5	2	PWM	TTL-level Input Signal with active pull-down. PWM input to the Gate Drivers.
3	7	4	DLY	Terminal for External Delay Capacitor Connection. Capacitor to Ground at this pin adds propagation delay from Lower Gate Driver going Low to the Upper Gate Driver going High. t_{DLY} (nS) = C_{DLY} (pF) x (0.5nS/pF)
4	8	5	VDD	Positive Supply Terminal for Logic and Lower Gate Driver. A ceramic bypass capacitor of 1uF should be connected from VDD to PGND.
5	9	6	LGD	Lower Gate Driver Output Terminal
6	10	7	PGND	Lower Gate Driver DC Power Return Terminal, Logic and Analog Ground
7	1	8	SW	Upper Gate Driver Floating DC Power Return Terminal
8	2	9	HGD	Upper Gate Driver Output Terminal
N/A	4	1	$\overline{SD}$	TTL-level Shut Down Input Signal with active pull-up. $\overline{SD}$ enables normal operation when high. When $\overline{SD}$ is low, the driver outputs are forced low and I_{DD} is at its minimum.
N/A	6	3	$\overline{LSD}$	TTL-level Low Side Shut Down Input Signal with active pull-up. $\overline{LSD}$, when low forces the Lower Gate Driver output low. When $\overline{LSD}$ is high, the lower Gate Driver output is enabled.

SOIC and QFN Top View Pin Configurations



Electrical Characteristics

Power Supply Terminals

T_A = -40°C to 85°C, V_{DD} = 5V, 4V ≤ V_{BST} ≤ 26V

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Analog Supply Voltage Range	V_{DD}	V_{DD}		4.5		5.5	V
High Gate Driver Supply Voltage Range		V_{BST} - V_{SW}		4.5		5.5	V
Low Gate Driver Supply Voltage Range		V_{DD} - V_{PGND}		4.5		5.5	V
Floating Supply Voltage Range		V_{SW} - V_{PGDN}		0.0		24.0	V
Analog Supply Current	I_{DD}	Normal Mode PWM = V_{PGND}			2	4	mA
High Gate Driver Supply Current	I_{BST}	Normal Mode PWM = V_{PGND}	IXS839/839B		0.5	1	mA
			IXS839A			1.5	
Analog Supply Current	$I_{DD\_Shutdown}$	Shut Down Mode, $\overline{LSD}$ = V_{DD}, $\overline{SD}$ = PWM = V_{PGND}	IXS839/839B		10		µA
			IXS839A		50		
High Gate Driver Supply Current	$I_{BST\_Shutdown}$	Shut Down Mode $\overline{LSD}$ = PWM = V_{PGND}			<1	10	µA

Digital Input Terminals

T_A = -40°C to 85°C, V_{DD} = 5V, 4V ≤ V_{BST} ≤ 26V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Leakage Current	I_{IN}	PWM = V_{PGND} LSD = SD = V_{DD}	-1		1	µA
Input pull-down Current		PWM = V_{DD}	2	10	100	µA
Input pull-up Current		$\overline{SD}$ = V_{PGND}	-2	-10	-100	µA
Input pull-up Current		$\overline{LSD}$ = V_{PGND}	-2	-10	-100	µA
Minimum High Level Input Voltage	V_{IH}		2.0			V
Maximum Low Level Input Voltage	V_{IL}				0.8	V

UVLO Circuit

T_A = -40°C to 85°C, V_{DD} = 5V, 4V ≤ V_{BST} ≤ 26V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
V_{DD} Rising Threshold	$UVOL_{RISE}$		4.2	4.4	4.5	V
V_{DD} Falling Threshold	$UVOL_{FALL}$		3.9	4.25	4.5	V

Delay Circuit

T_A = -40°C to 85°C, V_{DD} = 5V, 4V ≤ V_{BST} ≤ 26V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Upper Gate-Driver Turn on Delay Time with respect to external delay capacitor	t_{DLY}	Capacitor C_{DLY}(pF) from DLY pin to PGND		0.5		nS/pF

Electrical Characteristics

High Side Gate Driver Circuit

T_A = -40°C to 85°C, V_{DD} = 5V, 4V ≤ V_{BST} ≤ 26V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High Side Gate-Driver On-Resistance, Sourcing Current	R_{HGD_SRC}	$V_{BST} – V_{SW}$ = 4.6V			2.2	Ω
High Side Gate-Driver On-Resistance, Sinking Current	R_{HGD_SNK}	$V_{BST} – V_{SW}$ = 4.6V			1.2	Ω
High Side Gate-Driver(1) Rise-Time	t_{R_HGD}	C_{LOAD} = 3nF T_{R_HGD} measured from 10% to 90% of (V_{HGD} - V_{SW})			20	nS
High Side Gate-Driver(1) Fall-Time	t_{F_HGD}	C_{LOAD} = 3nF T_{F_HGD} measured from 90% to 10% of (V_{HGD} - V_{SW})			15	nS
Propagation Delay(1)	t_{PD_HGD1} t_{PD_HGD2}	C_{LOAD_HGD} = C_{LOAD_LGD} = 3nF C_{DLY} = 0pF			35 50	nS nS

Low Side Gate Driver Circuit

T_A = -40°C to 85°C, V_{DD} = 5V, 4V ≤ V_{BST} ≤ 26V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Low Side Gate-Driver On-Resistance, Sourcing Current	R_{LGD_SRC}	$V_{DD} – V_{PGND}$ = 4.6V			2	Ω
Low Side Gate-Driver On-Resistance, Sinking Current	R_{LGD_SNK}	$V_{DD} – V_{PGND}$ = 4.6V			1	Ω
Low Side Gate-Driver(1) Rise-Time	t_{R_LGD}	C_{LOAD} = 3nF T_{R_LGD} measured from 10% to 90% of ($V_{LGD} – V_{PGND}$)			18	nS
Low Side Gate-Driver(1) Fall-Time	t_{F_LGD}	C_{LOAD} = 3nF T_{F_LGD} measured from 90% to 10% of (V_{LGD} - V_{SW})			12	nS
Propagation Delay(1)	t_{PD_LGD1} t_{PD_LGD2}	C_{LOAD_HGD} = C_{LOAD_LGD} = 3nF C_{DLY} = 0pF			60 20	nS nS

Shut Down Circuit Characteristics

T_A = -40°C to 85°C, V_{DD} = 5V, 4V ≤ V_{BST} ≤ 26V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Propagation Delay(2)	t_{PD_LGDSD1}			25	50	nS
Propagation Delay(2)	t_{PD_LGDSD2}			10	20	nS
Propagation Delay(3)	t_{PD_GDSD1}			400	800	nS
Propagation Delay(3)	t_{PD_GDSD2}			800	1200	nS

*Notes:

(1) See Timing Diagram in Figure 4

(2) See Timing Diagram in Figure 5

(3) See Timing Diagram in Figure 6

Figure 4. Non-Overlap Timing Diagram for IXS839/839A/839B

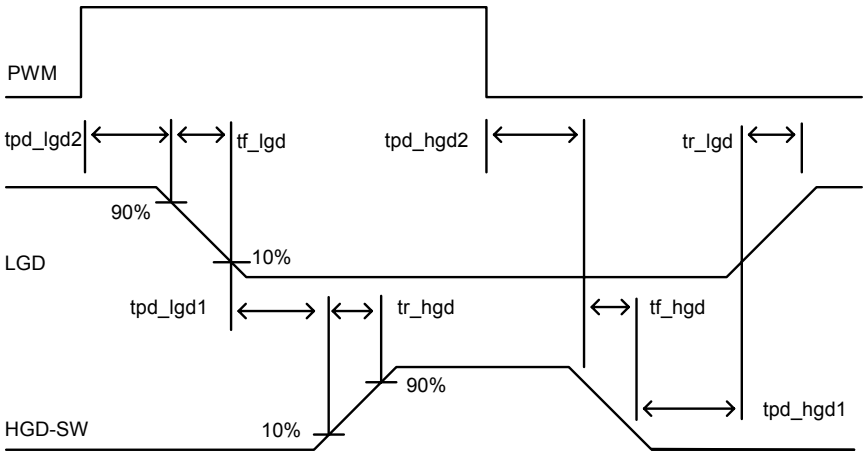


Figure 5. $\overline{\text{LSD}}$ Propagation Delay Timing for IXS839A/B

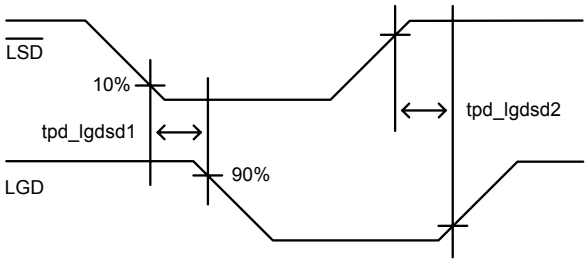
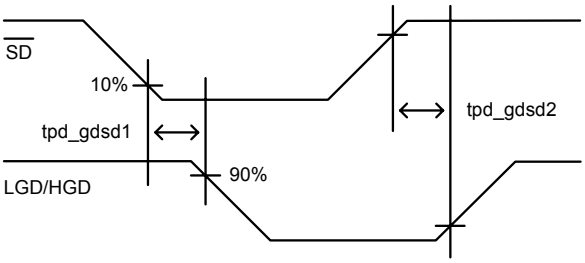
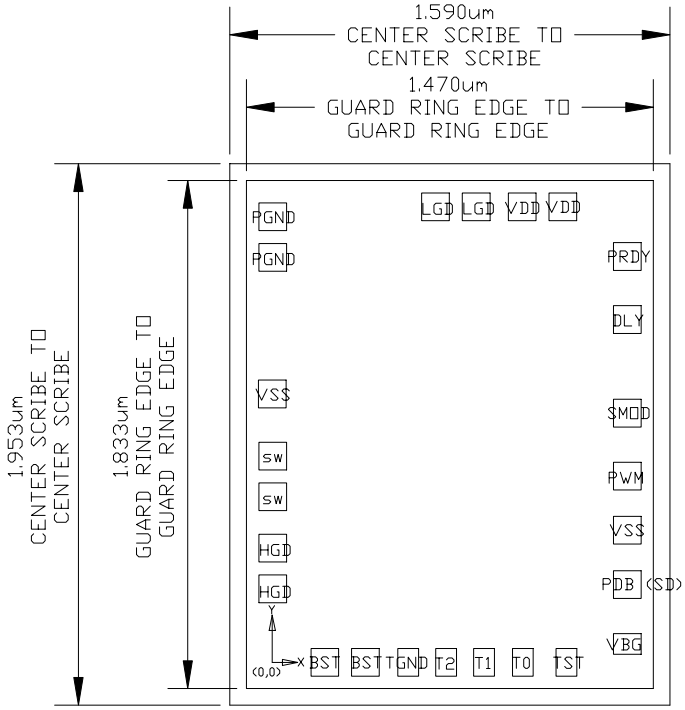


Figure 6. $\overline{\text{SD}}$ Propagation Delay Timing for IXS839A/B



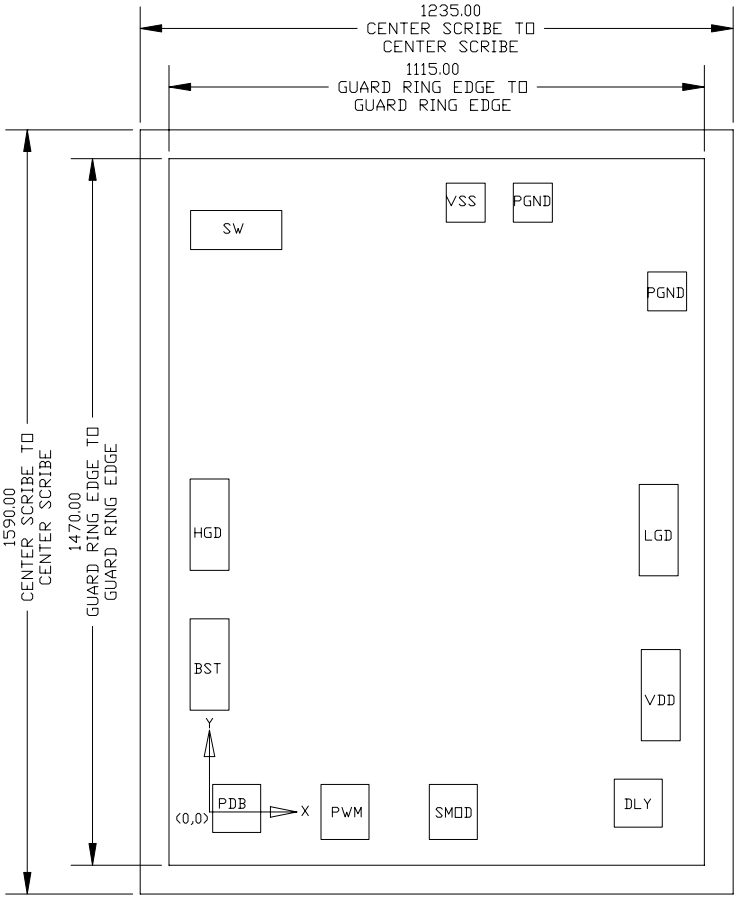
IXS839 and IXS839B Die Size and Pad Locations:



Ref. No.	Signal Name	Signal Type	Passivation Opening		Location [1]	
			X (um)	Y (um)	X (um)	Y (um)
1	HGD	Digital Output	100	100	2	266
2	HGD	Digital Output	100	100	2	412
3	SW	Power Supply	100	100	2	598
4	SW	Power Supply	100	100	2	744
5	VSS	Power Supply	100	100	0	968
6	PGND	Power Supply	100	100	2	1461
7	PGND	Power Supply	100	100	2	1608
8	LGD	Digital Output	100	100	590	1644
9	LGD	Digital Output	100	100	737	1644
10	VDD	Power Supply	100	100	903	1644
11	VDD	Power Supply	100	100	1050	1644
12	PRDY (Power Ready)	Digital Output	100	100	1283	1464
13	DLY	Digital I/O	100	100	1283	1237
14	SMOD (LSD BAR)	Digital Input	100	100	1283	899
15	PWM	Digital Input	100	100	1283	672
16	VSS	Power Supply	100	100	1283	477
17	SD (SDI BAR)	Digital Input	100	100	1283	280
18	VBG	No Connect	N/A	N/A	N/A	N/A
19	TST	No Connect	N/A	N/A	N/A	N/A
20	T0	No Connect	N/A	N/A	N/A	N/A
21	T1	No Connect	N/A	N/A	N/A	N/A
22	T2	No Connect	N/A	N/A	N/A	N/A
23	TGND	No Connect	N/A	N/A	N/A	N/A
24	BST	Power Supply	100	100	337	0
25	BST	Power Supply	100	100	190	0

Notes:
(1) Location is the distance from origin to the center of the passivation opening.

IXS839A Die Size and Pad Locations:



Ref. No.	Signal Name	Signal Type	Passivation Opening		Location [1]	
			X (um)	Y (um)	X (um)	Y (um)
1	HGD	Digital Output	81	190	0	598
2	SW	Power Supply	190	81	56	1211
3	VSS	Power Supply	81	81	534	1268
4	PGND	Power Supply	81	81	673	1268
5	PGND	Power Supply	81	81	953	1083
6	LGD	Digital Output	81	190	936	586
7	VDD	Power Supply	81	190	940	243
8	DLY	Digital I/O	100	100	893	18
9	SMOD (LSD BAR)	Digital Input	100	115	508	0
10	PWM	Digital Input	100	115	282	0
11	PDB (SDI BAR)	Digital Input	100	100	57	7
12	BST	Power Supply	81	190	0	307

Notes:
(1) Location is the distance from origin to the center of the passivation opening.

Typical Performance Characteristics

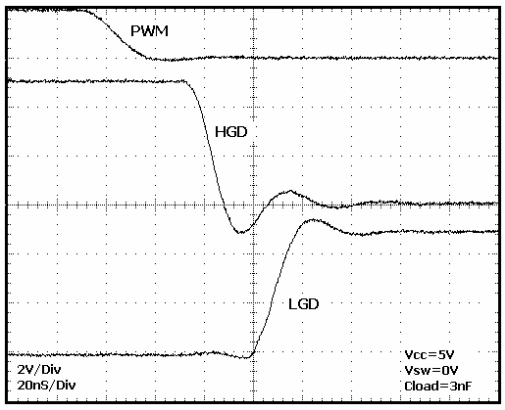


Fig 7. HGD Fall and LGD Rise Times

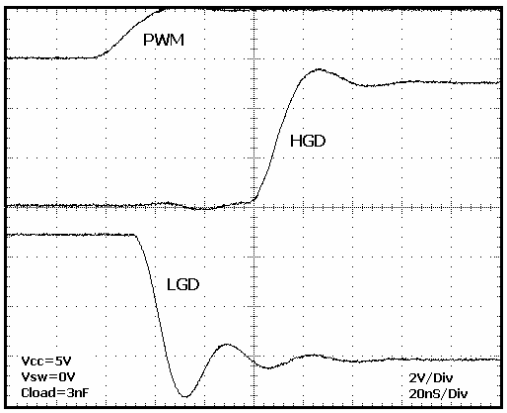


Fig 8. LGD Fall and HGD Rise Times

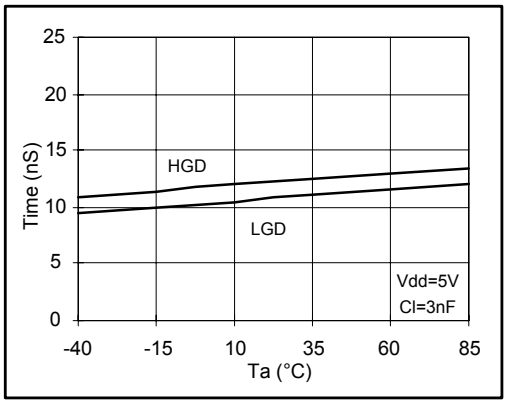


Fig 9. HGD & LGD Rise Time vs. Temperature

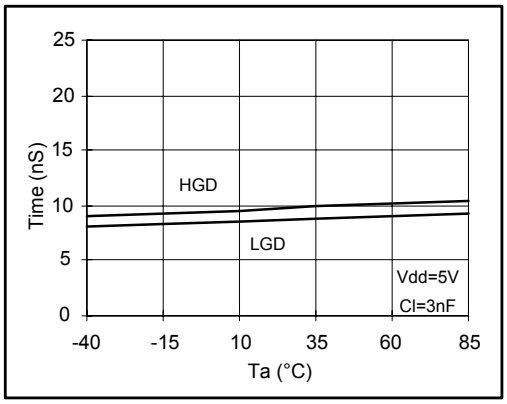


Fig 10. HGD & LGD Fall Time vs. Temperature

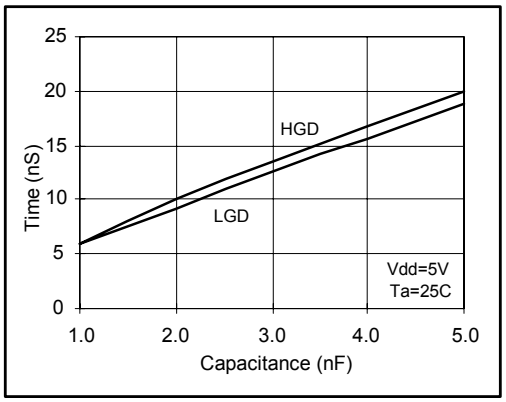


Fig 11. HGD and LGD Rise Time vs. Load Capacitance

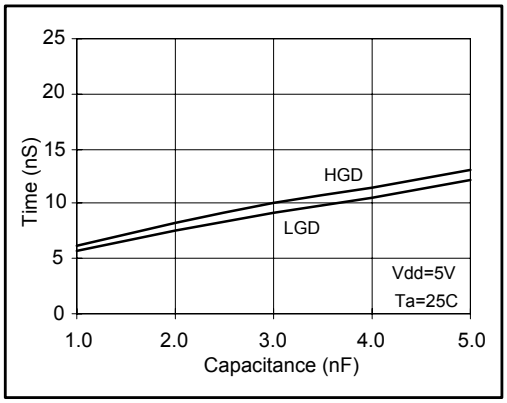


Fig 12. HGD and LGD Fall Time vs. Load Capacitance

Typical Performance Characteristics

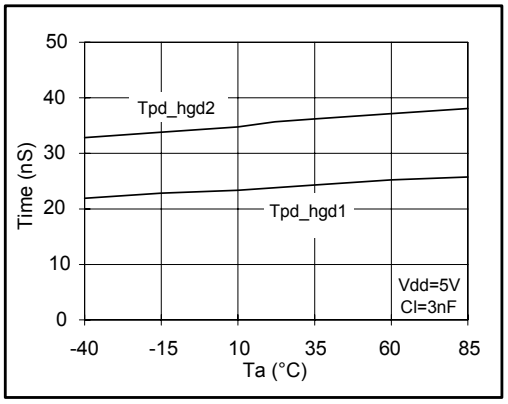


Fig 13. HGD Propagation Delay vs. Temperature

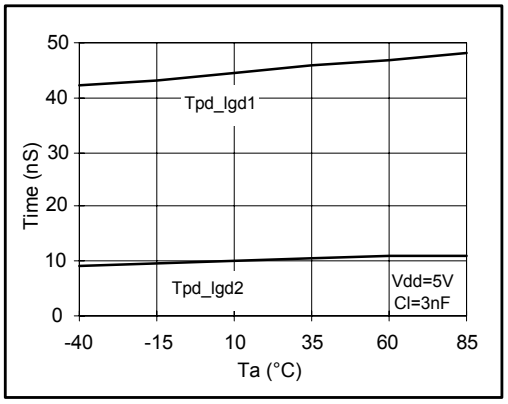


Fig 14. LGD Propagation Delay vs. Temperature

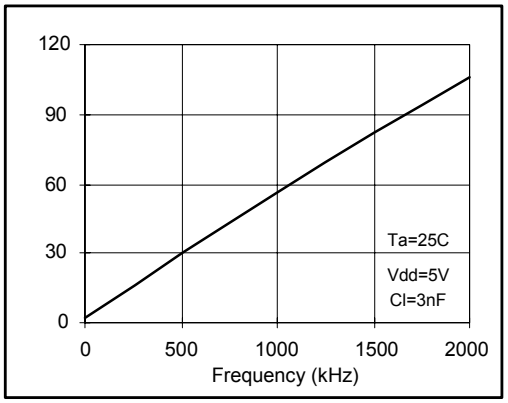


Fig 15. Supply Current vs. Frequency

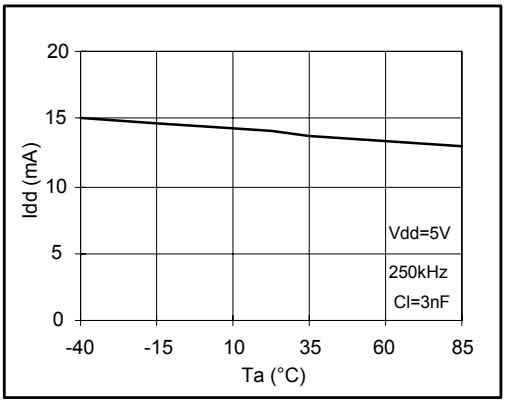
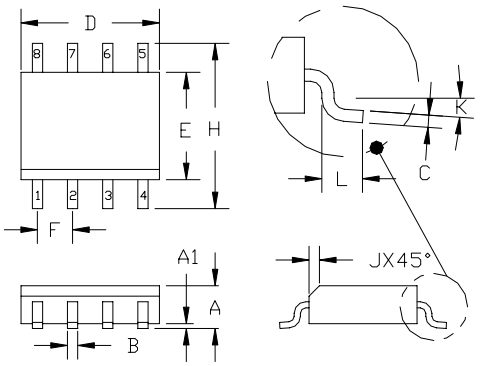


Fig 16. Supply Current vs. Temperature

Package Outlines

8-PIN SOIC



DIMENSIONS (1)					
DIM.	INCH		MM.		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.0532	.0688	1.35	1.75	----
A1	.0040	.0098	.10	.25	----
B	.013	.020	.33	.51	----
C	.0075	.0098	.19	.25	----
D	.1890	.1968	4.80	5.00	(2)
E	.1497	.1574	3.80	4.00	(2)
F	.050 BSC		1.27 BSC		----
H	.2284	.2440	5.80	6.20	----
J	.0099	.0196	.25	.50	----
K	0°	8°	0°	8°	----
L	.016	.050	.40	1.27	----

3. MOLDED PACKAGE SHALL CONFORM TO JEDEC STANDARD CONFIGURATION MS-012 VARIATION AA.

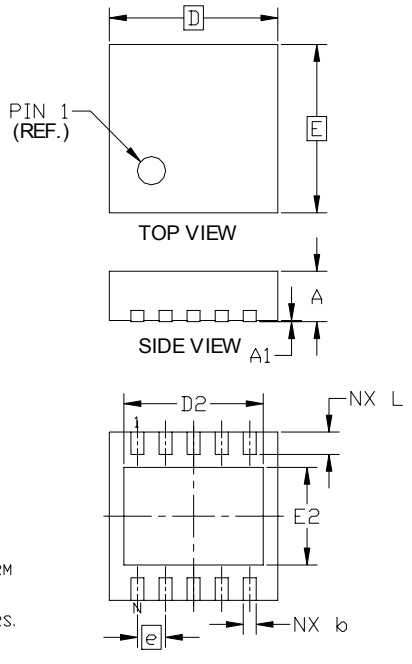
(2) DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.

(1) CONTROLLING DIMENSIONS: MILLIMETERS.

NOTES: (UNLESS OTHERWISE SPECIFIED)

QFN - 10

DIMENSIONS (1)				
DIM.	INCH		MM.	
	MIN.	MAX.	MIN.	MAX.
A	.0315	.0394	.80	1.00
A1	0	.0020	0	.05
b	.007	.012	.18	.30
D	.118 BSC		3.00 BSC	
D2	.0866	.1063	2.20	2.70
E	.118 BSC		3.00 BSC	
E2	.055	.069	1.40	1.75
e	.0197 BSC		.50 BSC	
L	.0118	.0197	.30	.50
N	10		10	



3. MOLDED PACKAGE SHALL CONFORM TO JEDEC STANDARD CONFIGURATION MO-229 VARIATION VEED-5.

2. DIMENSIONS AND TOLERANCING CONFORM TO ASME Y14.5M-1994.

(1) CONTROLLING DIMENSIONS: MILLIMETERS.

NOTES: (UNLESS OTHERWISE SPECIFIED)

Theory of Operation

The IXS839/839A/839B are dual MOSFET drivers, designed to drive two external N-channel power MOSFETs. The low-side driver is designed to drive a non-floating N-channel power MOSFET and its output is out of phase with the PWM input. The high-side driver is designed to drive a floating N-channel power MOSFET and its output is in phase with the PWM input. An external bootstrap circuit provides the floating power supply to the high-side driver.

The bootstrap circuit consists of a Schottky diode and a boost capacitor. When the PWM input transitions to a logic low, the low-side power MOSFET turns ON, the SW node is pulled to ground, and the bootstrap capacitor is charged to VDD through the Schottky diode. When the PWM transitions to a logic high, the high side power MOSFET begins to turn on and the SW node rises up to the input supply, VIN. In turn the boost capacitor raises the BST node voltage to a level equal to the input supply plus the boost capacitor voltage, providing sufficient voltage to the BST node to turn on the High-Side Power MOSFET. An internal cross-conduction prevention circuit monitors both gate driver outputs and allows each driver output to turn ON only when the other output driver turns OFF and falls below 1V.

The IXS839A is a cost reduced Driver, differentiated by the absence of the undervoltage lockout protection circuit featured in the IXS839 and IXS839B. IXS839A/B must be enabled using the SD terminal when the driver supply reaches the operating range. SD can be used to turn off both driver outputs to prevent the rapid discharge of the buck converter output capacitors. An additional terminal, LSD can be used to turn off the Low-Side Gate Driver Output. The High-Side Gate Driver remains active in this mode.

Detailed Circuit Description

(Refer to the Application Diagrams)

The PMW input signal controls both the High Side and Low Side power MOSFET drivers. The Power MOSFETs are driven so that the SW node follows the polarity of the PWM signal.

Low-Side Gate Driver

The Low-Side Gate Driver is designed to drive a ground referenced N-Channel Power MOSFET. In a synchronous buck converter application, it drives the gate of the synchronous rectifier FET, (Q2). When the driver is enabled, (IXS839A/B SD=LSD=VDD), the driver output is 180˚ out of phase with the PWM input. The internal overlap protection circuit monitors the High-Side Gate Driver, and allows the Low-Side Gate Driver to turn on only when the High-Side Gate Driver output falls below 1.0 Volt. The supply rails for the Low-Side Gate Driver are VDD and PGND.

High-Side Gate Driver

The High-Side Gate Driver is designed to drive a floating N-Channel Power MOSFET referenced to SW. In a synchronous buck converter application, it drives the gate of the high side power MOSFET, (Q1). When the driver is enabled (IXS839A/B SD=VDD), the driver output is in phase with the PWM input. The bootstrap supply rails for the High-Side Gate Driver are BST and SW, and are generated by an external bootstrap circuit. The bootstrap circuit consists of a Schottky diode DBST, and a bootstrap capacitor CBST. During start up, the SW pin is at ground and the bootstrap capacitor CBST charges up to VDD through the Schottky diode DBST. When the PWM input transitions high the High-Side Gate Driver begins to turn Q1 ON by transferring charge from the bootstrap capacitor CBST to the gate of Q1. As Q1 turns on the SW pin will rise up to VIN, forcing the BST pin to VIN + VBOOSTCAP. This supplies the required gate to source voltage to Q1. When PWM transitions low the High-Side Driver and in turn Q1 switch off. When SW falls below 1 Volt the Low-Side Gate Driver turns on and recharges the bootstrap capacitor which completes the cycle.

Overlap Protection Circuit

The overlap protection circuit (OPC) monitors the High Side and Low Side Gate Driver Outputs and prevents both main power switches, Q1 and Q2, from being ON at the same time. This inhibits excessive shoot-through currents and minimizes the associated losses.

When the PWM input transitions low, Q1 begins to turn OFF, and Q2 turns ON only when the High-Side Gate Driver output falls below 1 volt. By

waiting for the voltage on the High Side Gate Driver Output pin to reach 1 volt, the overlap protection circuit ensures that Q1 is OFF before Q2 turns on.

Similarly, when the PWM input transitions high, Q2 begins to turn OFF, and Q1 turns ON after the overlap protection circuit detects that the voltage at the Low-Side Gate Driver output has dropped below 1 volt. Once the driver output voltage falls below 1 volt, the overlap protection circuit initiates a delay timer that adds additional delay set by the external capacitor connected to the DLY pin. This programmable delay circuit allows adjustments to optimize performance based on the switching characteristics of the external power MOSFET.

Low-Side Driver Shutdown
The IXS839A/B include a Low-Side Gate Driver shutdown feature. A logic low signal at the LSD input shuts down the Low Side Gate Driver, and in turn the synchronous rectifier FET. This signal can be used to achieve maximum battery life under light load conditions and maximum efficiency under heavy load conditions. Under heavy load conditions, LSD should be high so that the synchronous switch is controlled by the PWM signal for maximum efficiency. Under light load conditions the LSD can be low to disable the Low Side Gate Driver so the switching current can be minimized.

Shutdown
For optimal system power management, the IXS839A/B drivers can be shut down to conserve power. When the SD pin is high, the IXS839A/B are enabled for normal operation. Pulling the SD pin low forces the HGD and LGD outputs low, and reduces the supply current by disabling the internal reference.

Under Voltage Lockout (IXS839 and IXS839B)
The Under Voltage Lockout (UVLO) circuit holds both driver outputs low during VDD supply ramp-up. The UVLO logic becomes active and in control of the driver outputs at a supply voltage of no greater than 1.5 V. When the supply voltage rises above the UVLO upper threshold the circuit allows the PWM input to control the drivers.

Application Information

Supply Capacitor Selection
A 1 uF ceramic bypass capacitor is recommended for the VDD input to provide noise suppression. The bypass capacitor should be located as close as possible to the IXS939/A/B.

Bootstrap Circuit
The bootstrap circuit requires a charge storage capacitor CBST and a Schottky diode DBST, as shown in Figure 1. Selecting these components should be done with consideration of the electrical characteristics of the high-side FET chosen.

The bootstrap capacitor voltage rating must exceed the maximum input voltage, (VIN) + the maximum VDD voltage. The capacitance is determined using the following equation:

$$C_{BST} = \frac{Q_{GATE}}{\Delta V_{BST}}$$

Where, QGATE is the total gate charge of Q1, and ΔVBST is the allowable Q1 voltage droop.

To maximize the available drive for Q1 in the bootstrap circuit a Schottky diode is recommended. The bootstrap diode voltage rating must exceed the maximum input voltage, (VIN) + the maximum VDD voltage. The average forward current can be estimated by:

$$I_{F(AVG)} = Q_{GATE} \text{ X } F_{MAX}$$

where F_{MAX} is the maximum PWM input switching frequency. Peak surge current is dependent on the source impedance of the 5V supply and the ESR of CBST, and should be checked in-circuit.

Delay Capacitor Selection
A ceramic capacitor is recommended for the DLY input, and should be located as close a possible to the DLY pin.

Printed Circuit Board Layout Considerations
Use the following general guidelines when designing printed circuit boards:

1. Trace out the high current paths and use short, wide traces to make these connections.
2. Locate the VDD bypass capacitor as close as possible to the VDD and PGND pins.
3. Connect the source of the Lower MOSFET, (Q2) as close as possible the PGND.