

# MSM521008

**131,072-Word × 8-Bit CMOS STATIC RAM**

## DESCRIPTION

The MSM521008 is a 131,072-word by 8-bit CMOS fast static RAM featuring a single 5 V power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to use. The MSM521008 uses NMOS cells and CMOS peripherals and provides high-speed operation at 17 ns access time. In addition, the MSM521008 is provided with a chip enable signal ( $\overline{CE}_1$ ) suited to the expansion of a memory capacity, a chip enable signal ( $CE_2$ ) suited to the power-down function, and an output enable signal ( $\overline{OE}$ ) suited to the I/O bus line control.

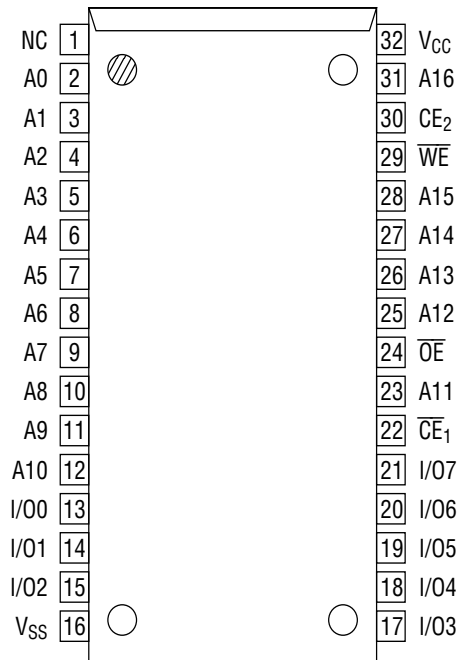
## FEATURES

- 131,072-word × 8-bit configuration
- Single 5 V power supply
- Fully static operation
- Operating temperature range: Ta = 0°C to 70°C
- Power dissipation
  - Standby: 1 mA (Max.)
  - Operation:
    - 17 180 mA (Max.)
    - 20 170 mA (Max.)
    - 25 160 mA (Max.)
- Access time:
  - 17 17 ns (Max.)
  - 20 20 ns (Max.)
  - 25 25 ns (Max.)
- (Input/Output) TTL compatible
- Power-down function by chip enable signal
- 3-state output
- Package:
  - 32-pin 400 mil plastic SOJ (SOJ32-P-400-1.27) (Product : MSM521008-xxJS)
  - xx indicates speed rank.

## PRODUCT FAMILY

Family	Access Time (Max.)	Package
MSM521008-17	17 ns	400 mil 32-pin SOJ
MSM521008-20	20 ns	
MSM521008-25	25 ns	

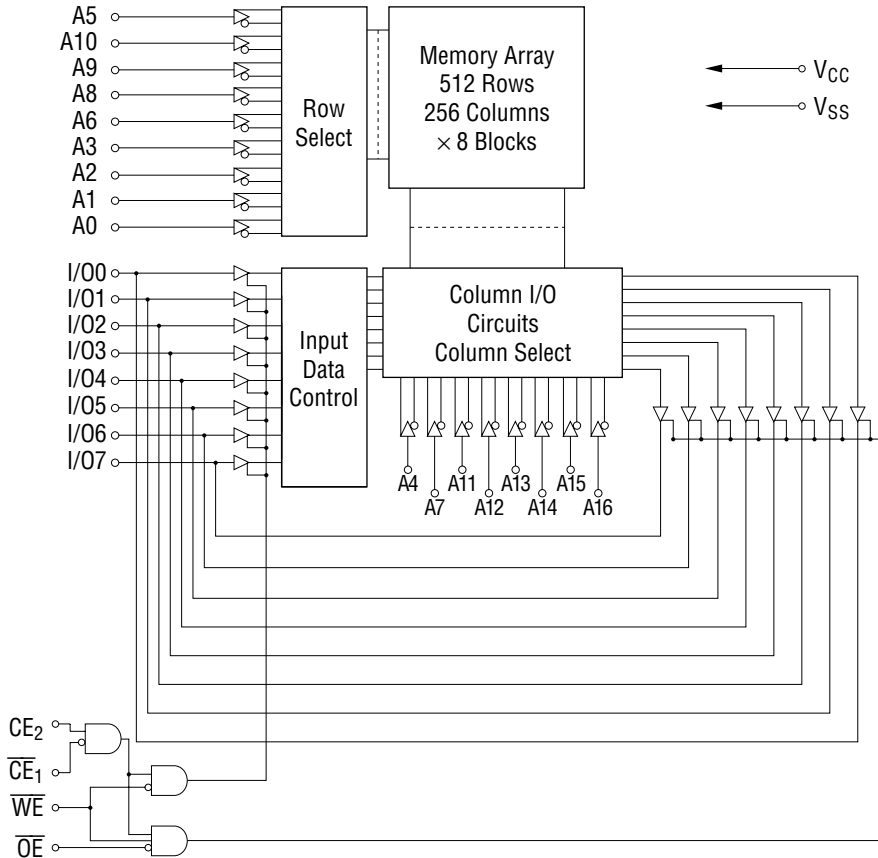
**PIN CONFIGURATION (TOP VIEW)**



32-Pin Plastic SOJ

Pin Name	Function
A0 - A16	Address Input
I/O0 - I/O7	Data Input/Output
$\overline{CE}_1, CE_2$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$V_{CC}, V_{SS}$	Power Supply
NC	No Connection

**BLOCK DIAGRAM**



**FUNCTION TABLE**

Operating Mode	$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	Operating Contents	Power Mode
Read Cycle	H	*	*	*	Output Floating	Standby
	*	L	*	*		Standby
	L	H	H	H	Data Read	Active
	L	H	H	L		Active
Write Cycle	H	*	*	*	Output Floating	Standby
	*	L	*	*		Standby
	L	H	L	*	Data Write	Active

\*Don't Care ("H" or "L")

## ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	$V_{CC}$	$T_a = 25^\circ\text{C}$ , for $V_{SS}$	-0.3 to 7.0	V
Pin Voltage	$V_T$		$-0.3^*$ to $V_{CC} + 0.3$	V
Power Dissipation	$P_D$	$T_a = 25^\circ\text{C}$	1.0	W
Operating Temperature	$T_{opr}$	—	0 to 70	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	—	-55 to 125	$^\circ\text{C}$

\* -3.0 V Min. for pulse width less than 10 ns.

### Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	$V_{CC}$	—	4.5	5	5.5	V
	$V_{SS}$		0	0	0	V
Input High Voltage	$V_{IH}$	$V_{CC} = 5\text{ V} \pm 10\%$	2.2	—	$V_{CC} + 0.3$	V
Input Low Voltage	$V_{IL}$		$-0.3^*$	—	0.8	V
Load Capacitance	$C_L$	—	—	—	30	pF

\* -3.0 V Min. for pulse width less than 10 ns.

### Capacitance

( $T_a = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )

Parameter	Symbol	Condition	Min.	Max.	Unit
Input Capacitance	$C_I$	$V_{IN} = 0\text{ V}$	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0\text{ V}$	—	8	pF

Note: This parameter is periodically sampled and not 100% tested.

DC Characteristics

(V<sub>CC</sub> = 5 V ±10%, Ta = 0°C to 70°C)

Parameter	Symbol	Condition	MSM521008			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> = 0 to V <sub>CC</sub>	-10	—	10	μA
Output Leakage Current	I <sub>LO</sub>	$\overline{CE}_1 = V_{IH}$ or $CE_2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ , V <sub>OUT</sub> = 0 to V <sub>CC</sub>	-10	—	10	μA
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0 mA	2.4	—	—	V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8.0 mA	—	—	0.4	V
Standby Power Supply Current	I <sub>CCS</sub>	$\overline{CE}_1 \geq V_{CC} - 0.2$ V, $CE_2 \geq V_{CC} - 0.2$ V or 0 V ≤ CE <sub>2</sub> ≤ 0.2 V, V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V	—	—	1	mA
	I <sub>CCS1</sub>	$\overline{CE}_1 = V_{IH}$ , CE <sub>2</sub> = V <sub>IL</sub> , T <sub>CYC</sub> = Min. cycle	—	—	20	mA
Operating Power Supply Current	I <sub>CCA</sub>	$\overline{CE}_1 = V_{IL}$ , CE <sub>2</sub> = V <sub>IH</sub> , T <sub>CYC</sub> = Min. cycle, I <sub>OUT</sub> = 0 mA	—	—	①	mA

① 521008-17 180 mA  
521008-20 170 mA  
521008-25 160 mA

AC Characteristics

Test Conditions

Parameter	Condition
Input Pulse Level	V <sub>IH</sub> = 3 V, V <sub>IL</sub> = 0 V
Input Rise and Fall Times	3 ns
Input/Output Timing Level	1.5 V
Output Load	See Figures

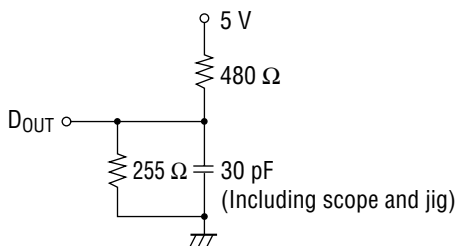


Figure 1 Output Load

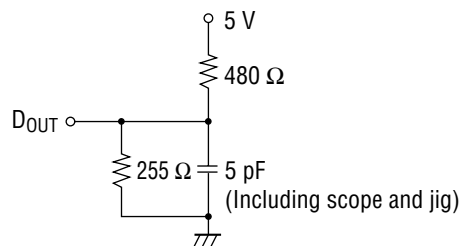


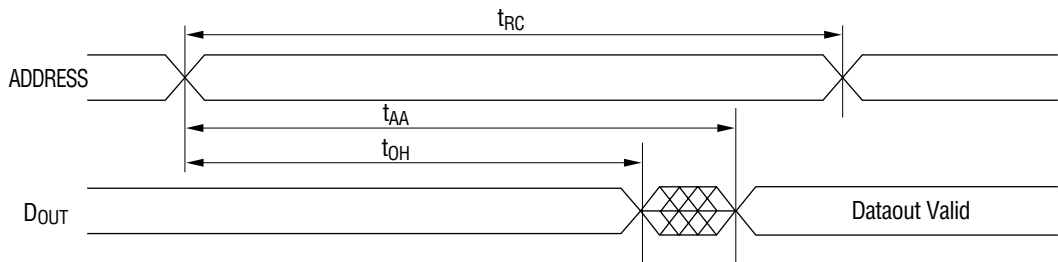
Figure 2 Output Load  
(t<sub>OLZ</sub>, t<sub>OHZ</sub>, t<sub>CLZ1</sub>, t<sub>CLZ2</sub>, t<sub>CHZ1</sub>, t<sub>CHZ2</sub>, t<sub>WLZ</sub>, t<sub>WHZ</sub>)

Read Cycle

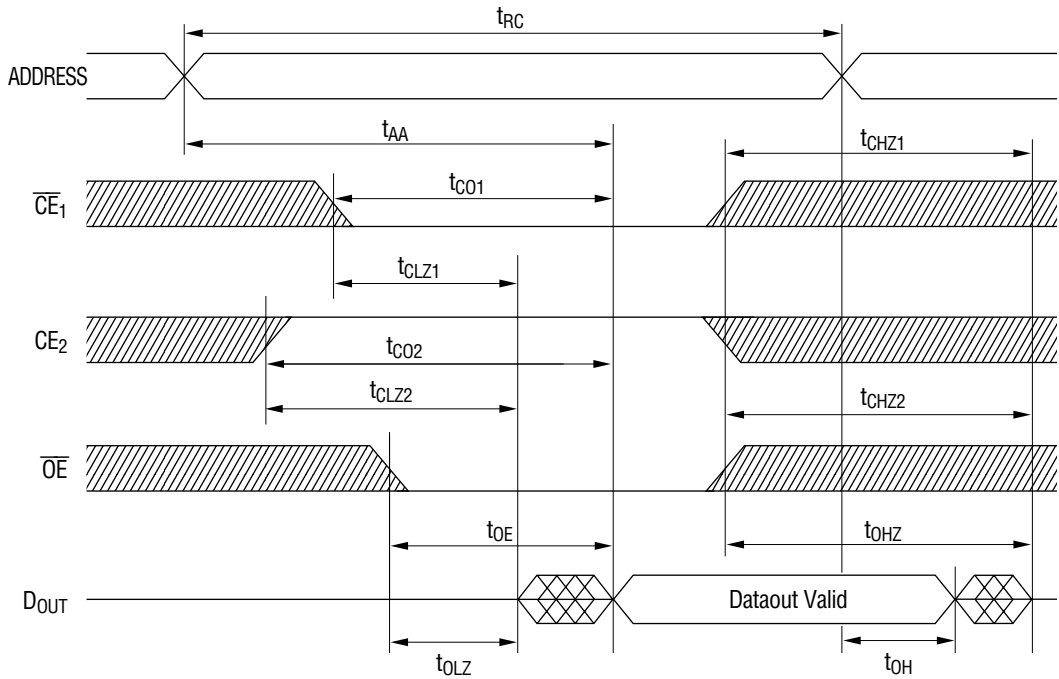
( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_a = 0^\circ\text{C}$  to  $70^\circ\text{C}$ )

Parameter	Symbol	MSM521008-17		MSM521008-20		MSM521008-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	$t_{RC}$	17	—	20	—	25	—	ns
Address Access Time	$t_{AA}$	—	17	—	20	—	25	ns
$\overline{CE}_1, CE_2$ Access Time	$t_{C01}$	—	17	—	20	—	25	ns
	$t_{C02}$	—	17	—	20	—	25	
$\overline{OE}$ Access Time	$t_{OE}$	—	9	—	10	—	12	ns
$\overline{CE}_1, CE_2$ to Output in Low-Z	$t_{CLZ1}$	3	—	3	—	3	—	ns
	$t_{CLZ2}$	3	—	3	—	3	—	
$\overline{OE}$ to Output in Low-Z	$t_{OLZ}$	0	—	0	—	0	—	ns
Output Hold Time from Address Change	$t_{OH}$	3	—	3	—	3	—	ns
$\overline{CE}_1, CE_2$ to Output in High-Z	$t_{CHZ1}$	—	7	—	8	—	10	ns
	$t_{CHZ2}$	—	7	—	8	— </td <td>10</td>	10	
$\overline{OE}$ to Output in High-Z	$t_{OHZ}$	—	7	—	8	—	10	ns

Address Controlled Read ( $\overline{WE} = H, \overline{CE}_1 = L, CE_2 = H, \overline{OE} = L$ )



**$\overline{CE}_1$ ,  $CE_2$ ,  $\overline{OE}$  Controlled Read ( $\overline{WE} = H$ )**



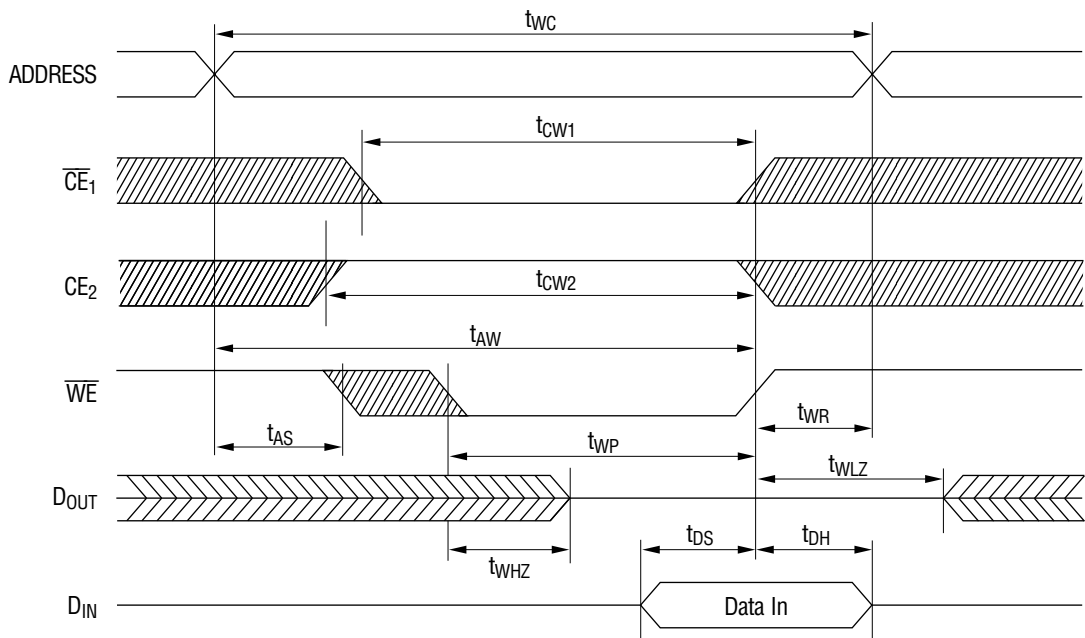
- Notes :
1. A read cycle occurs during the overlap of  $\overline{CE}_1 = "L"$ ,  $CE_2 = "H"$ ,  $\overline{OE} = "L"$  and  $\overline{WE} = "H"$ .
  2.  $t_{CLZ1}$  and  $t_{CLZ2}$  are specified from  $\overline{CE}_1 = "L"$  or  $CE_2 = "H"$ , whichever occurs last.
  3.  $t_{CHZ1}$  and  $t_{CHZ2}$  are specified from  $\overline{CE}_1 = "H"$  or  $CE_2 = "L"$ , whichever occurs first.
  4.  $t_{OHZ}$ ,  $t_{CHZ1}$  and  $t_{CHZ2}$  are specified by the time when DATA is floating, not defined by the output level.

**Write Cycle**

( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_a = 0^\circ\text{C}$  to  $70^\circ\text{C}$ )

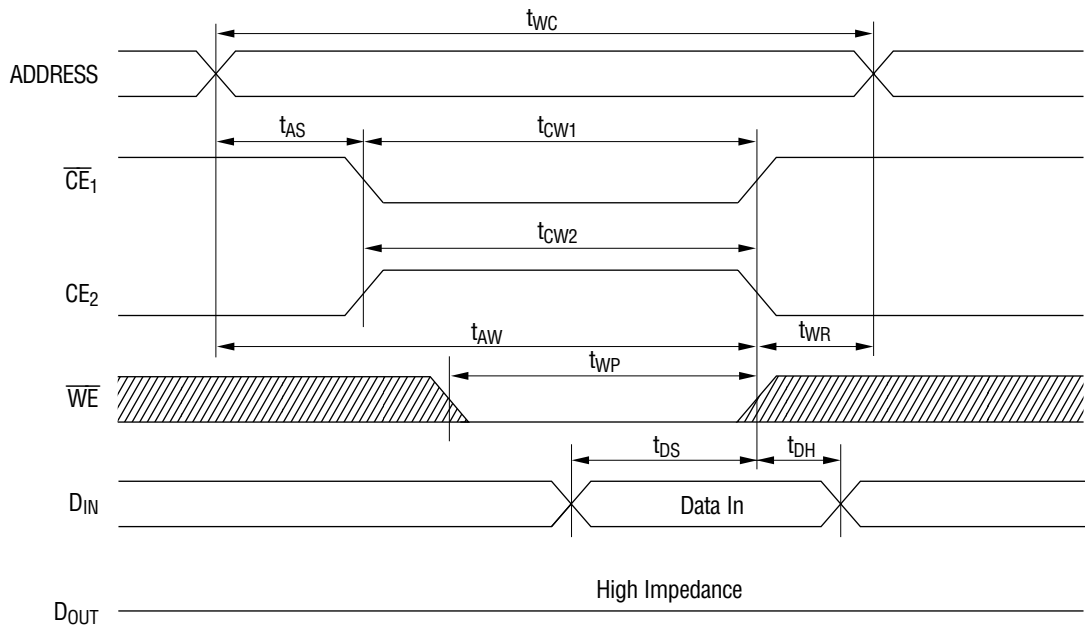
Parameter	Symbol	MSM521008-17		MSM521008-20		MSM521008-25		Unit	
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Cycle Time	$t_{WC}$	17	—	20	—	25	—	ns	
Address Setup Time	$t_{AS}$	0	—	0	—	0	—	ns	
Write Pulse Width	$t_{WP}$	13	—	15	—	20	—	ns	
Write Recovery Time	$\overline{WE}$	$t_{WR}$	0	—	0	—	0	—	ns
	$\overline{CE}_1$		0	—	0	—	0	—	
	$CE_2$		0	—	0	—	0	—	
Data Setup Time	$t_{DS}$	9	—	10	—	12	—	ns	
Data Hold Time	$t_{DH}$	0	—	0	—	0	—	ns	
$\overline{WE}$ to Output in High-Z	$t_{WHZ}$	—	7	—	8	—	10	ns	
$\overline{CE}_1, CE_2$ to End of Write	$t_{CW1}$	13	—	15	—	20	—	ns	
	$t_{CW2}$	13	—	15	—	20	—		
Address Valid to End of Write	$t_{AW}$	13	—	15	—	20	—	ns	
Output Active from End of Write	$t_{WLZ}$	0	—	0	—	0	—	ns	

**$\overline{WE}$  Controlled Write ( $\overline{OE} = L$ )**





**$\overline{CE}_1$ ,  $CE_2$  Controlled Write ( $\overline{OE} = H$ )**



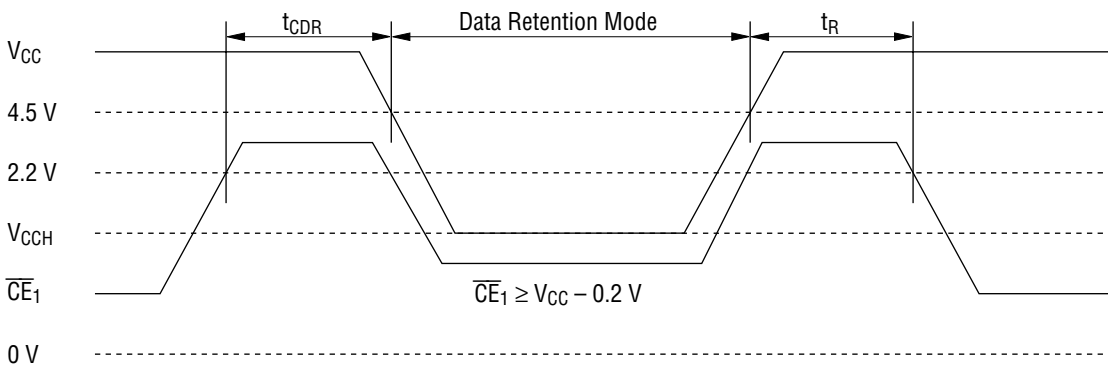
- Notes:
1. A write cycle occurs during the overlap of  $\overline{CE}_1 = "L"$ ,  $CE_2 = "H"$  and  $\overline{WE} = "L"$ .
  2.  $\overline{OE}$  may be either of "H" or "L" in the write cycle.
  3.  $t_{AS}$  is specified from  $\overline{CE}_1 = "L"$ ,  $CE_2 = "H"$  or  $\overline{WE} = "L"$ , whichever occurs last.
  4.  $t_{WP}$  is an overlap time of  $\overline{CE}_1 = "L"$ ,  $CE_2 = "H"$  and  $\overline{WE} = "L"$ .
  5.  $t_{WR}$ ,  $t_{DS}$  and  $t_{DH}$  are specified from  $\overline{CE}_1 = "H"$ ,  $CE_2 = "L"$  or  $\overline{WE} = "H"$ , whichever occurs first.
  6.  $t_{WHZ}$  is specified by the time when DATA output is floating, not defined by the output level.
  7. When I/O pins are in the output mode, don't apply the inverted input signal to the output pins.

Data Retention Characteristics

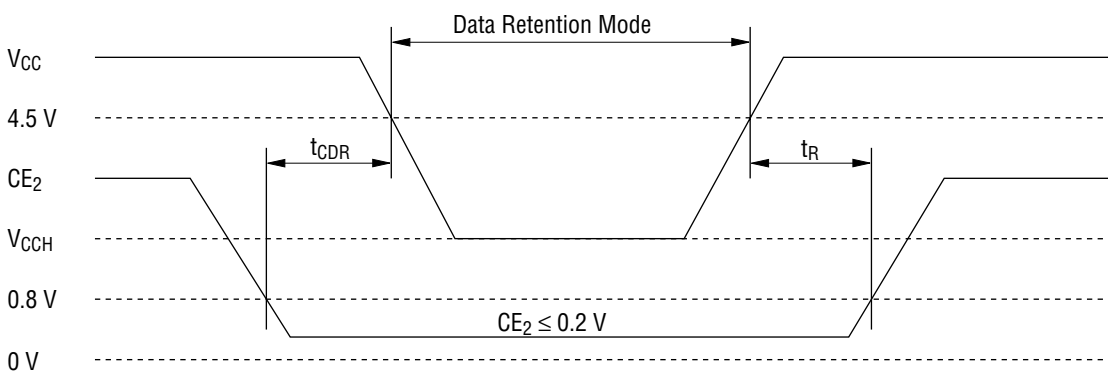
(Ta = 0°C to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Data Retention Power Supply Voltage	V <sub>CCH</sub>	$\overline{CE}_1 \geq V_{CC} - 0.2 V$ , $CE_2 \geq V_{CC} - 0.2 V$ or $0 V \leq CE_2 \leq 0.2 V$ , $V_{IN} = 0$ to $V_{CC}$	2.0	—	—	V
Data Retention Power Supply Current	I <sub>CCH</sub>	$V_{CC} = 3 V$ , $V_{IN} = 0$ to $V_{CC}$ , $\overline{CE}_1 \geq V_{CC} - 0.2 V$ , $CE_2 \geq V_{CC} - 0.2 V$ or $0 V \leq CE_2 \leq 0.2 V$	—	—	500	μA
Chip Deselect to Data Retention Time	t <sub>CDR</sub>	—	0	—	—	ns
Operation Recovery Time	t <sub>R</sub>	—	5	—	—	ms

**$\overline{CE}_1$  Control**

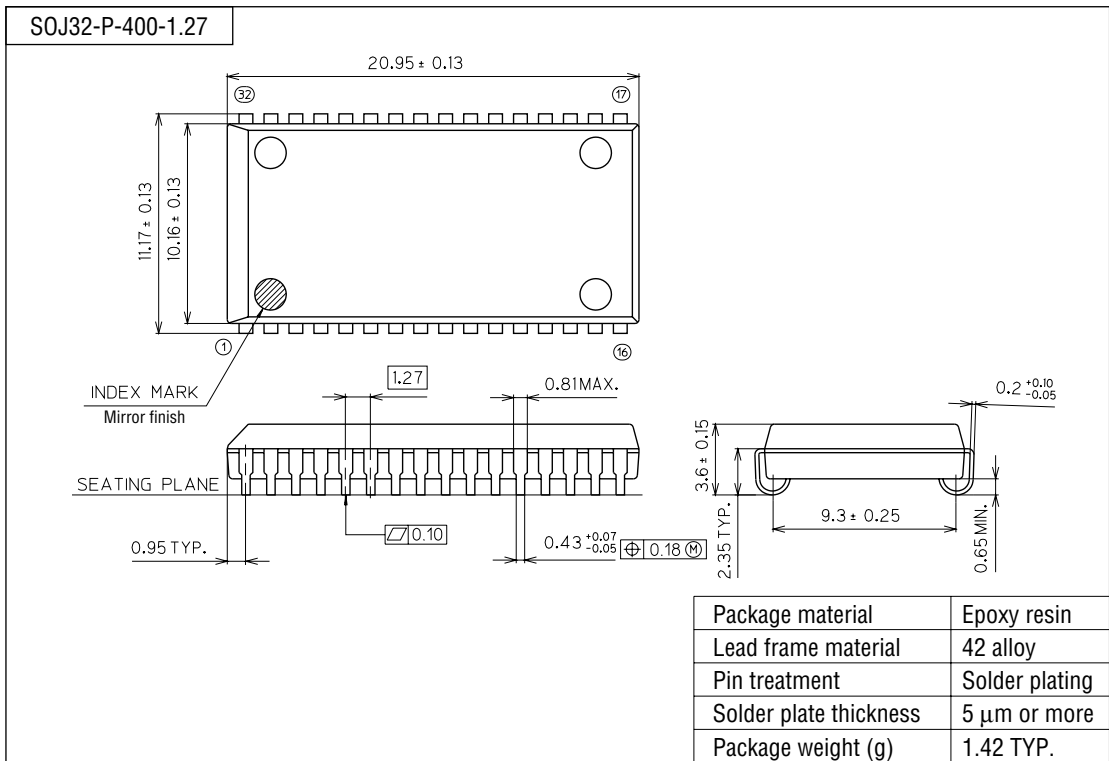


**CE<sub>2</sub> Control**



**PACKAGE DIMENSIONS**

(Unit : mm)



**Notes for Mounting the Surface Mount Type Package**

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).