

# FAST 54F251 Multiplexer

8-Input Multiplexer (3-State)  
Product Specification

Military  
Logic Products

## FEATURES

- High-speed 8-to-1 multiplexing
- True and complement outputs
- Both outputs are 3-State for further multiplexer expansion

## DESCRIPTION

The 'F251 is a logical implementation of a single-pole, 8-position switch with the state of three Select inputs ( $S_0, S_1, S_2$ ) controlling the switch position. Assertion ( $Y$ ) and Negation ( $\bar{Y}$ ) outputs are both provided. The Output Enable input ( $\bar{OE}$ ) is active LOW.

Both outputs are in the HIGH impedance (HIGH Z) state when the output enable is HIGH, allowing multiplexer expansion by tying the outputs of up to 128 devices together. All but one device must be in the HIGH impedance state to avoid high currents that would exceed the maximum ratings, when the outputs of the 3-State devices are tied together. Design of the output enable signals must ensure there is no overlap in the active LOW portion of the enable voltages.

## ORDERING INFORMATION

PACKAGES	ORDER CODE
Ceramic DIP	54F251/BEA
Ceramic Flat Pack	54F251/BFA
Ceramic LLCC	54F251/B2C

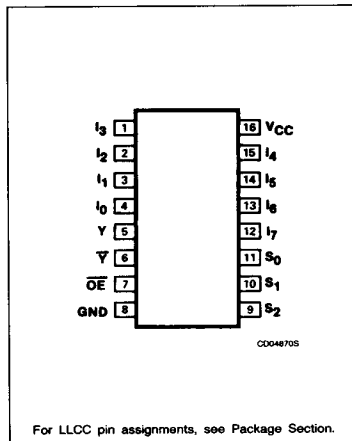
## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I_0 - I_7$	Data inputs	1.0/1.0	20 $\mu$ A/0.6mA
$S_0 - S_2$	Select inputs	1.0/1.0	20 $\mu$ A/0.6mA
$\bar{OE}$	3-State output enable input (active LOW)	1.0/1.0	20 $\mu$ A/0.6mA
$Y, \bar{Y}$	3-State output 3-State output inverted	150/33	3.0mA/20mA

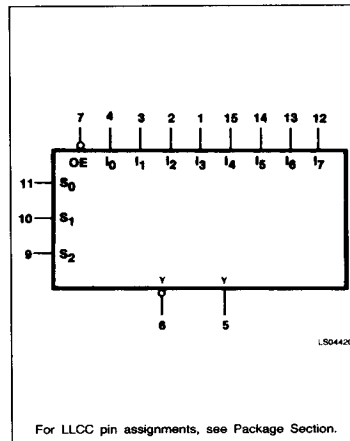
### NOTE:

One (1.0) FAST Unit Load is defined as: 20 $\mu$ A in the HIGH state and 0.6mA in the LOW state.

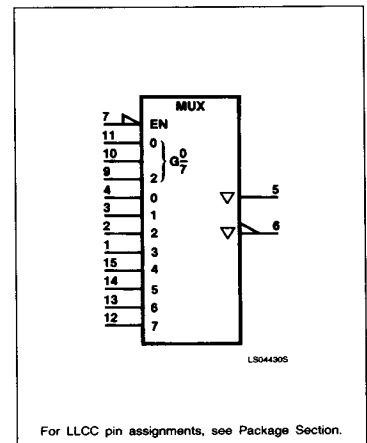
## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



May 30, 1986

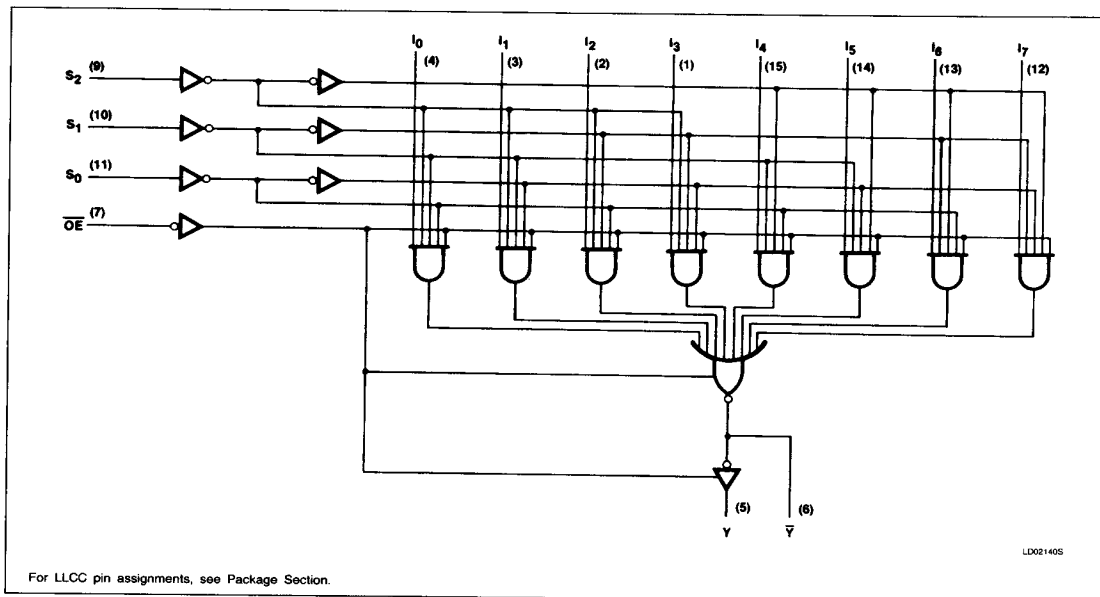
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## LOGIC DIAGRAM



## FUNCTION TABLE

INPUTS												OUTPUTS	
OE	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	I <sub>0</sub>	I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	I <sub>4</sub>	I <sub>5</sub>	I <sub>6</sub>	I <sub>7</sub>	Y-bar	Y
H	X	X	X	X	X	X	X	X	X	X	X	(Z)	(Z)
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	H	X	X	X	X	X	X	X	H	L
L	L	L	H	L	X	X	X	X	X	X	X	L	H
L	L	L	H	L	X	H	X	X	X	X	X	L	H
L	L	L	H	H	X	X	L	X	X	X	X	H	L
L	L	L	H	H	X	X	H	X	X	X	X	L	L
L	L	H	L	L	X	X	X	X	X	X	X	L	L
L	L	H	L	L	X	X	X	H	X	X	X	H	L
L	L	H	L	H	X	X	X	X	L	X	X	L	L
L	L	H	H	L	X	X	X	X	H	X	X	L	L
L	L	H	H	L	X	X	X	X	X	L	X	H	L
L	L	H	H	L	X	X	X	X	X	H	X	L	L
L	L	H	H	H	X	X	X	X	X	X	L	H	L
L	H	X	X	X	X	X	X	X	X	X	H	L	L
L	H	L	X	X	X	X	X	X	X	X	X	L	L
L	H	L	H	X	X	X	X	X	X	X	X	L	L
L	H	H	X	X	X	X	X	X	X	X	X	L	L
L	H	H	L	X	X	X	X	X	X	X	X	L	L
L	H	H	H	X	X	X	X	X	X	X	X	L	L
L	H	H	H	X	X	X	X	X	X	X	X	L	L

H = HIGH voltage level  
 L = LOW voltage level  
 X = Don't care  
 (Z) = HIGH impedance (off) state

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**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5 to +7.0	V
V <sub>I</sub>	Input voltage range	-0.5 to +7.0	V
I <sub>I</sub>	Input current range	-30 to +5	mA
V <sub>O</sub>	Voltage applied to output in HIGH output state range	-0.5 to +V <sub>CC</sub>	V
I <sub>O</sub>	Current applied to output in LOW output state	40	mA
T <sub>STG</sub>	Storage temperature range	-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	HIGH-level input voltage	2.0			V
V <sub>IL</sub>	LOW-level input voltage			0.8	V
I <sub>IK</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	HIGH-level output current			-3.0	mA
I <sub>OL</sub>	LOW-level output current			20	mA
T <sub>A</sub>	Operating free-air temperature range	-55		+125	°C

**DC ELECTRICAL CHARACTERISTICS** (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>	54F251			UNIT
			Min	Typ <sup>2</sup>	Max	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX V <sub>IH</sub> = MIN, I <sub>OH</sub> = MAX	2.4			V
V <sub>OL</sub>	LOW-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX V <sub>IH</sub> = MIN, I <sub>OL</sub> = MAX		0.35	0.50	V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>		-0.73	-1.2	V
I <sub>IH2</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V			100	μA
I <sub>IH1</sub>	HIGH-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V		1	20	μA
I <sub>IL</sub>	LOW-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V		-0.4	-0.6	mA
I <sub>OZH</sub>	Off-state output current, HIGH-level voltage applied	V <sub>CC</sub> = MAX, V <sub>IH</sub> = MIN, V <sub>O</sub> = 2.7V			50	μA
I <sub>OZL</sub>	Off-state output current, LOW-level voltage applied	V <sub>CC</sub> = MAX, V <sub>IH</sub> = MIN, V <sub>O</sub> = 0.5V		-2	-50	μA
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>	V <sub>CC</sub> = MAX	-60	-80	-150	mA
I <sub>CC</sub>	Supply current <sup>4</sup> (total)	I <sub>CC</sub> ON		15	24	mA
		I <sub>CC</sub> OFF		16	26	mA

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.
- I<sub>CC</sub> is measured with V<sub>CC</sub> = MAX, Select and Data inputs at ≥ 4.0V, and  $\overline{OE}$  ground for output ON conditions; V<sub>CC</sub> = MAX, Data inputs and the  $\overline{OE}$  at ≥ 4.0V for outputs OFF condition. I<sub>CC</sub> is measured with outputs open.

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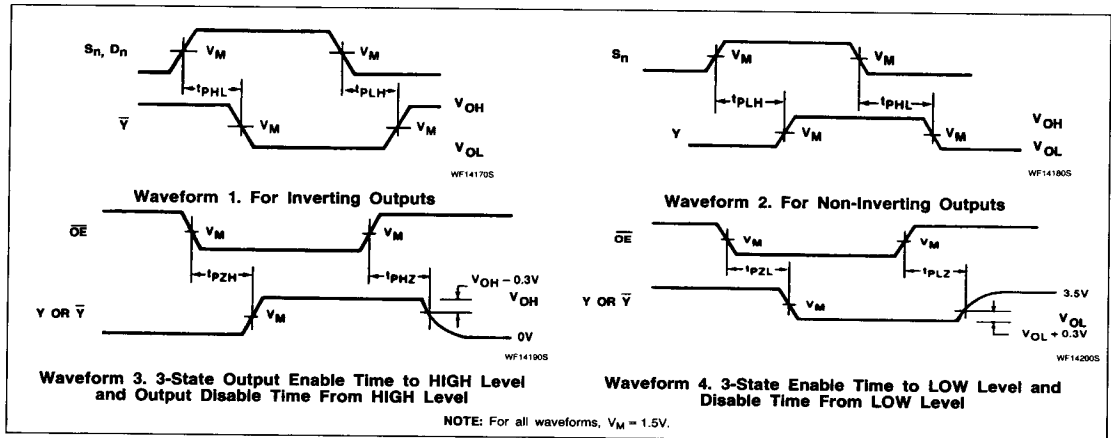
# FAST 54F251

## AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω			T <sub>A</sub> = -55°C to +125°C <sup>5</sup> V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω		
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay S <sub>n</sub> to Y	Waveform 2	4.5 4.0	9.6 6.9	9.5 9.0	3.5 4.0	13.0 11.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay S <sub>n</sub> to $\bar{Y}$	Waveform 1	3.5 1.5	5.9 5.7	9.0 7.5	3.5 1.5	12.5 9.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay I <sub>n</sub> to Y	Waveform 2	3.0 3.0	7.2 5.1	6.0 6.5	2.5 3.0	9.5 8.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay I <sub>n</sub> to $\bar{Y}$	Waveform 1	2.5 1.0	4.1 3.0	6.0 3.5	2.0 1.0	8.5 5.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time to HIGH or LOW level $\bar{OE}$ to Y	Waveform 3	4.0 3.5	6.9 6.0	13.0 8.0	4.0 3.5	16.0 10.0	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time to HIGH or LOW level $\bar{OE}$ to $\bar{Y}$	Waveform 4	4.0 4.0	5.4 6.4	8.0 8.5	5.0 3.5	10.0 10.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time from HIGH or LOW level $\bar{OE}$ to $\bar{Y}$	Waveform 3	2.5 2.0	5.0 3.2	7.0 7.5	2.0 2.0	9.0 11.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time from HIGH or LOW level $\bar{OE}$ to Y	Waveform 4	2.5 3.0	4.7 3.5	6.5 8.0	2.0 2.5	8.0 11.5	ns

5. These parameters are guaranteed, but not tested.

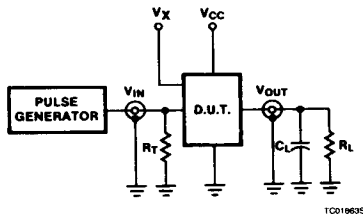
## AC WAVEFORMS



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## TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs

### SWITCH POSITION

TEST	SWITCH
$t_{PLZ}$	closed
$t_{PZL}$	closed
All other	open

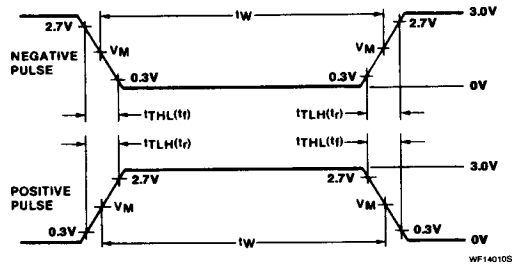
### DEFINITIONS

$R_L$  = Load resistor; see AC CHARACTERISTICS for value.

$C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

$V_X$  = Unclocked pins must be held at:  $\leq 0.8V$ ,  $\geq 2.7V$  or open per function table.



$V_M = 1.5V$

### Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS			
	Rep. Rate	Pulse Width	$t_{TLH}$	$t_{THL}$
54F	1MHz	500ns	$\leq 2.5ns$	$\leq 2.5ns$