Description

The SK12430 is a general purpose synthesized clock source. Its internal VCO will operate over a range of frequencies from 400 to 800MHz. The differential PECL output can be configured to be the VCO frequency divided by 1, 2, 4 or 8. With the output configured to divide the VCO frequency by 2, and with a 16.000MHz external quartz crystal used to provide the reference frequency, the output frequency can be specified in 1MHz steps. The PLL loop filter is fully integrated so that no external components are required. The synthesizer output frequency is configured using a parallel or serial interface.

The internal oscillator uses the external quartz crystal as the basis of its frequency reference. The output of the reference oscillator is divided by 16 before being sent to the phase detector. With a 16MHz crystal, this provides a reference frequency of 1MHz. Although this data sheet illustrates functionality only for a 16MHz crystal, any crystal in the 10-20MHz range can be used.

The VCO within the PLL operates over a range of 400 to 800 MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The output of this loop divider is applied to the phase detector.

The phase detector and loop filter attempt to force the VCO output frequency to be M X 2 times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve loop lock. (N divider) is configured through either the serial of the parallel interfaces and can provide one of four division ratios (1, 2, 4 or 8). This divider extends performance of the part while providing a 50% duty cycle.

The output driver is driven differentially from the output divider and is capable of driving a pair of transmission lines terminated in 50Ω to V_{CC} - 2.0V. The positive reference for the output driver and the internal logic is separated from the power supply for the phase-locked loop to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[8:0] and N[1:0] inputs to configure the internal counters. Normally, on system reset, the P_LOAD input is held LOW until sometime after power becomes valid.. On the LOW -to-HIGH transition of P_LOAD, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[8:0] and N[1:0] inputs to reduce component count in the application of the chip.

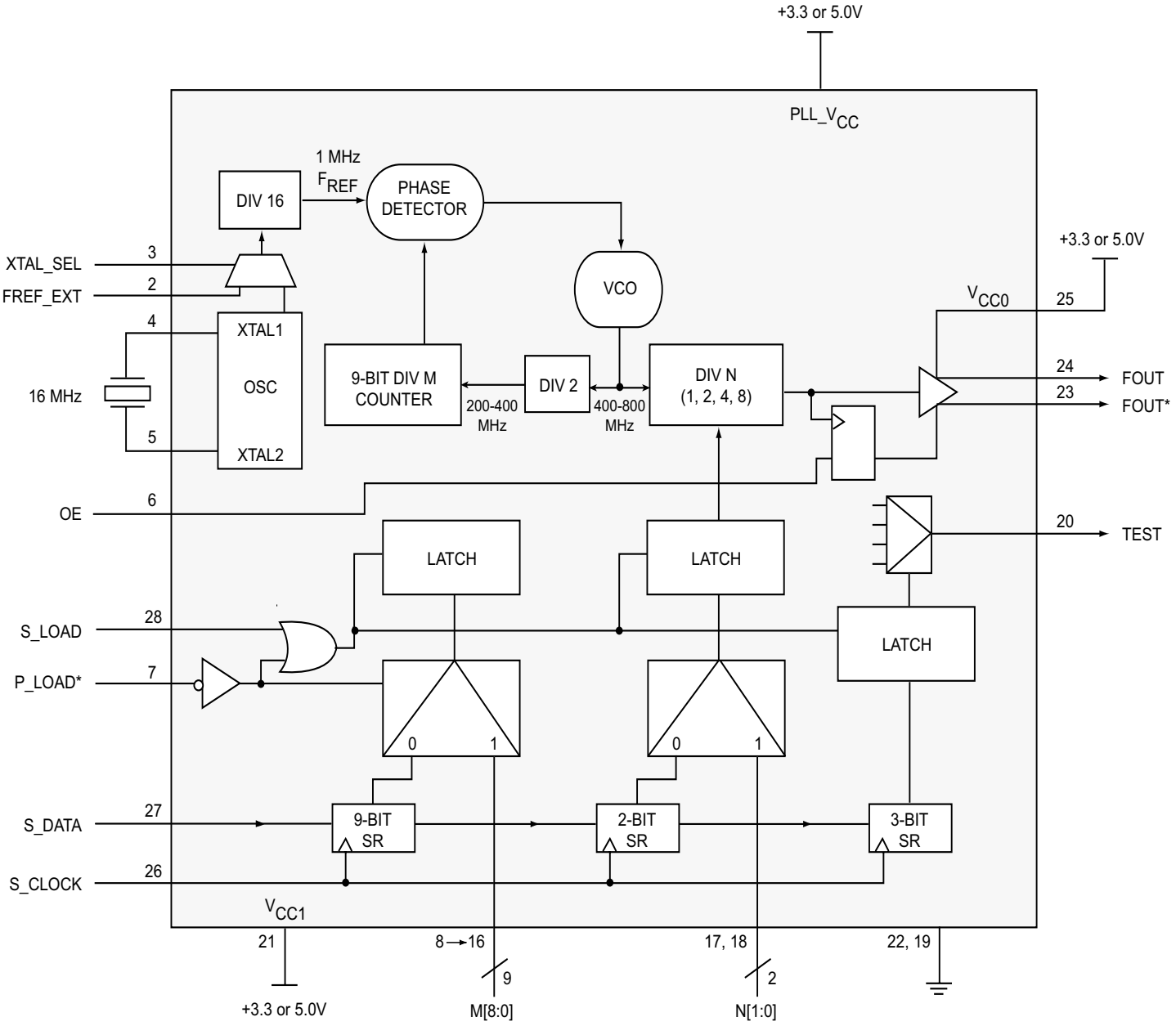
The serial interface centers on a fourteen bit shift register. The shift register shifts once per rising edge of the S_Clock input. The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[8:0] and N[1:0] inputs to configure the internal counters. Normally, on system reset, the P_LOAD input is held LOW until sometime after power becomes valid.. On the LOW -to-HIGH transition of P_LOAD, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[8:0] and N[1:0] inputs to reduce component count in the application of the chip.

The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. See the programming section for more information.

Features

- 50 to 800MHz Differential PECL Outputs
- ±25ps Peak-to-Peak Outputs
- Fully Integrated Phase-Locked Loop
- Minimal Frequency Over-Shoot
- Serial 3-Wire Interface
- Parallel Interface for Power-Up
- Quartz Crystal Interface
- 28-Lead PLCC Package
- Operates from 3.3V or 5.0V Power Supply
- ESD Protection of >4000V

Functional Block Diagram

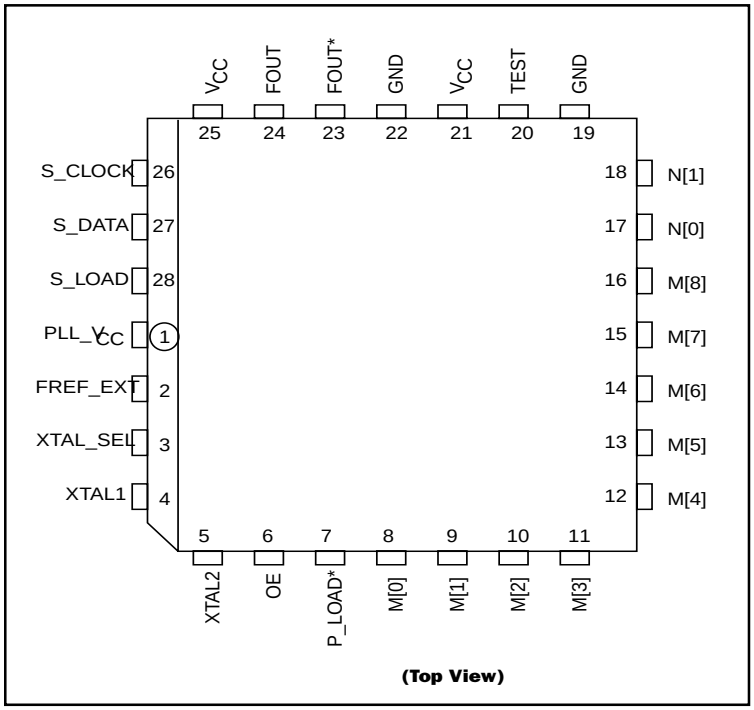


Pin Descriptions

Pin Name	Function
Inputs	
XTAL1, XTAL2	These pins form an oscillator when connected to an external series-resonant crystal.
S_LOAD (Int. Pull-down)	This pin loads the configuration latches with the contents of the shift registers. The latch will be transparent when this signal is HIGH, thus the data must be stable on the HIGH-to-LOW transition of S_LOAD for proper operation.
S_DATA (Int. Pull-down)	This pin acts as the data input to the serial configuration shift registers.
S_CLOCK (Int. Pull-down)	This pin serves to clock the serial configuration shift registers. Data from S_DATA is sampled on the rising edge.
P_LOAD* (Int. Pull-up)	This pin loads the configuration latches with the contents of the parallel inputs. The latches will be transparent when this signal is LOW, thus the parallel data must be stable on the LOW-to-HIGH transition of P_LOAD* for proper operation. P_LOAD* is state sensitive.
M[8:0] (Int. Pull-up)	These pins are used to configure the PLL loop divider. They are sampled on the LOW-to-HIGH transition of P_LOAD*. M[8] is the MSB, M[0] is the LSB.
N[1:0] (Int. Pull-up)	These pins are used to configure the output divider modulus. They are sampled on the LOW-to-HIGH transition of P_LOAD*.
OE (Int. Pull-up)	Active HIGH Output Enable. The Enable is synchronous to eliminate possibility of runt pulse generation of the F_{OUT} output.
Outputs	
F_{OUT}, F_{OUT}	These differential positive-referenced ECL signals (PECL) are the output of the synthesizer.
TEST	The function of this output is determined by the serial configuration bits T[2:0]. The output is single-ended ECL.
Power	
V_{CC}	This is the positive supply for the internal logic and the output buffer of the chip, and is connected to +3.3V or 5.0V (V_{CC} = PLL_V_{CC}). Current drain through $V_{CC} \cong$ 85 mA.
PLL_V_{CC}	This is the positive supply for the PLL, and should be as noise-free as possible for low-jitter operation. This supply is connected to +3.3V or 5.0V (V_{CC} = PLL_V_{CC}). Current drain through PLL_$V_{CC} \cong$ 15 mA.
GND	These pins are the negative supply for the chip and are normally all connected to ground.
Other	
FREF_EXT (Int. Pulldown)	LVCMOS/CMOS input which can be used as the PLL reference.
XTAL_SEL (Int. Pullup)	LVCMOS/CMOS input that selects between the crystal and the FREF_EXT source for the PLL reference signal. A HIGH selects the crystal input.

N[1:0]	Output Division
0 0	2
0 1	4
1 0	8
1 1	1

Pin Descriptions *(continued)*



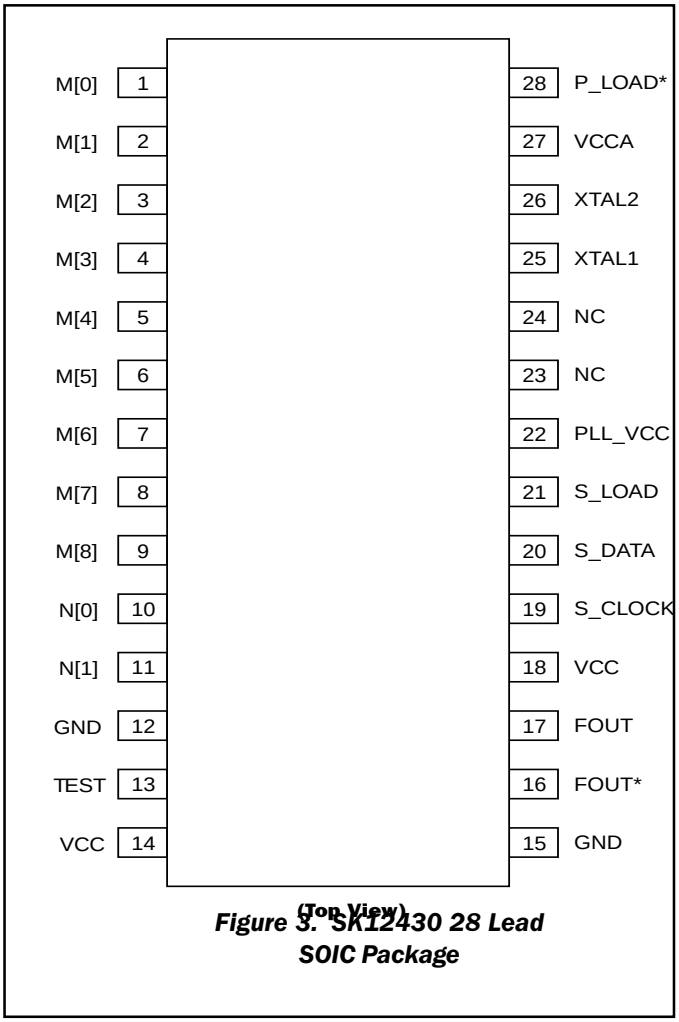


Figure 3. SK12430 28 Lead SOIC Package

Input	0	1
XTAL_SEL	FREF_EXT	XTAL
OE	Disabled	Enabled

Application Information

Programming Interface

The serial interface centers on a fourteen bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH-to-LOW edge of the S_LOAD input. See the programming section for more information.

Programming the device amount to properly configuring the internal dividers to produce the desired frequency at the outputs. The output frequency can by represented by this formula:

$$FOUT = (FXTAL \div 16) \times M \times 2 \div N \quad (1)$$

Where F_{XTAL} is the crystal frequency, M is the loop divider modulus, and N is the output divider modulus. Note that it is possible to select values of M such that the PLL is unable to achieve loop lock. To avoid this, always make sure that M is selected to be $200 \leq M \leq 400$ for any input reference.

Assuming that a 16MHz reference frequency is used, the above equation reduces to:

$$FOUT = 2 \times M \div N$$

Substituting the four values for N (1, 2, 4, 8) yields:

N	FOUT	OUTPUT FREQUENCY RANGE
1	2 X M	400 - 800 MHz
2	M	200 - 400 MHz
4	M ÷ 2	100 - 200 MHz
8	M ÷ 4	50 - 100 MHz

From these ranges, the user will establish the value of N required, then the value of M can be calculated based upon the appropriate equation above. For example, if an output frequency of 131 MHz was desired, the following steps would be taken to identify the appropriate M and N values. 131MHz falls within the frequency range set by an N value of 4 so N [1:0] = 01. For N = 4, FOUT - M ÷ 2 X FOUT. Therefore, M = 131 X 2 = 262, so M[8:0] = 100000110.

Following this same procedure, a user can generate any whole frequency desired between 50 and 800 MHz. Note that for n> 2 fractional values of FOUT can be realized. The size of the programmable frequency steps (and thus the indicator of the fractional output frequencies
achievable) will be equal to FXTAL ÷ 8 ÷ N. For input reference frequencies other than 16MHz, the set of appropriate equations can be deduced from equation 1. For computer applications, another useful frequency base would be 16.666MHz reference, the following M and N values would be used:

$$FOUT = 16.666 \div 16 \times M \times 2 \div N = 1.04166 \times M \times 2 \div N$$

$$\text{Let } N = 4,\ M = 133.333 \div 1.04166 \times 2 = 256$$

The value for M falls within the constraints set for PLL stability, therefore, N[1:0] = 01 and M[8:0] = 10000000. If the value for M fell outside of the valid range, a different N value would be selected to try to move M in the appropriate direction.

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the P_LOAD* signal such that a LOW to HIGH transition will latch the information present on the M[8:0] and N[1:0] inputs into the M and N counters. When the P_LOAD* signal is LOW, the input latches will be transparent and any changes on the M[8:0] and N[1:0] inputs will affect the FOUT output pair. To use the serial port, the S_CLOCK signal samples the information on the S_DATA line and loads it into a 14 bit shift register. Note that the P_LOAD* signal must be HIGH for the serial load operation to function. The test register is loaded with the first three bits, the N register with the next two and the M register with the final eight bits of the data stream on the S_DATA input. For each register, the most significant bit is loaded first (T2, N1 and M8]. A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 3 illustrates the timing diagram for both a parallel and a serial load of the SK12430 synthesizer.

Application Information *(continued)*

M[8:0] and N[1:0] are normally specified once at a power-up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine-tune the clock as the ability to control the serial interface becomes available.

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. The T2 and TO control bits are preset to '000' when P_LOAD* is LOW so that the PECL FOUT outputs are as jitter-free as possible. Any active signal on the TEXT output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEXT output is static. The serial configuration port can be used to select one of the alternate functions for this pin.

Most of the signals available on the TEXT output pin are useful only for performance verification of the SK12430, itself. However, the PLL bypass mode may be of interest at the board level for functional debug. When T(2:0) is set to 110, the V is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the FOUT differential pair and the M counter drives the TEST output pin. In this mode, the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving FOUT directly gives the user more control on the test clocks sent through the clock tree. Figure 4 shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level, the input frequency is limited to 250MHz or less. This means the fastest the FOUT pin can be toggled via the S_CLOCK is 250MHz as the minimum divide ratio of the N counter is 1. Note that the M counter ouptu on the TEST output will not be a 50% duty cycle due to the way the divider is implemented.

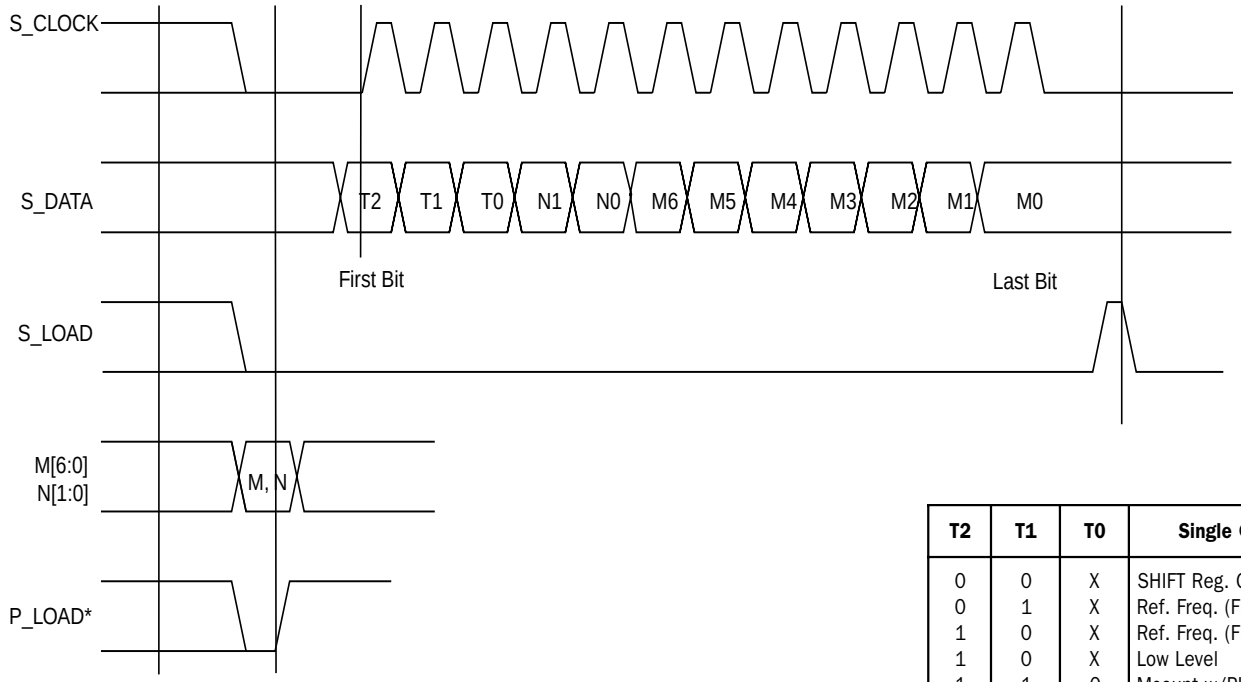


Figure 3. Timing Diagram

T2	T1	T0	Single @ TEST (Pin 20)
0	0	X	SHIFT Reg. Out
0	1	X	Ref. Freq. (FREF)
1	0	X	Ref. Freq. (FREF)
1	0	X	Low Level
1	1	0	Mcount w/PLL Bypass
1	1	1	Mcount

Note: X = Don't Care

Functional Block Diagram

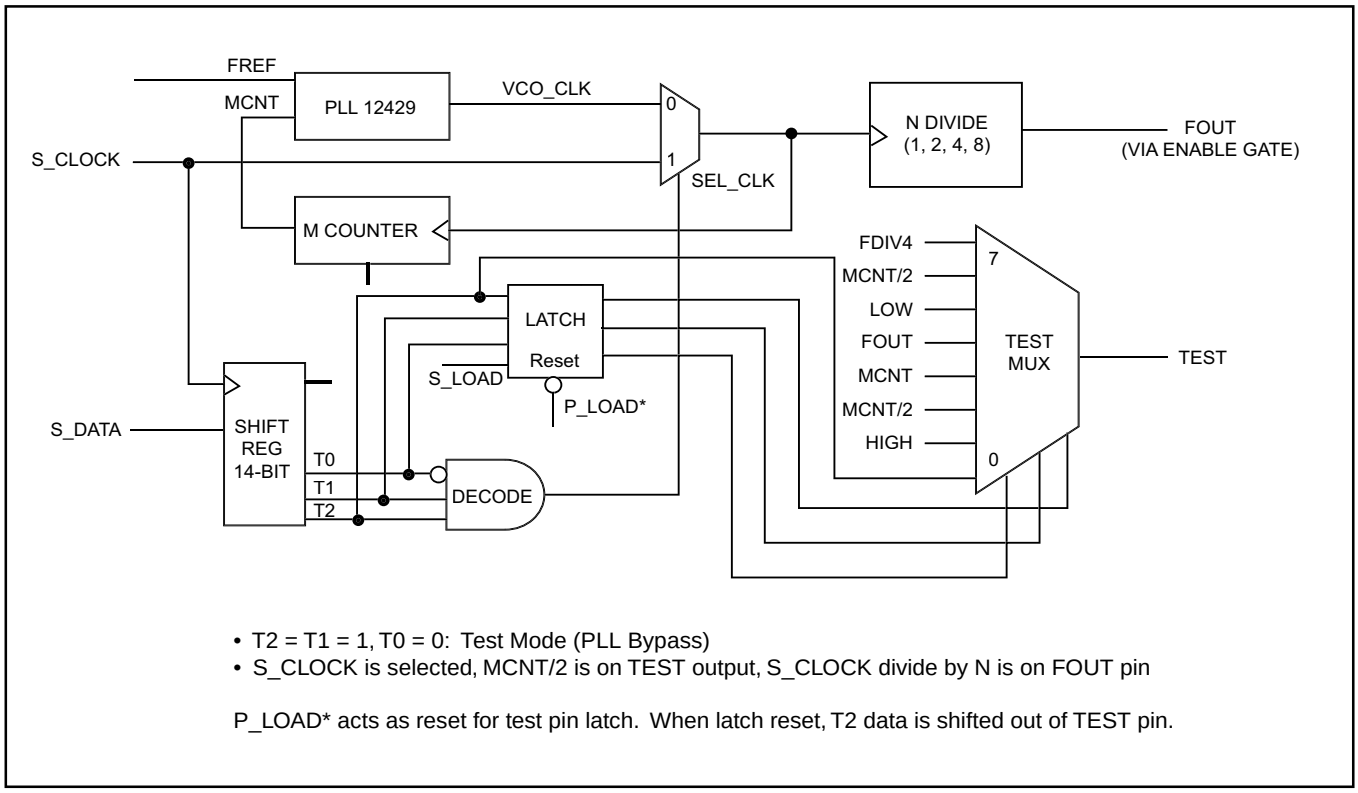


Figure 4. Serial Test Clock Block Diagram

Using the On-Board Crystal Oscillator

The SK12430 features a fully integrated on-board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self-contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the SK12430 as possible to avoid any board level parasitics. To facilitate co-location surface mount crystals are recommended, but not required.

The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Unfortunately, most crystals are characterized in a parallel resonant mode. Fortunately, there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result, a parallel resonant crystal can be used with the V with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to kHz inaccuracies. In a general computer application, this level of inaccurancy is immaterial Table 1 below specifies the performance requirements of the crystals to be used with the SK12430.

Application Information *(continued)*

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance*
Frequency Tolerance	± 75 ppm at 25°C
Frequency/Temperature Stability	± 150 ppm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7 pF
Equivalent Series Resistance (ESR)	50 to 80Ω
Correlation Drive Level	100 µΩ
Aging	5 ppm/yr (first 3 years)

*see accompanying text for series versus parallel resonant discussion.

Table 1. Crystal Specifications

Power Supply Filtering

The SK12430 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The SK12430 provides separate power supplies for the digital circuitry (V_{CC}) and the internal PLL (PLL_VCC) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest from of isolation is a power supply filter on the PLL_VCC pin for the SK12430.

Figure 5 illustrates a typical power supply filter scheme. The SK12430 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the PLL_VCC pin of the SK12430. From the data sheet, the I_{PLL_VCC} current (the current sourced through the PLL_VCC pin) is typically 15 mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the PLL_VCC pin, very little DC voltage drop can be tolerated when a 3.3V VCC supply is used. The resistor shown in Figure 5 must have a resistance of 10-15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination show ensures that a low impedance path to ground exists for rrequencies will above the bandwidth of the PLL.

A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inducto9r. A 1000µH choke will show a significant impedance at 10KHz frequencies and above. Because of the current draw and the voltage that must be maintained on the PLL_VCC pin, a low voltage that must be maintained on the PLL_VCC pin, a low DC resistance inductor is required (less than 15Ω).

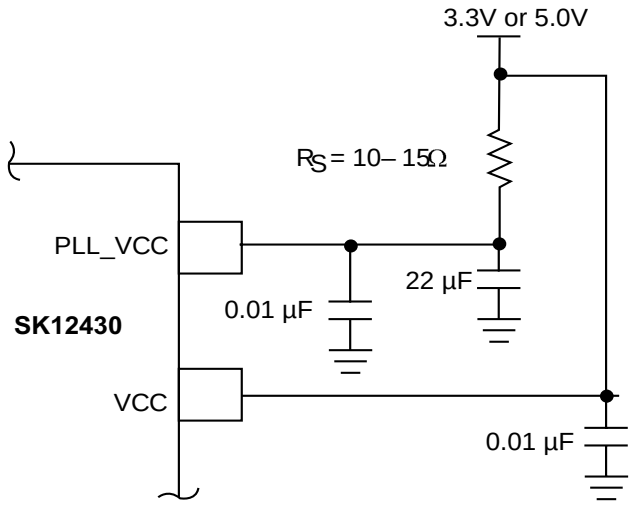


Figure 5. Power Supply Filter

Application Information *(continued)*

Generally the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering.

The SK12430 provides sub-nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 6 shows a representative board layout for the SK12430. There exists many different potential board layouts and the one pictured below is but one. The important aspect of the layout in Figure 6 is the low impedance connections between VCC and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frquencies adequate to supply the instantaneous switching current for the 1240 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should beavoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors.

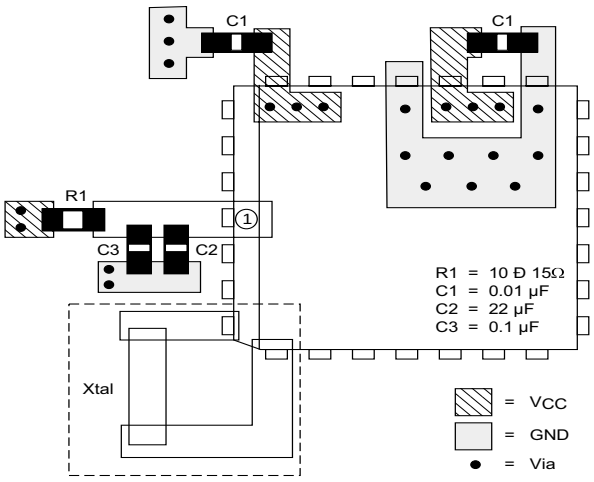


Figure 6. PCB Board Layout for the SK12430

Note: The dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on-board oscillator.

Although the SK12430 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Jitter Performance of the SK12430

The SK12430 exhibits long term and cycle-to-cycle jitter which rivals that of SAW based oscillators. This jitter performance comes with the added flexibility one gets with a synthesizer of a fixed frequency oscillator.

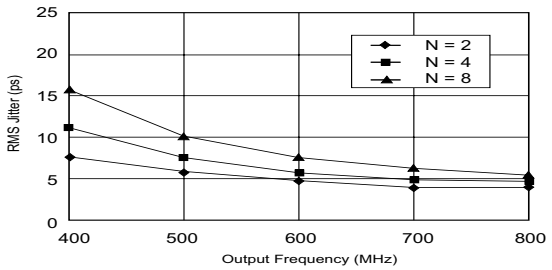


Figure 7. RMS Jitter versus VCO Frequency

Figure 7 illustrates the RMS jitter performance of the SK12430 across its specified VCO frequency range. Note that the jitter is a function of both the output frequency as well as the VCO frequency However, the VCO frequency shows a much stronger dependence. The data presented has not been compensated for trigger jitter and this fact provides a measure of guardband to the reported data. The typical method of measuring the jitter is to accumulate a large number of cycles, create a histogram of the edge placements and record peak-to-peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge.

Application Information *(continued)*

The oscilloscope cannot collect adjacent pulses, rather, it collects pulses from a very large sample of pulses. It is safe to assume that collecting pulse information in this mode will produce period jitter values somewhat larger than if consecutive cycles (cycle-to-cycle jitter) were measured. All of the jitter data reported on the SK12430 was collected in this manner.

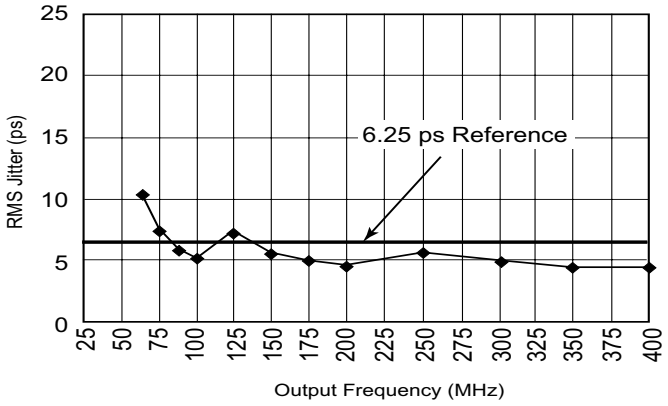


Figure 8. RMS Jitter

Figure 8 shows the jitter as a function of the output frequency. For the SK12430, this information is probably of more importance. The flat line represents an RMS jitter value that corresponds to an 8 sigma ±25ps peak-to-peak long term period jitter.

The graph shows that for output frequencies from 87.5 to 400 MHz, the jitter falls within the ±25ps peak-to-peak specification. The general trend is that as the output frequency is decreased the output edge jitter will increase.

The jitter data from Figure 7 and Figure 8 do not include the performance of the SK12430, when the output is in the divide by 1 mode. In divide by one mode, the SK12430 output jitter distribution is bimodal. Since a bimodal distribution cannot be accurately represented with an rms value, peak-to-peak values of jitter for the divide by one mode are presented.

The jitter data presented should provide users with enough information to determine the effect on their overall timing budget. The jitter performance meets the needs of most system designs while adding the flexibility of frequency margining and field upgrades. These features are not available with a fixed frequency SAW oscillator.

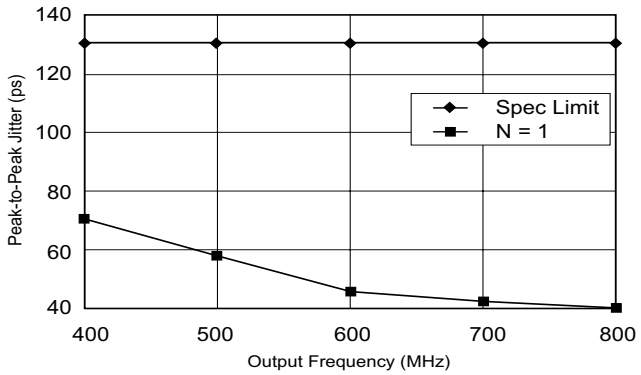


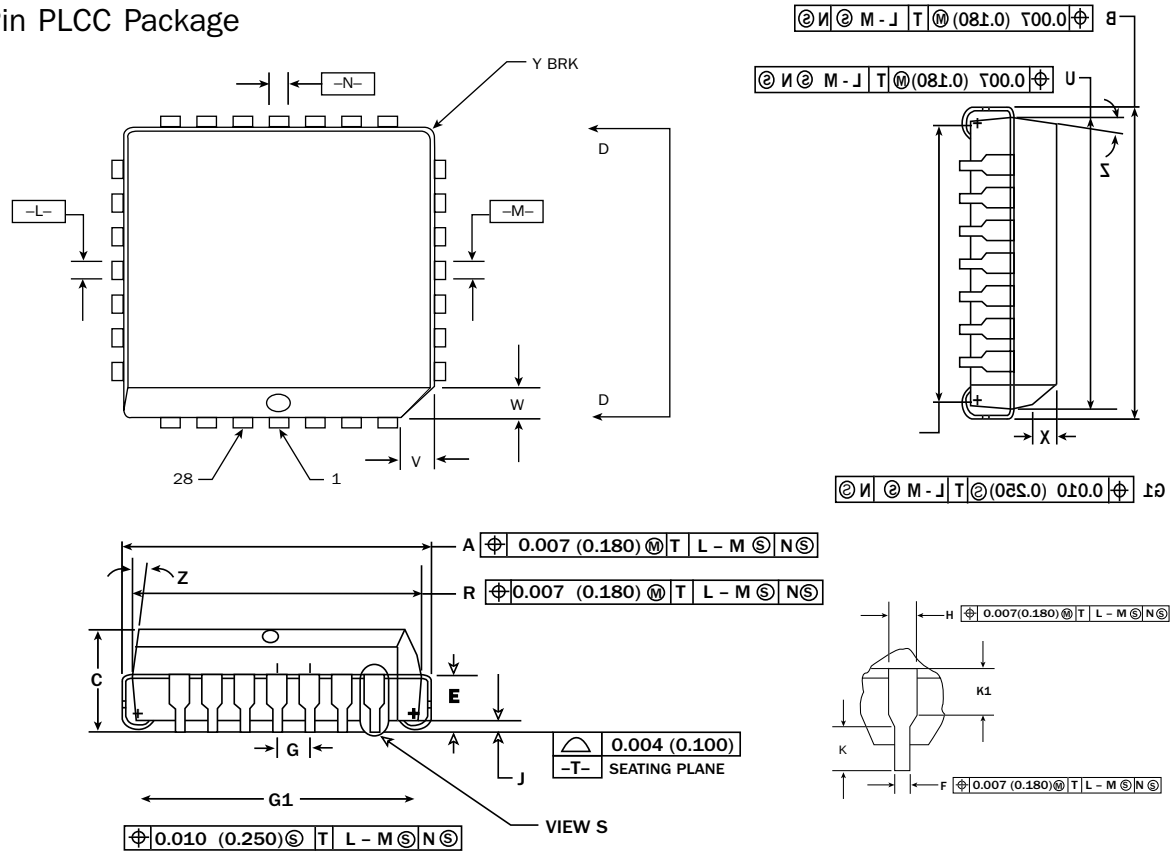
Figure 9. Peak-to-Peak Output Voltage Swing

Output Voltage Swing vs Frequency

In the divide by one mode, the output rise and fall times will limit the peak-to-peak output voltage swing. For a 400MHz output, the peak-to-peak swing of the SK12430 output will be approximately 700mV. This swing will gradually degrade as the output frequency increases, at 800MHz the output swing will be reduce to approximately 500mV. For a worst case analysis, it would be safe to assume that the SK12430 output will always generate at least a 500mV output swing. Note that most high speed ECL receivers require only a few hundred millivolt input swings for reliable operation. As a result, the output generated by the SK12430 will, under all conditions, be sufficient for clocking standard ECL devices. Note that if a larger swing is required the SK12430 could drive a clock fanout buffer like the SK100EP111.

Package Information

28 Pin PLCC Package



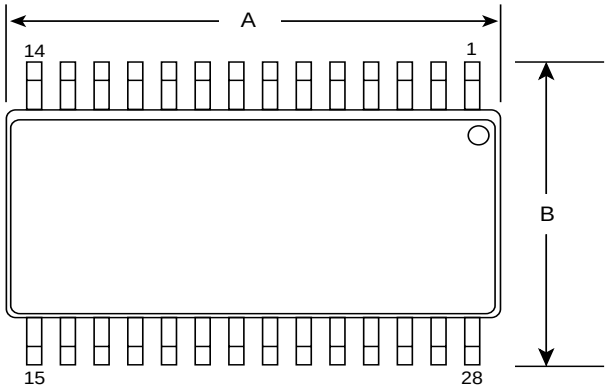
NOTES:

1. Datums -L-, -M-, and -N- determined where top of lead shoulder exits plastic body at mold parting line.
2. DIM G1, true position to be measured at Datum -T-, Seating Plane.
3. DIM R and U do not include mold flash. Allowable mold flash is 0.010 (0.250) per side.
4. Dimensioning and tolerancing per ANSI Y14.5M, 982.
5. Controlling Dimension: Inch.
6. The package top may be smaller than the package bottom by up to 0.012 (0.300). Dimensions R and U are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
7. Dimension H does not include Dambar protrusion or intrusion. The Dambar protrusion(s) shall not cause the H dimension to be greater than 0.037 (0.940). The Dambar ntrusion(s) shall not cause the H dimension to be smaller than 0.025 (0.635).

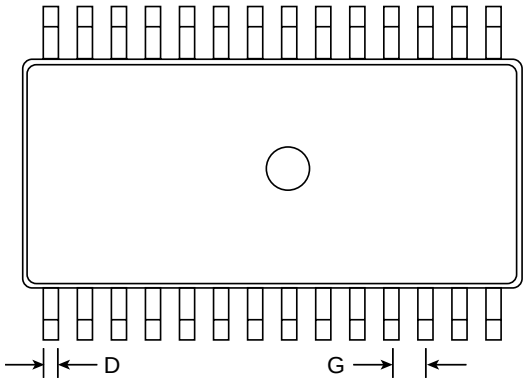
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	–	0.51	–
K	0.025	–	0.64	–
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	–	0.020	–	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	–	1.02	–

Package Information *(continued)*

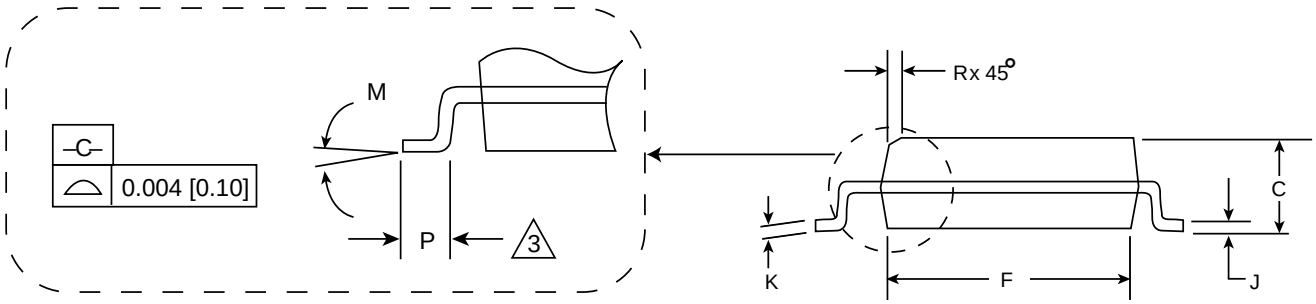
28 Pin SOIC Package



Top View



Bottom View



DIM	Millimeters	
	MIN	MAX
A	17.80	18.05
B	10.15	10.40
C	2.35	2.65
D	0.36	0.49
F	7.42	7.59
G	1.27 BSC	
J	.13	.29
K	.23	.32
M	0°	8°
P	.58	1.06
R	.25	.41

NOTES:
1. Dimensions are in millimeters.
2. Controlling dimension: Millimeters
3. Dimension does not include mold flash or protrusions, either of which shall not exceed 0.006 [0.15] per side.

Absolute Maximum Ratings Wali??

I copied 12429, but got some info out of the Product Data Book. The MCsheet doesn't have an absolute rating on it.

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0V		-0.5 to +7.0	V
V_{EE}	ECL	V_{CC} = 0V			V
V_I	PECL mode Input Voltage ECL Mode Input Voltage	V_{EE} = 0V V_{CC} = 0V	$V_I < V_{CC}$ $V_I > V_{EE}$	Book says -0.5 to +7.0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			+ 0.5	mA
TA	Operating Temperature Range			-0 to +75	^oC
T_{stg}	Storage Temperature Range			- 65 to +150	^oC
θJA	Thermal Resistance (Junction to Ambient)	LFPM LFPM	28 PLCC 28 PLCC		$^oC/W$ $^oC/W$
θJC	Thermal Resistance(Jumction to Case)	std bd	28 PLCC		$^oC/W$
V_{EE}	PECL Operating Range ECL Operating Range				V V
T_{sol}	Wave Solder				^oC

1. * Maximum Ratings are thsre values beyodg whiche device damage may occur.

DC Characteristics

DC Characteristics (VCC = 3.3V±5%)

Symbol	Characteristic	TA = 0°C			TA = 25°C			TA = 85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
V_{IH}	Input HIGH Voltage	2.2			2.2			2.2			V	
V_{IL}	Input LOW Voltage			0.8			0.8			0.8	V	
I_{IN}	Input Current			1.0			1.0			1.0	mA	
V_{OH}	Output HIGH Voltage TEST	2.5			2.5			2.5			mA	I_{OH} = –0.8 mA
V_{OL}	Output LOW Voltage TEST			0.4			0.4			0.4	V	I_{OL} = 0.8 mA
V_{OH}	Output HIGH Voltage1 FOUT, FOUT*	2.28		2.60	2.32		2.49	2.38		2.565	V	V_{CCO} = 3.3V[2,3]
V_{OL}	Output LOW Voltage1 FOUT, FOUT*	1.35		1.67	1.35		1.67	1.35		1.70	V	V_{CCO} = 3.3V[2,3]
I_{CC}	Power Supply Current V_{CC} PLL_V_{CC}		90 15	110 20		90 15	110 20		90 15	110 20	mA mA	

DC Characteristics (V_{cc} = 5.0V ±5%)

Symbol	Characteristic	TA = 0°C			TA = 25°C			TA = 85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
V_{IH}	Input HIGH Voltage	3.5			3.5			3.5			V	
V_{IL}	Input LOW Voltage			0.8			0.8			0.8	V	
I_{IN}	Input Current			1.0			1.0			1.0	mA	
V_{OH}	Output HIGH Voltage TEST	2.5			2.5			2.5			V	I_{OH} = -0.8 mA
V_{OL}	Output LOW Voltage TEST			0.4			0.4			0.4	V	I_{OL} = 0.8 mA
V_{OH}	Output HIGH Voltage[1] FOUT*, FOUT	3.98		4.30	4.02		4.19	4.08		4.265	V	V_{CCO} = 5.0V [2,3]
V_{OL}	Output LOW Voltage FOUT*, FOUT	1.41		1.76								V_{CCO} = 3.3V
I_{CC}	Power Supply Current V_{CC} PLL_V_{CC}		90 15	110 20		90 15	110 20		90 15	110 20	mA mA	

AC Characteristics

Symbol	Characteristic	Min	Max	Unit	Condition
F_{MAXI}	Maximum Input Frequency S_CLOCK XTAL Oscillator FREF_EXT	 10 10	 10 20 Note 5.	 MHz MHz MHz	Note 4
F_{MAXO}	Maximum Output Frequency VCO (Internal) FOUT	400 50	800 800	MHz MHz	Note 7
t_{LOCK}	Maximum PLL Lock Time		10	ms	
t_{jitter}	Period Deviation (Peak-to-Peak) Note 6		±25 65	ps ps	N = 2, 4, 8; Note 7 N = 1; Note 7
t_s	Setup Time S_DATA to S_CLOCK S_CLOCK to S_LOAD M, N to P_LOAD*	 20 20 20		 ns ns ns	
t_h	Hold Time S_DATA to S_CLOCK M, N to P_LOAD*	 20 20		 ns ns	
tpw_{MIN}	Minimum Pulse Width S_LOAD P_LOAD*	 50 50		 ns ns	
t_r, t_f	Output Rise/Fall FOUT	 300	 800	 ps	 20% - 80%, Note 7

1. See application information section for output level versus frequency information.
2. Output levels will vary 1:1 with V_{CCO} variation.
3. 50Ω to V_{CC} - 2.0V termination.
4. 10MHz is the maximum frequencyn to load the feedback divide registers, S_CLOCK can be switched at higher frequencies when used as a test clock in TEST_MODE 6.
5. Maximum frequency on FREF_EXT is a function of the internal M counter limitations. The phase detector can handle up to 100MHz on the input, but the M counter must reamin in the valid range of $200 \leq M \leq 400$. See the Programming Interface section on page 5 of this data sheet for more details.
6. See applications Information below for additional information.
7. 50Ω to V_{CC} - 2.0V pull-down.
8. For Standard ECL DC Specifications, refer to the Logic Family Standard DC Specification Data Sheet.
9. For part ordering description, see HPP Part Ordering Information Data Sheet.

Ordering Information

Ordering Code	Package ID	Temperature Range
SK12430PJ	28-PLCC	Industrial
SK12430PJT	28-PLCC	Industrial

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