DATA SHEET

M 65604

256 K × 4
ULTIMATE CMOS SRAM

FEATURES

- **ACCESS TIME: COMMERCIAL: 25/30/35/45 ns**
  INDUSTRIAL AND MILITARY: 25/30/35/45 ns
- **VERY LOW POWER CONSUMPTION**
  ACTIVE: 250 mW (typ)
  STANDBY: 1 µW (typ)
  DATA RETENTION: 0.5 µW (typ)
- **WIDE TEMPERATURE RANGE:**
  – 55 TO + 125 °C
- **400 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **SINGLE 5 VOLT SUPPLY**
- **EQUAL CYCLE AND ACCESS TIME**
- **GATED INPUTS:**
  NO PULL-UP/DOWN
  RESISTORS ARE REQUIRED

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INTRODUCTION

The M 65604 is a very low power CMOS static RAM organized as 262144 × 4 bits. It is manufactured using the MHS high performance CMOS technology named SCMOS.

With this process, MHS brings the solution to applications where fast computing is as mandatory as low consumption, such as aerospace electronics, portable instruments, or embarked systems.

Utilizing an array of six transistors (6T) memory cells, the M 65604 combines an extremely low standby supply current (Typical value = 0.2 µA) with a fast access time at 25 ns over the full commercial temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

Extra protection against heavy ions is given by the use of an epitaxial layer of a P substrate.

For military/space applications that demand superior levels of performance and reliability the M 65604 is processed according to the methods of the latest revision of the MIL STD 883 (class B or S) and/or ESA SCC 9000.

See 65608 for A.C. and D.C. specifications.