NEC

MOS INTEGRATED CIRCUIT
μPD44321181, 44321361

32M-BIT ZEROSB™ SRAM
FLOW THROUGH OPERATION

Description

The μPD44321181 is a 2,097,152-word by 18-bit and the μPD44321361 is a 1,048,576-word by 36-bit ZEROSB static RAM fabricated with advanced CMOS technology using full CMOS six-transistor memory cell.

The μPD44321181 and μPD44321361 are optimized to eliminate dead cycles for read to write, or write to read transitions. These ZEROSB static RAMs integrate unique synchronous peripheral circuitry, 2-bit burst counter and output buffer as well as SRAM core. All input registers are controlled by a positive edge of the single clock input (CLK).

The μPD44321181 and μPD44321361 are suitable for applications which require synchronous operation, high speed, low voltage, high density and wide bit configuration, such as buffer memory.

ZZ has to be set LOW at the normal operation. When ZZ is set HIGH, the SRAM enters Power Down State (“Sleep”). In the “Sleep” state, the SRAM internal state is preserved. When ZZ is set LOW again, the SRAM resumes normal operation.

The μPD44321181 and μPD44321361 are packaged in 100-pin PLASTIC LQFP with a 1.4 mm package thickness for high density and low capacitive loading.

Features

- Low voltage core supply: V_{DD} = 3.3 ± 0.165 V / 2.5 ± 0.125 V
- Synchronous operation
- 100 percent bus utilization
- Internally self-timed write control
- Burst read / write : Interleaved burst and linear burst sequence
- Fully registered inputs and outputs for flow through operation
- All registers triggered off positive clock edge
- 3.3V or 2.5V LVTTL Compatible : All inputs and outputs
- Fast clock access time : 7.5 ns (117 MHz)
- Asynchronous output enable : /G
- Burst sequence selectable : MODE
- Sleep mode : ZZ (ZZ = Open or Low : Normal operation)
- Separate byte write enable : /BW1 to /BW4 (μPD44321361)
  /BW1 and /BW2 (μPD44321181)
- Three chip enables for easy depth expansion
- Common I/O using three state outputs

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The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

Ordering Information

	Part number	Access Time ns	Clock Frequency MHz	Core Supply Voltage V	I/O Interface	Package
	μPD44321181GF-A75	7.5	117	3.3 ± 0.165	3.3 V or 2.5 V LVTTL	100-pin PLASTIC LQFP (14 x 20)
				2.5 ± 0.125	2.5 V LVTTL	
	μPD44321361GF-A75	7.5	117	3.3 ± 0.165	3.3 V or 2.5 V LVTTL	
				2.5 ± 0.125	2.5 V LVTTL	
<R>	μPD44321181GF-A75-A	7.5	117	3.3 ± 0.165	3.3 V or 2.5 V LVTTL	
				2.5 ± 0.125	2.5 V LVTTL	
<R>	μPD44321361GF-A75-A	7.5	117	3.3 ± 0.165	3.3 V or 2.5 V LVTTL	
				2.5 ± 0.125	2.5 V LVTTL	

<R> **Remark** Products with -A at the end of the part number are lead-free products.

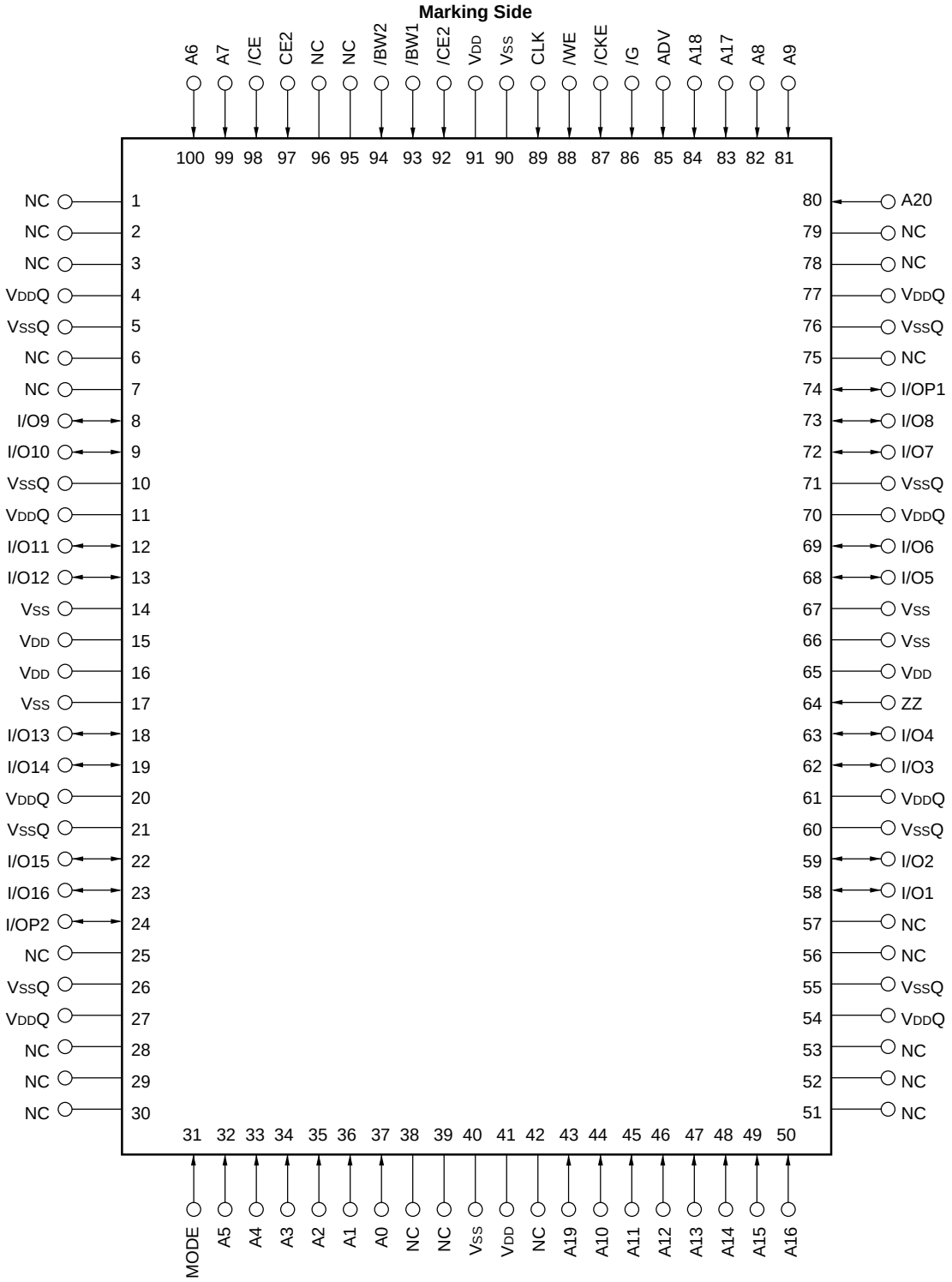
Pin Configurations

/××× indicates active low signal.

100-pin PLASTIC LQFP (14 × 20)

[μPD44321181GF]

<R> **[μPD44321181GF-A]**



Remark Refer to **Package Drawing** for the 1-pin index mark.

Pin Identifications

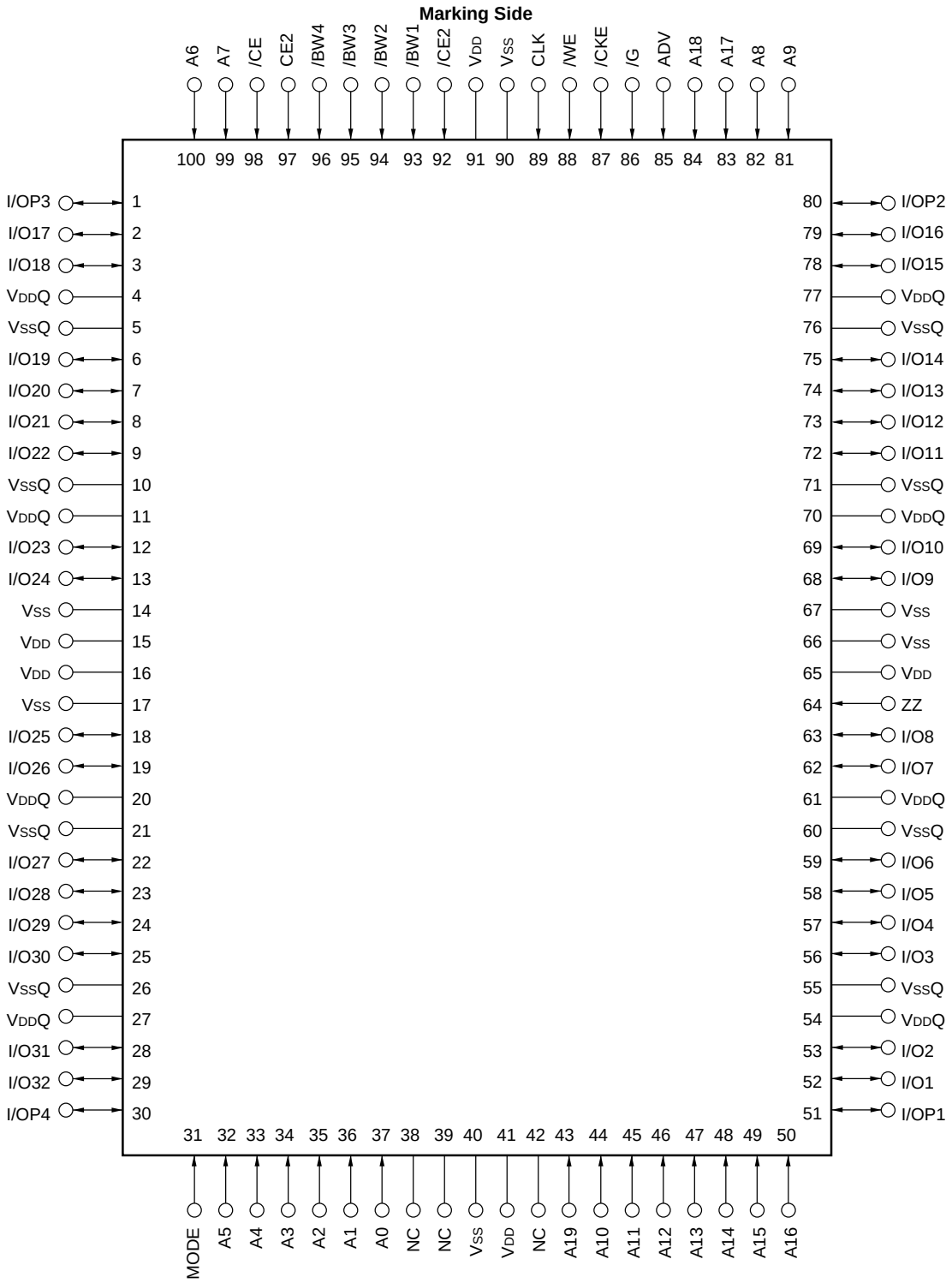
<R> **[μPD44321181GF, μPD44321181GF-A]**

Symbol	Pin No.	Description
A0 to A20	37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49, 50, 83, 84, 43, 80	Synchronous Address Input
I/O1 to I/O16	58, 59, 62, 63, 68, 69, 72, 73, 8, 9, 12, 13, 18, 19, 22, 23	Synchronous Data In, Synchronous / Asynchronous Data Out
I/OP1, I/OP2	74, 24	Synchronous Data In (Parity), Synchronous / Asynchronous Data Out (Parity)
ADV	85	Synchronous Address Load / Advance Input
/CE, CE2, /CE2	98, 97, 92	Synchronous Chip Enable Input
/WE	88	Synchronous Write Enable Input
/BW1, /BW2	93, 94	Synchronous Byte Write Enable Input
/G	86	Asynchronous Output Enable Input
CLK	89	Clock Input
/CKE	87	Synchronous Clock Enable Input
MODE	31	Asynchronous Burst Sequence Select Input Have to tied to V_{DD} or V_{SS} during normal operation
ZZ	64	Asynchronous Power Down State Input
V_{DD}	15, 16, 41, 65, 91	Power Supply
V_{SS}	14, 17, 40, 66, 67, 90	Ground
$V_{DD}Q$	4, 11, 20, 27, 54, 61, 70, 77	Output Buffer Power Supply
$V_{SS}Q$	5, 10, 21, 26, 55, 60, 71, 76	Output Buffer Ground
NC	1, 2, 3, 6, 7, 25, 28, 29, 30, 38, 39, 42, 51, 52, 53, 56, 57, 75, 78, 79, 95, 96	No Connection

100-pin PLASTIC LQFP (14 × 20)

[μPD44321361GF]

<R> **[μPD44321361GF-A]**



Remark Refer to **Package Drawing** for the 1-pin index mark.

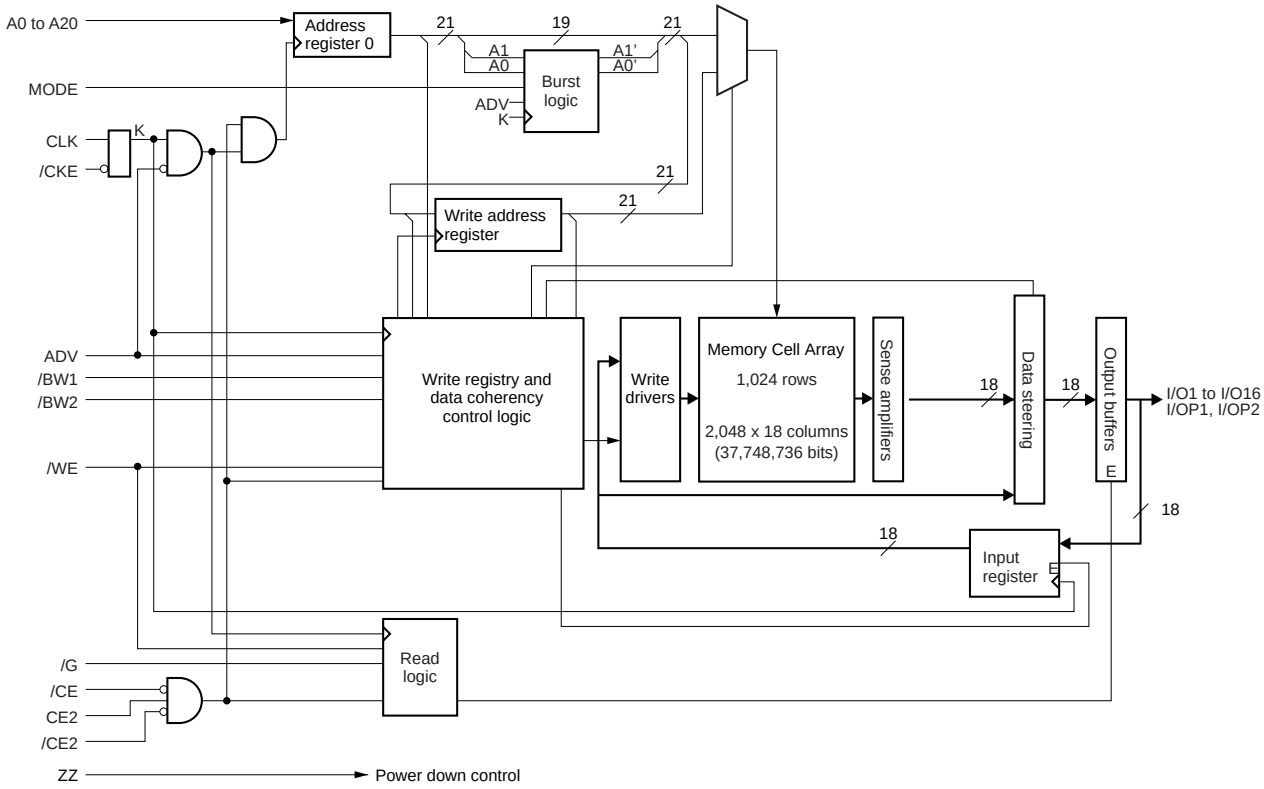
Pin Identifications

<R> **[μPD44321361GF, μPD44321361GF-A]**

Symbol	Pin No.	Description
A0 to A19	37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49, 50, 83, 84, 43	Synchronous Address Input
I/O1 to I/O32	52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29	Synchronous Data In, Synchronous / Asynchronous Data Out
I/OP1 to I/OP4	51, 80, 1, 30	Synchronous Data In (Parity), Synchronous / Asynchronous Data Out (Parity)
ADV	85	Synchronous Address Load / Advance Input
/CE, CE2, /CE2	98, 97, 92	Synchronous Chip Enable Input
/WE	88	Synchronous Write Enable Input
/BW1 to /BW4	93, 94, 95, 96	Synchronous Byte Write Enable Input
/G	86	Asynchronous Output Enable Input
CLK	89	Clock Input
/CKE	87	Synchronous Clock Enable Input
MODE	31	Asynchronous Burst Sequence Select Input Have to tied to V_{DD} or V_{SS} during normal operation
ZZ	64	Asynchronous Power Down State Input
V_{DD}	15, 16, 41, 65, 91	Power Supply
V_{SS}	14, 17, 40, 66, 67, 90	Ground
$V_{DD}Q$	4, 11, 20, 27, 54, 61, 70, 77	Output Buffer Power Supply
$V_{SS}Q$	5, 10, 21, 26, 55, 60, 71, 76	Output Buffer Ground
NC	38, 39, 42	No Connection

Block Diagrams

[μPD44321181]



Burst Sequence

[μPD44321181]

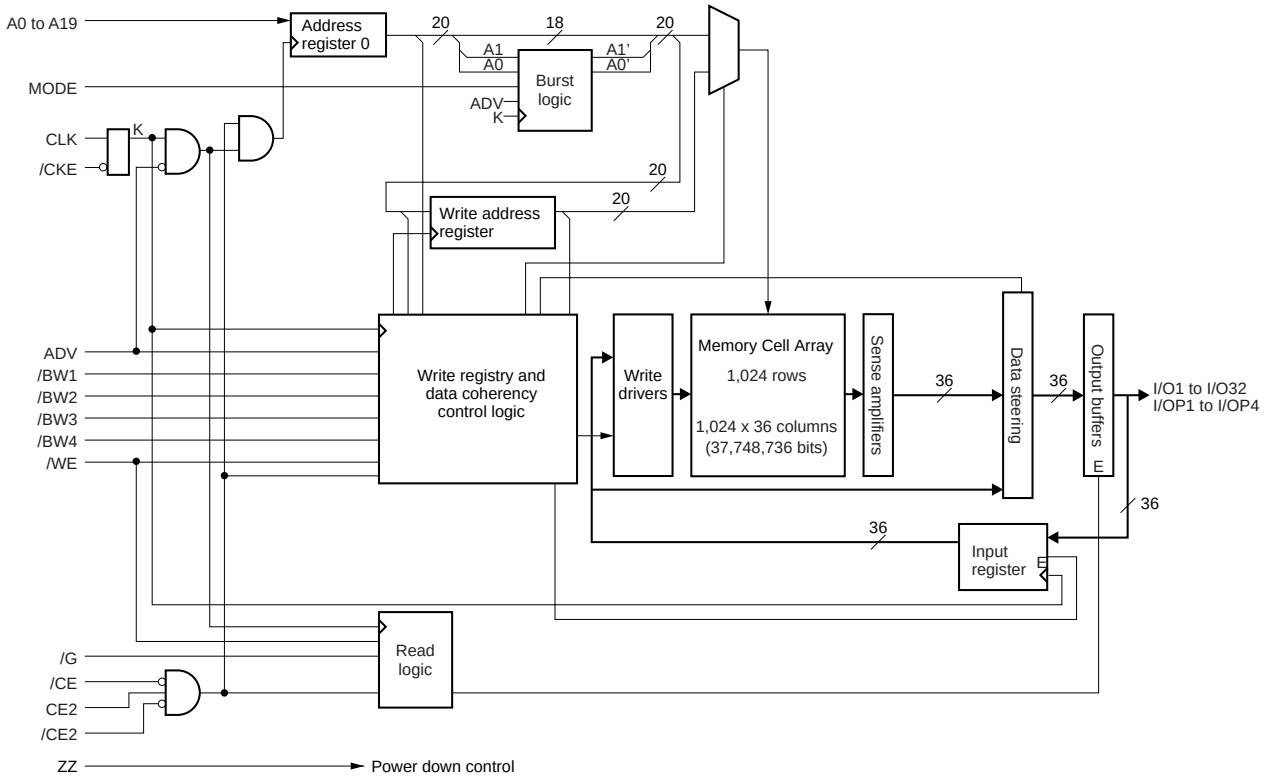
Interleaved Burst Sequence Table (MODE = V_{DD})

External Address	A20 to A2, A1, A0
1st Burst Address	A20 to A2, A1, /A0
2nd Burst Address	A20 to A2, /A1, A0
3rd Burst Address	A20 to A2, /A1, /A0

Linear Burst Sequence Table (MODE = V_{SS})

External Address	A20 to A2, 0, 0	A20 to A2, 0, 1	A20 to A2, 1, 0	A20 to A2, 1, 1
1st Burst Address	A20 to A2, 0, 1	A20 to A2, 1, 0	A20 to A2, 1, 1	A20 to A2, 0, 0
2nd Burst Address	A20 to A2, 1, 0	A20 to A2, 1, 1	A20 to A2, 0, 0	A20 to A2, 0, 1
3rd Burst Address	A20 to A2, 1, 1	A20 to A2, 0, 0	A20 to A2, 0, 1	A20 to A2, 1, 0

[μPD44321361]



Burst Sequence

[μPD44321361]

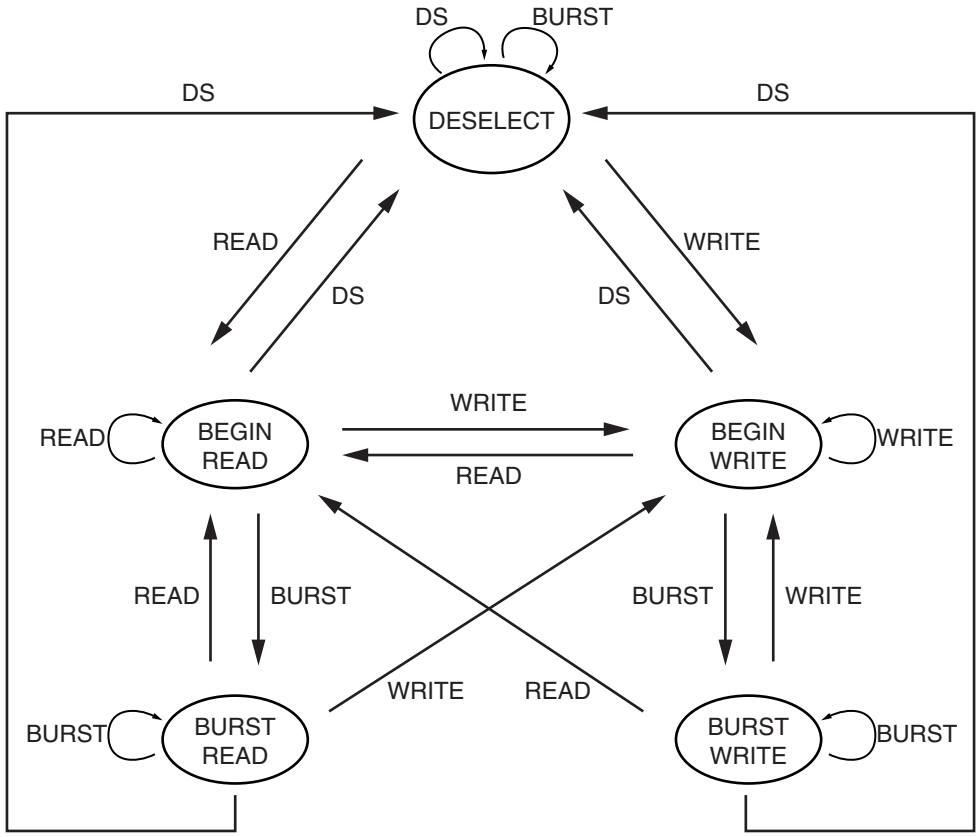
Interleaved Burst Sequence Table (MODE = V_{DD})

External Address	A19 to A2, A1, A0
1st Burst Address	A19 to A2, A1, /A0
2nd Burst Address	A19 to A2, /A1, A0
3rd Burst Address	A19 to A2, /A1, /A0

Linear Burst Sequence Table (MODE = V_{SS})

External Address	A19 to A2, 0, 0	A19 to A2, 0, 1	A19 to A2, 1, 0	A19 to A2, 1, 1
1st Burst Address	A19 to A2, 0, 1	A19 to A2, 1, 0	A19 to A2, 1, 1	A19 to A2, 0, 0
2nd Burst Address	A19 to A2, 1, 0	A19 to A2, 1, 1	A19 to A2, 0, 0	A19 to A2, 0, 1
3rd Burst Address	A19 to A2, 1, 1	A19 to A2, 0, 0	A19 to A2, 0, 1	A19 to A2, 1, 0

State Diagram



Command	Operation
DS	Deselect
Read	New Read
Write	New Write
Burst	Burst Read, Burst Write or Continue Deselect

Remarks 1. States change on the rising edge of the clock.

2. A Stall or Ignore Clock Edge cycle is not shown in the above diagram. This is because /CKE HIGH only blocks the clock (CLK) input and does not change the state of the device.

Asynchronous Truth Table

Operation	/G	I/O
Read Cycle	L	Data-Out
Read Cycle	H	High-Z
Write Cycle	×	High-Z, Data-In
Deselected	×	High-Z

Remark × : don't care

Synchronous Truth Table

Operation	/CE	CE2	/CE2	ADV	/WE	/BWs	/CKE	CLK	I/O	Address	Note
Deselected	H	×	×	L	×	×	L	L → H	High-Z	None	1
Deselected	×	L	×	L	×	×	L	L → H	High-Z	None	1
Deselected	×	×	H	L	×	×	L	L → H	High-Z	None	1
Continue Deselected	×	×	×	H	×	×	L	L → H	High-Z	None	1
Read Cycle / Begin Burst	L	H	L	L	H	×	L	L → H	Data-Out	External	
Read Cycle / Continue Burst	×	×	×	H	×	×	L	L → H	Data-Out	Next	
Write Cycle / Begin Burst	L	H	L	L	L	L	L	L → H	Data-In	External	
Write Cycle / Continue Burst	×	×	×	H	×	L	L	L → H	Data-In	Next	
Write Cycle / Write Abort	L	H	L	L	L	H	L	L → H	High-Z	External	
Write Cycle / Write Abort	×	×	×	H	×	H	L	L → H	High-Z	Next	
Stall / Ignore Clock Edge	×	×	×	×	×	×	H	L → H	–	Current	2

Notes 1. Deselect status is held until new "Begin Burst" entry.

2. If an Ignore Clock Edge command occurs during a read operation, the I/O bus will remain active (Low impedance). If it occurs during a write cycle, the bus will remain High impedance. No write operation will be performed during the Ignore Clock Edge cycle.

Remarks 1. × : don't care

2. /BWs = L means any one or more byte write enables (/BW1, /BW2, /BW3 or /BW4) are LOW.
/BWs = H means all byte write enables (/BW1, /BW2, /BW3 or /BW4) are HIGH.

Partial Truth Table for Write Enables

[μPD44321181]

Operation	/WE	/BW1	/BW2
Read Cycle	H	×	×
Write Cycle / Byte 1 (I/O [1:8], I/OP1)	L	L	H
Write Cycle / Byte 2 (I/O [9:16], I/OP2)	L	H	L
Write Cycle / All Bytes	L	L	L
Write Abort / NOP	L	H	H

Remark × : don't care

[μPD44321361]

Operation	/WE	/BW1	/BW2	/BW3	/BW4
Read Cycle	H	×	×	×	×
Write Cycle / Byte 1 (I/O [1:8], I/OP1)	L	L	H	H	H
Write Cycle / Byte 2 (I/O [9:16], I/OP2)	L	H	L	H	H
Write Cycle / Byte 3 (I/O [17:24], I/OP3)	L	H	H	L	H
Write Cycle / Byte 4 (I/O [25:32], I/OP4)	L	H	H	H	L
Write Cycle / All Bytes	L	L	L	L	L
Write Abort / NOP	L	H	H	H	H

Remark × : don't care

ZZ (Sleep) Truth Table

ZZ	Chip Status
≤ 0.2 V	Active
Open	Active
≥ V_{DD} – 0.2 V	Sleep

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		–0.5		+4.0	V
Output supply voltage	$V_{DD}Q$		–0.5		V_{DD}	V
Input voltage	V_{IN}		–0.5 Note		V_{DD} + 0.5	V
Input / Output voltage	$V_{I/O}$		–0.5 Note		$V_{DD}Q$ + 0.5	V
Operating ambient temperature	T_A		0		70	°C
Storage temperature	T_{stg}		–55		+125	°C

Note –2.0 V (MIN.) (Pulse width : 2 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (V_{DD} = 3.3 ± 0.165 V) (1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		3.135	3.3	3.465	V
2.5 V LVTTL Interface						
Output supply voltage	$V_{DD}Q$		2.375	2.5	2.9	V
High level input voltage	V_{IH}		2.0		$V_{DD}Q$ + 0.3	V
Low level input voltage	V_{IL}		–0.3 Note		+0.7	V
3.3 V LVTTL Interface						
Output supply voltage	$V_{DD}Q$		3.135	3.3	3.465	V
High level input voltage	V_{IH}		2.0		$V_{DD}Q$ + 0.3	V
Low level input voltage	V_{IL}		–0.3 Note		+0.8	V

Note –0.8 V (MIN.) (Pulse width : 2 ns)

Recommended DC Operating Conditions (V_{DD} = 2.5 ± 0.125 V) (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		2.375	2.5	2.625	V
Output supply voltage	$V_{DD}Q$		2.375	2.5	2.625	V
High level input voltage	V_{IH}		1.7		$V_{DD}Q$ + 0.3	V
Low level input voltage	V_{IL}		–0.3 Note		+0.7	V

Note –0.8 V (MIN.) (Pulse width : 2 ns)

DC Characteristics (V_{DD} = 3.3 ± 0.165 V or 2.5 ± 0.125 V)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input leakage current	I_{LI}	V_{IN} (except ZZ, MODE) = 0 V to V_{DD}	–2		+2	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to $V_{DD}Q$, Outputs are disabled.	–2		+2	μA
Operating supply current	I_{DD}	Device selected, Cycle = MAX. $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$, $I_{I/O}$ = 0 mA			290	mA
Standby supply current	I_{SB}	Device deselected, Cycle = 0 MHz, $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$, All inputs are static.			70	mA
	I_{SB1}	Device deselected, Cycle = 0 MHz, $V_{IN} \leq$ 0.2 V or $V_{IN} \geq V_{DD}$ – 0.2 V, $V_{I/O} \leq$ 0.2 V, All inputs are static.			60	
	I_{SB2}	Device deselected, Cycle = MAX. $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$			110	
Power down supply current	I_{SBZZ}	ZZ ≥ V_{DD} – 0.2 V, $V_{I/O} \leq V_{DD}Q$ + 0.2 V			60	mA
2.5 V LVTTL Interface						
High level output voltage	V_{OH}	I_{OH} = –2.0 mA	1.7			V
		I_{OH} = –1.0 mA	2.1			
Low level output voltage	V_{OL}	I_{OL} = +2.0 mA			0.7	V
		I_{OL} = +1.0 mA			0.4	
3.3 V LVTTL Interface						
High level output voltage	V_{OH}	I_{OH} = –4.0 mA	2.4			V
Low level output voltage	V_{OL}	I_{OL} = +8.0 mA			0.4	V

Capacitance (T_A = 25 °C, f = 1MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			6.0	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			8.0	pF
Clock input capacitance	C_{clk}	V_{clk} = 0 V			6.0	pF

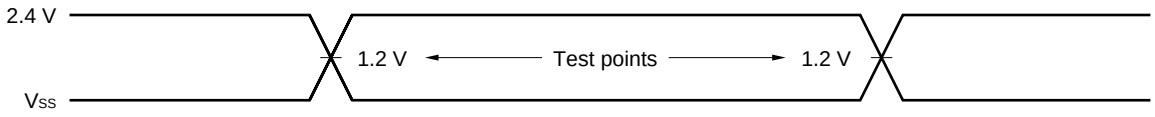
Remark These parameters are periodically sampled and not 100% tested.

AC Characteristics (V_{DD} = 3.3 ± 0.165 V or 2.5 ± 0.125 V)

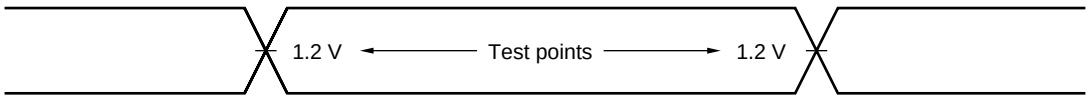
AC Test Conditions

2.5 V LVTTL Interface

Input waveform (Rise / Fall time ≤ 2.4 ns)

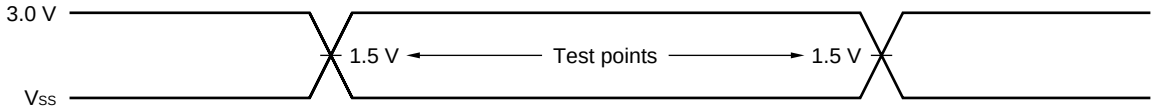


Output waveform

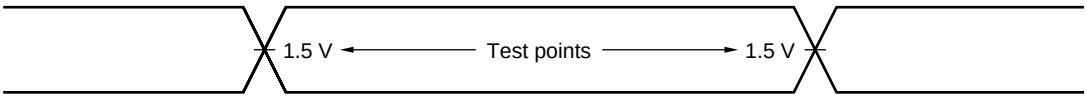


3.3 V LVTTL Interface

Input waveform (Rise / Fall time ≤ 3.0 ns)



Output waveform

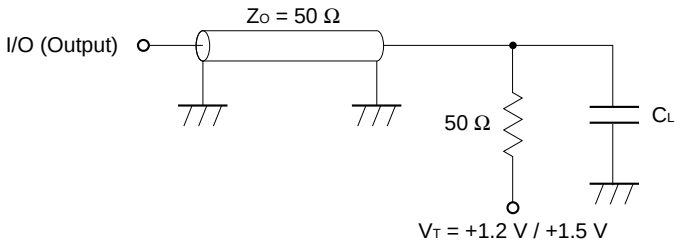


Output load condition

C_L : 30 pF

5 pF (TKHQX1, TKHQX2, TGLQX, TGHQZ, TKHQZ)

Figure External load at test



Remark C_L includes capacitances of the probe and jig, and stray capacitances.

Read and Write Cycle

Parameter		Symbol		-A75 (117 MHz)		Unit	Notes
		Standard	Alias	MIN.	MAX.		
Cycle time		TKHKH	TCYC	8.6	–	ns	
Clock access time		TKHQV	TCD	–	7.5	ns	
Output enable access time		TGLQV	TOE	–	3.5	ns	
Clock high to output active		TKHQX1	TDC1	2.5	–	ns	1, 2
Clock high to output change		TKHQX2	TDC2	2.5	–	ns	
Output enable to output active		TGLQX	TOLZ	0	–	ns	1
Output disable to output High-Z		TGHQZ	TOHZ	0	3.5	ns	1
Clock high to output High-Z		TKHQZ	TCZ	2.5	5	ns	1, 2
Clock high pulse width		TKHKL	TCH	2.5	–	ns	
Clock low pulse width		TKLKH	TCL	2.5	–	ns	
Setup times	Address	TAVKH	TAS	1.5	–	ns	
	Address advance	TADVVKH	TADVS				
	Clock enable	TEVKH	TCES				
	Chip enable	TCVKH	TCSS				
	Data in	TDVKH	TDS				
	Write enable	TWVKH	TWS				
Hold times	Address	TKHAX	TAH	0.5	–	ns	3
	Address advance	TKHADVX	TADVH	(1.0)	(–)		
	Clock enable	TKHEX	TCEH				
	Chip enable	TKHCX	TCSH				
	Data in	TKHDX	TDH				
	Write enable	TKHWX	TWH				
Power down entry time		TZZE	TZZE	–	8.6	ns	
Power down recovery time		TZZR	TZZR	–	8.6	ns	

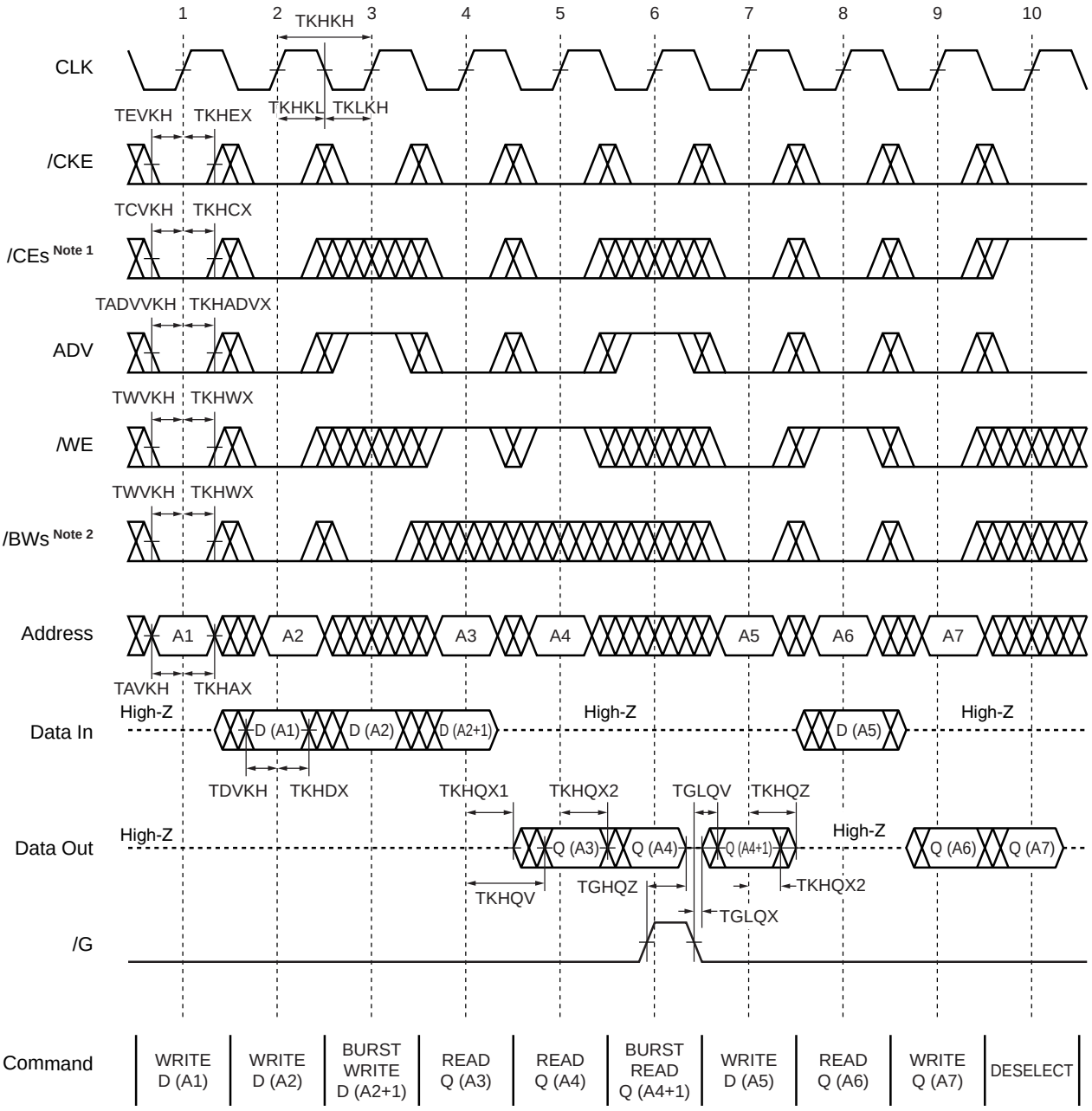
Notes 1. Transition is measured ±200 mV from steady state.

2. To avoid bus contention, the output buffers are designed such that TKHQZ (device turn-off) is faster than TKHQX1 (device turn-on) at a given temperature and voltage. The specs as shown do not imply bus contention because TKHQX1 is a min. parameter that is worse case at totally different conditions (T_A min., V_{DD} max.) than TKHQZ, which is a max. parameter (worse case at T_A max., V_{DD} min.).

3. These values apply when V_{DD} = 3.3 V ±0.165 V with a 3.3 V LVTTL interface, or when V_{DD} = 2.5 V ±0.125 V with a 2.5 V LVTTL interface.

Values in parentheses apply when V_{DD} = 3.3 V ±0.165 V with a 2.5 V LVTTL interface.

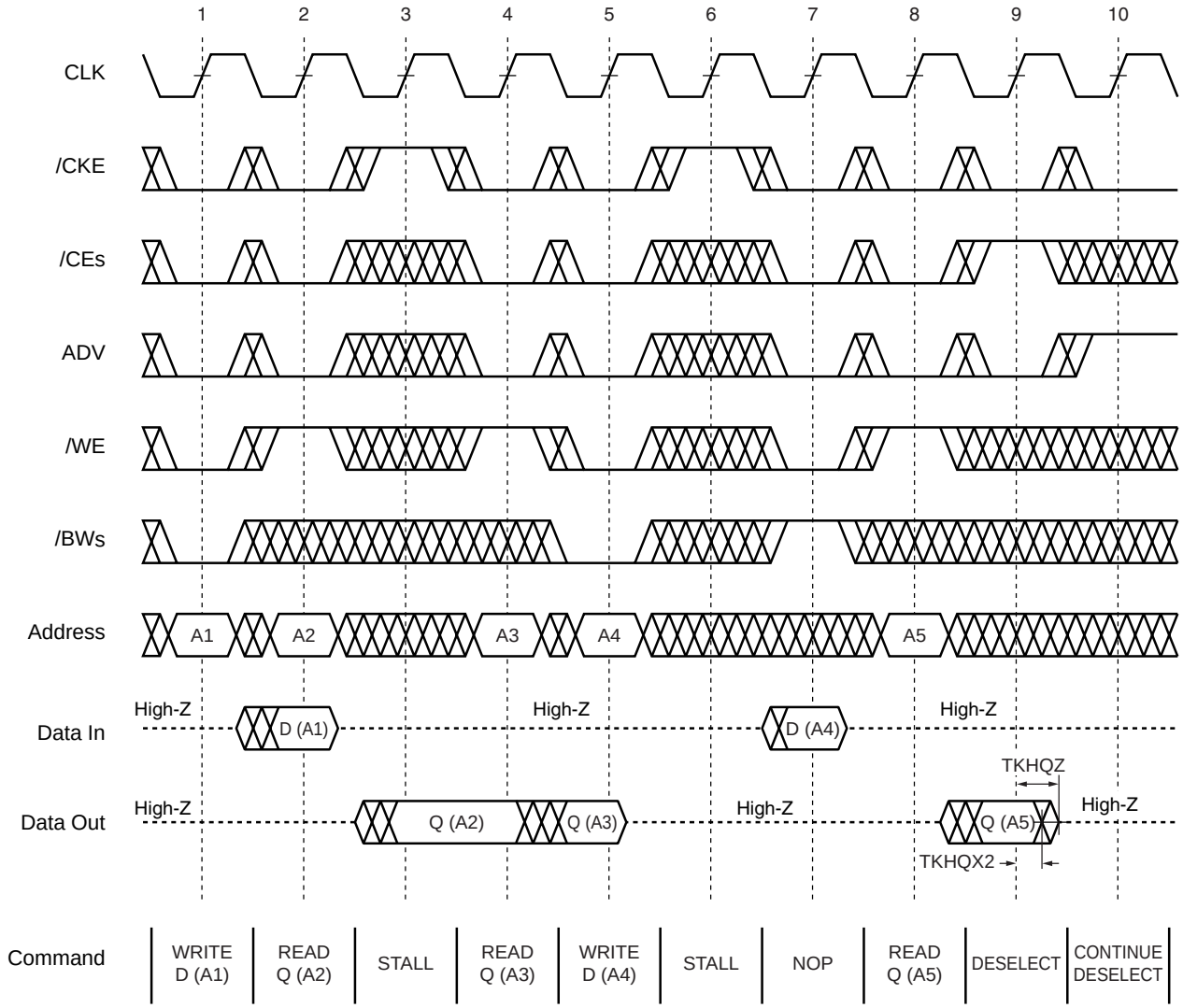
READ / WRITE CYCLE



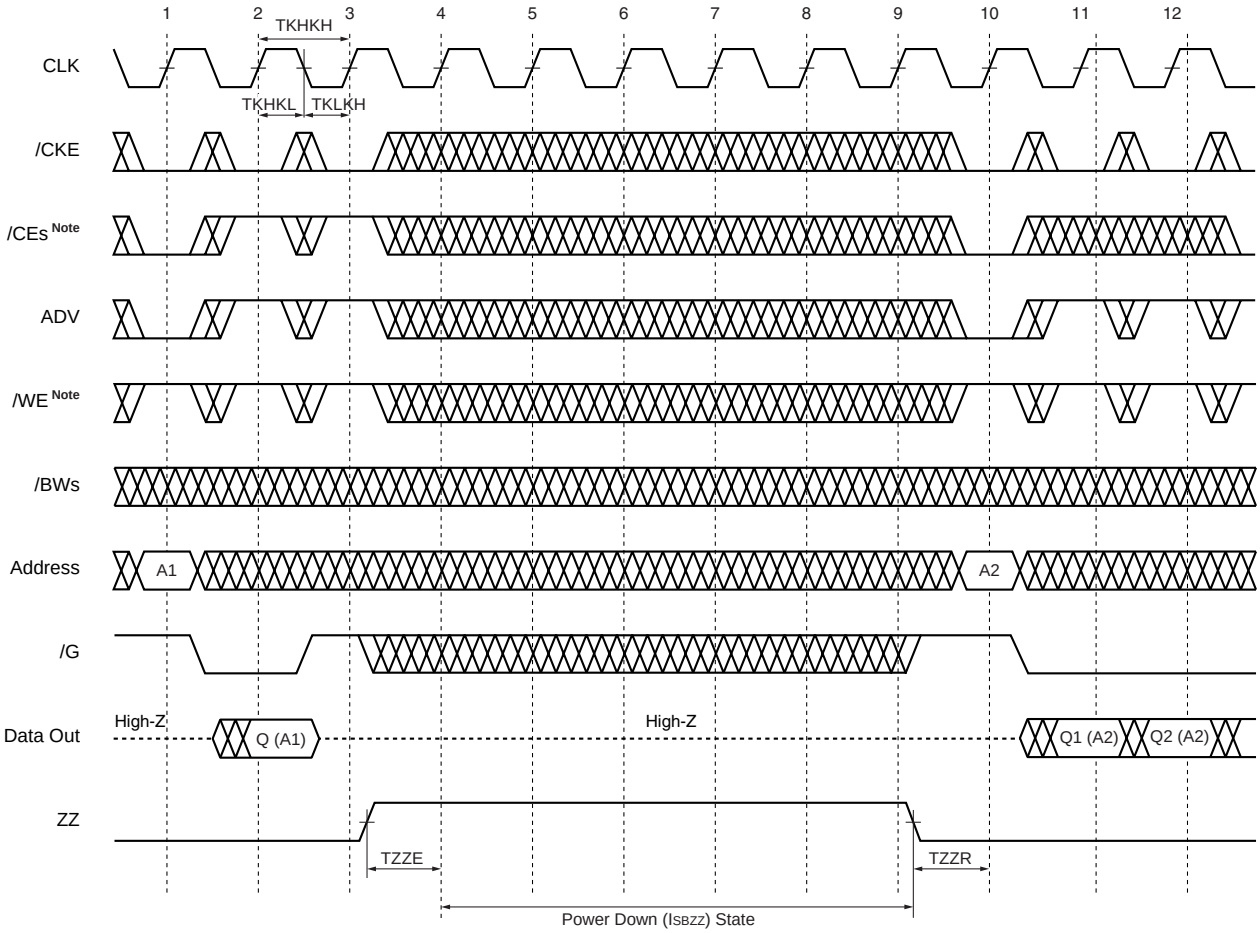
Notes 1. /CEs refers to /CE, CE2 and /CE2. When /CEs is LOW, /CE and /CE2 are LOW and CE2 is HIGH. When /CEs is HIGH, /CE and /CE2 are HIGH and CE2 is LOW.

2. /BWs refers to /BW1, /BW2, /BW3 and /BW4. When /BWs is LOW, any one or more byte write enables (/BW1, /BW2, /BW3 or /BW4) are LOW.

NOP, STALL AND DESELECT CYCLE



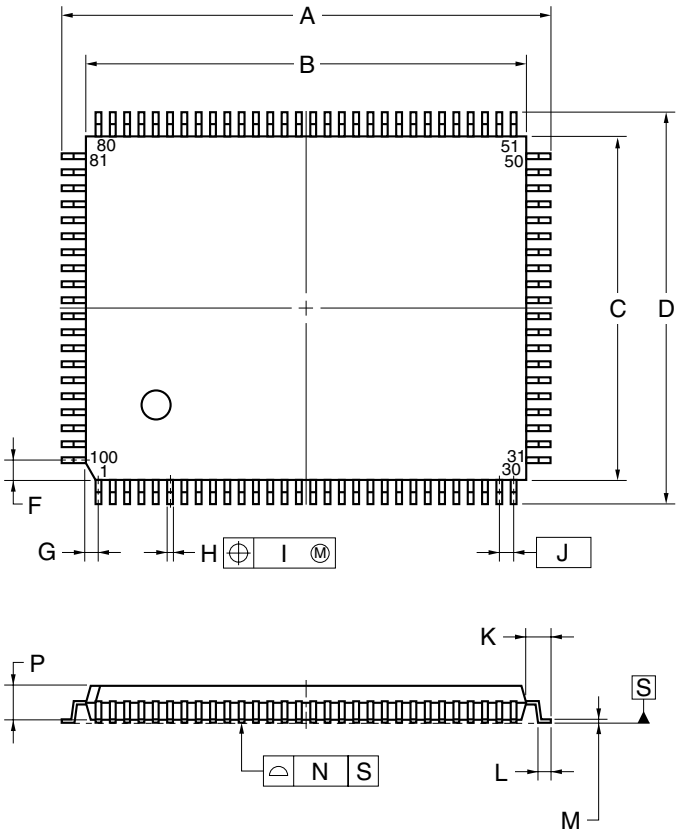
POWER DOWN (ZZ) CYCLE

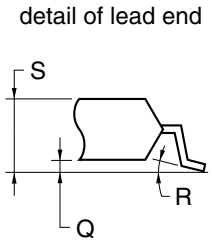


Note /WE or /CEs must be held HIGH at CLK rising edge (clock edge No.3 in this figure) prior to power down state entry.

Package Drawing

100-PIN PLASTIC LQFP (14x20)





NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	22.0±0.2
B	20.0±0.2
C	14.0±0.2
D	16.0±0.2
F	0.825
G	0.575
H	$0.32^{+0.08}_{-0.07}$
I	0.13
J	0.65 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.17^{+0.06}_{-0.05}$
N	0.10
P	1.4
Q	0.125±0.075
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.7 MAX.

S100GF-65-8ET-1

Recommended Soldering Condition

Please consult with our sales offices for soldering conditions of the μPD44321181 and μPD44321361.

Types of Surface Mount Devices

μPD44321181GF : 100-pin PLASTIC LQFP (14 x 20)

μPD44321361GF : 100-pin PLASTIC LQFP (14 x 20)

<R> μPD44321181GF-A : 100-pin PLASTIC LQFP (14 x 20)

<R> μPD44321361GF-A : 100-pin PLASTIC LQFP (14 x 20)

Revision History

Edition/ Date	Page		Type of revision	Location	Description (Previous edition → This edition)
	This edition	Previous edition			
6th edition/ Feb. 2006	p.2	p.2	Addition	Ordering Information	Lead-free products have been added
	pp.3-6	pp.3-6	Addition	Pin Configuration	Lead-free products have been added
	p.20	p.20	Addition	Recommended Soldering Conditions	Lead-free products have been added

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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