HARRIS SEMICONDUCTOR

ACTS74MS

Radiation Hardened Dual D Flip Flop with Set and Reset

December 1992

Features

- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose Up to 1 Mega-RAD (Si)
- Dose Rate Upset >10^{11} RAD(Si)/s, 20ns Pulse
- Cosmic Ray Upset Immunity < 10^{-11} Errors/Bit-Day
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to ALSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.8V Max
  - VIH = VCC/2V Min
- Input Current Levels Ii ≤ 1μA at VOL, VOH

Description

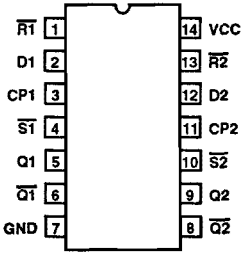
The Harris ACTS74MS is a Radiation Hardened dual D flip flop with set(s) and reset (R). The logic level at data input is transferred to the output during the positive transition of the clock. The Set and Reset are independent from the clock and accomplished by a low level on the appropriate input.

The ACTS74MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

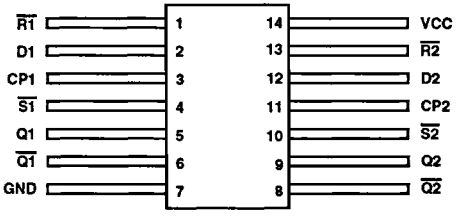
The ACTS74MS is supplied in a 14 lead Ceramic flatpack (K suffix) or a 14 Lead Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW



Truth Table

INPUTS				OUTPUTS	
SET	RESET	CP	D	Q	Q
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↗	H	H	L
H	H	↗	L	L	H
H	H	L	X	Q0	Q0

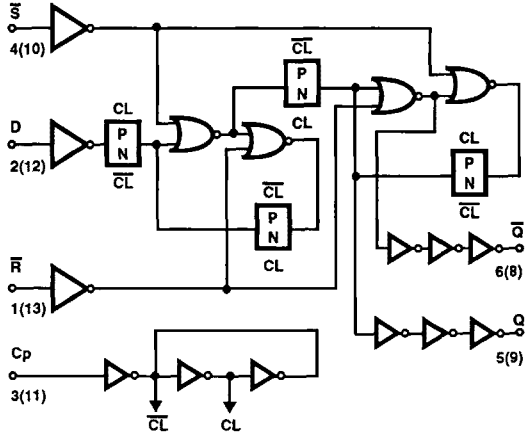
H = High Level (Steady State)
L = Low Level (Steady State)
X = Don't Care
↗ = Transition from Low to High Level

NOTES:

1. Q0 = the level of Q before the indicated input conditions were established.

*This configuration is nonstable, that is, it will not persist when set and reset inputs return to their inactive (high) level.

Functional Diagram



7 LOGIC

File Number 3382

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +6.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±50mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
DIC	75°C/W	16°C/W
Flatpack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC) . . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . 10ns/V Max
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Source)	IOH	VCC = VIH = 4.5V VOUT = VCC - 0.4V, VIL = 0V (Note 2)	1	+25°C	-12	-	mA
			2, 3	+125°C, -55°C	-8	-	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V VOUT = 0.4V VIL = 0V (Note 2)	1	+25°C	12	-	mA
			2, 3	+125°C, -55°C	8	-	mA
Output Voltage High	VOH	VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC - 0.1	-	V
		VCC = 4.5V, VIH =2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC - 0.1	-	V
Output Voltage Low	VOL	VCC = 5.5V, VIH = 2.75V, IOH = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 4.5V, VIH = 2.25V, IOH = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	1.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 3)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:
1. All voltages reference to device GND.
2. Force/Measure functions may be interchanged.
3. Per functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO = 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay CP to Q, $\overline{Q}$	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	1	20	ns
			10, 11	+125°C, -55°C	1	20	ns
	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	1	15	ns
			10, 11	+125°C, -55°C	1	18	ns
Propagation Delay $\overline{S}$ to Q, $\overline{Q}$	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	1	16	ns
			10, 11	+125°C, -55°C	1	17	ns
	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	1	12	ns
			10, 11	+125°C, -55°C	1	13	ns
Propagation Delay $\overline{R}$ to Q, $\overline{Q}$	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	1	16	ns
			10, 11	+125°C, -55°C	1	17	ns
	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	1	12	ns
			10, 11	+125°C, -55°C	1	13	ns
Output Transition Time	TTHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	1	11	ns
	TTLH		10, 11	+125°C, -55°C	1	12	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, VIH = 5.0V F = 1MHz	1	+25°C	Typical 43		pF
			1	+125°C	Typical 50		pF
Input Capacitance	CIN	VCC = 5.0V, VIH = 5.0V F = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Pulse Width CP, $\overline{S}$, $\overline{R}$	TW	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	5.5	-	ns
			1	+125°C	6.3	-	ns
Data to CP Set-up Time	TSU	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	4.3	-	ns
			1	+125°C	4.9	-	ns
Hold Time	TH	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	2	-	ns
			1	+125°C	2	-	ns
Removal Time $\overline{S}$, $\overline{R}$ to CP	TREM	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	3.7	-	ns
			1	+125°C	3.7	-	ns
Max Operating Frequency	FMAX	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	79	-	MHz
			1	+125°C	76	-	MHz

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	1M LIMITS MIN	1M LIMITS MAX	UNITS
Supply Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	mA
Output Current (Source)	IOH	VCC = VIH = 4.5V VOUT = VCC -0.4V, VIL = 0,	+25°C	-8	-	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V VOUT = 0.4V, VIL = 0,	+25°C	8	-	mA
Output Voltage High	VOH	VCC = 5.5V, VIH = 2.75V, VIL = 0.8V, IOH = -50µA	+25°C	VCC -0.1	-	V
		VCC = 4.5V, VIH = 2.25V, VIL = 0.8V, IOH = -50µA	+25°C	VCC -0.1	-	V
Output Voltage Low	VOL	VCC = 5.5V, VIH = 2.75V, VIL = 0.8V, IOH = 50µA	+25°C	-	0.1	V
		VCC = 4.5V, VIH = 2.25V, VIL = 0.8V, IOH = 50µA	+25°C	-	0.1	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±1	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	+25°C	-	-	V
Propagation Delay CP to Q, $\overline{Q}$	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	1	20	ns
	TPLH		+25°C	1	18	ns
Propagation Delay $\overline{S}$ to Q, $\overline{Q}$	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	1	17	ns
	TPLH		+25°C	1	13	ns
Propagation Delay $\overline{R}$ to Q, $\overline{Q}$	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	1	17	ns
	TPLH		+25°C	1	13	ns
Output Transition Time	TTHL TTLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	1	12	ns

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMIT	UNITS
Supply Current	ICC	±2	µA
Output Current	IOL / IOH	±15	%

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with MIL-STD-883 Method 5005 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
-	1, 2, 3, 4, 7, 10, 11, 12, 13	5, 6, 8, 9	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
-	7	5, 6, 8, 9	1, 2, 3, 4, 10, 11, 12, 13, 14	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	7	5, 6, 8, 9	1, 4, 10, 13, 14	3, 11	2, 12

NOTES:

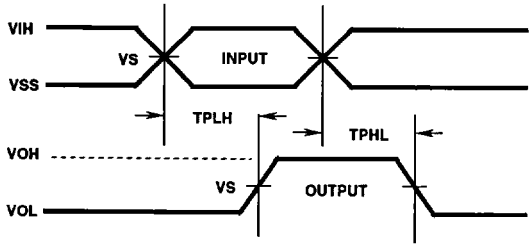
1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 1kΩ ± 5% for dynamic burn-in.

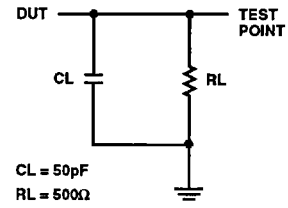
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V	1/2 VCC = 3V ± 0.5V
5, 6, 8, 9	7	1, 2, 3, 4, 10, 11, 12, 13, 14	-

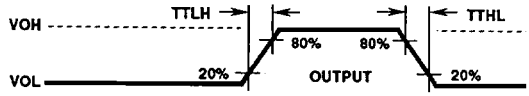
NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

Propagation Delay Timing Diagram and Load Circuit





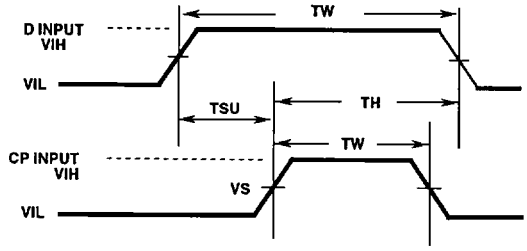
Transition Timing Diagram

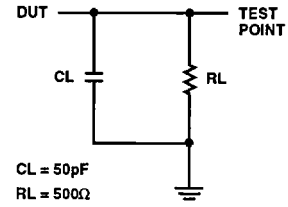


PROPAGATION DELAY VOLTAGE LEVELS

PARAMETER	ACTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Pulse Width, Setup, Hold Timing Diagram Positive Edge Trigger





TH = Hold Time
TSU = Setup Time
TW = Pulse Width

PULSE WIDTH, SETUP, HOLD VOLTAGE LEVELS

PARAMETER	ACTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
88 x 88 mils
2240 x 2240 mm

METALLIZATION:
Type: AlSiCu
Metal 1 Thickness: 6.75kÅ ± 8.25kÅ
Metal 2 Thickness: 9kÅ ± 11kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Silver Glass

WORST CASE CURRENT DENSITY:
$< 2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
110µm x 110µm
4.3 x 4.3 mils

Metallization Mask Layout

ACTS74MS