# 1 Megabit 3.3V Static RAM
# 128K x 8-Bit
# Revolutionary Pinout

## Features

- ☐ High-speed access times
  Com'l: 9, 10, 12, 15 and 20 ns
  Ind'l.: 12, 15 and 20 ns
  Automotive: 15 and 20 ns
- ☐ Low power operation (typical)
  - PDM31034SA
    Active: 200 mW
    Standby: 15 mW
- ☐ Single +3.3V (±0.3V) power supply
- ☐ TTL-compatible inputs and outputs
- ☐ Packages
  Plastic SOJ (400 mil) - SO
  Plastic SOJ (300 mil) - TSO
  Plastic TSOP (II) - T

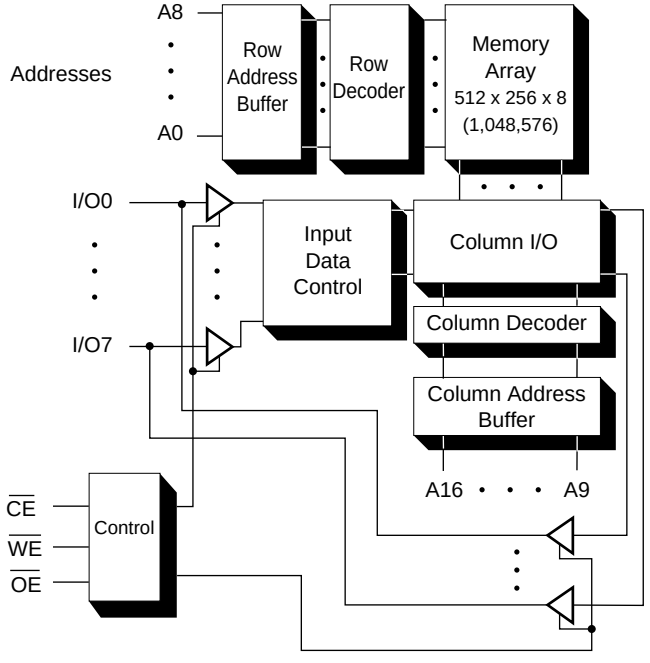
## Description

The PDM31034 is a high-performance CMOS static RAM organized as 131,072 x 8 bits. Writing is accomplished when the write enable ($\overline{WE}$) and the chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ are both LOW.

The PDM31034 operates from a single +3.3V power supply and all the inputs and outputs are fully TTL-compatible.

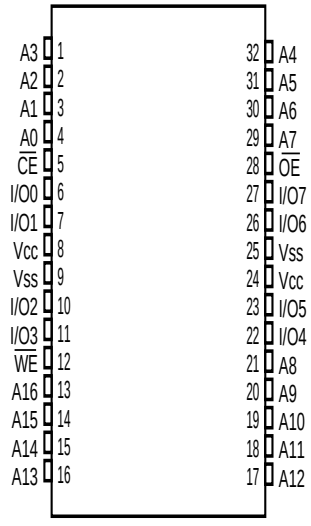
The PDM31034 is available in a 32-pin 400 mil plastic SOJ and 300 mil plastic SOJ, and a 32-pin plastic TSOP (II) package in revolutionary pinout.

## Functional Block Diagram

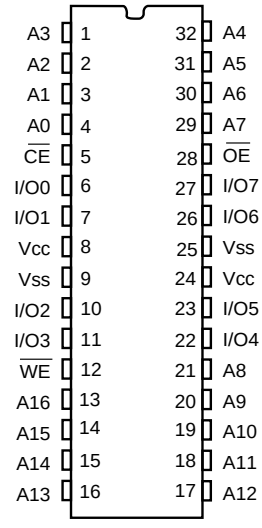


## Pin Configuration

### TSOP (II)




### SOJ




## Pin Description

| Name | Description |
|---|---|
| A16-A0 | Address Inputs |
| I/O7-I/O0 | Data Inputs/Outputs |
| $\overline{OE}$ | Output Enable Input |
| $\overline{WE}$ | Write Enable Input |
| $\overline{CE}$ | Chip Enable Input |
| NC | No Connect |
| $V_{CC}$ | Power (+3.3V) |
| $V_{SS}$ | Ground |

## Truth Table(1)

| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | I/O | MODE |
|---|---|---|---|---|
| L | L | H | $D_{OUT}$ | Read |
| L | X | L | $D_{IN}$ | Write |
| L | H | H | Hi-Z | Output Disable |
| H | X | X | Hi-Z | Standby |

NOTE: 1. H = $V_{IH}$, L = $V_{IL}$, X = DON'T CARE

## Absolute Maximum Ratings (1)

| Symbol | Rating | Com'l. | Ind. | Auto. | Unit |
|---|---|---|---|---|---|
| $V_{TERM}$ | Terminal Voltage with Respect to $V_{SS}$ | –0.5 to +4.6 | –0.5 to +4.6 | –0.5 to +4.6 | V |
| $T_{BIAS}$ | Temperature Under Bias | –55 to +125 | –65 to +135 | –65 to +145 | °C |
| $T_{STG}$ | Storage Temperature | –55 to +125 | –65 to +150 | –65 to +150 | °C |
| $P_T$ | Power Dissipation | 900 | 900 | 900 | mW |
| $I_{OUT}$ | DC Output Current | 50 | 50 | 50 | mA |
| $T_j$ | Maximum Junction Temperature (2) | 125 | 145 | 145 | °C |

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Appropriate thermal calculations should be performed in all cases and specifically for those where the chosen package has a large thermal resistance (e.g., TSOP). The calculation should be of the form: $T_j = T_a + P * \theta_{ja}$ where $T_a$ is the ambient temperature, P is average operating power and $\theta_{ja}$ the thermal resistance of the package. For this product, use the following $\theta_{ja}$ values:

   SOJ: 72° C/W
   TSOP: 95° C/W

## Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| $V_{SS}$ | Supply Voltage | 0 | 0 | 0 | V |
| Industrial | Ambient Temperature | –40 | 25 | 85 | °C |
| Commercial | Ambient Temperature | 0 | 25 | 70 | °C |
| Automotive | Ambient Temperature | –40 | 25 | 105 | °C |

## DC Electrical Characteristics ($V_{CC}$ = 3.3V ± 0.3V)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | $V_{CC}$ = Max., $V_{IN}$ = $V_{SS}$ to $V_{CC}$ | –5 | 5 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{CC}$ = Max., $\overline{CE}$ = $V_{IH}$, $V_{OUT}$ = $V_{SS}$ to $V_{CC}$ | –5 | 5 | µA |
| $V_{IL}$ | Input Low Voltage | | –0.3(1) | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.2 | Vcc+0.3 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 8 mA, $V_{CC}$ = Min. | — | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = –4 mA, $V_{CC}$ = Min. | 2.4 | — | V |

NOTE:1.$V_{IL}$(min) = –3.0V for pulse width less than 20 ns

## Power Supply Characteristics

| | | -9 (1) | -10 (1) | -12 | | -15 | | | -20 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | Parameter | Com'l. | Com'l. | Com'l | Ind. | Com'l | Ind. | Auto. | Com'l | Ind. | Auto. | Unit |
| $I_{CC}$ | Operating Current $\overline{CE}$ = $V_{IL}$<br>f = $f_{MAX}$ = $1/t_{RC}$<br>$V_{CC}$ = Max.<br>$I_{OUT}$ = 0 mA | 125 | 115 | 110 | 120 | 100 | 115 | 120 | 90 | 110 | 115 | mA |
| $I_{SB}$ | Standby Current $\overline{CE}$ = $V_{IH}$<br>f = $f_{MAX}$ = $1/t_{RC}$<br>$V_{CC}$ = Max. | 20 | 20 | 20 | 20 | 20 | 20 | 30 | 20 | 20 | 30 | mA |
| $I_{SB1}$ | Full Standby Current $\overline{CE}$ ≥ $V_{CC}$ – 0.2V<br>f = 0<br>$V_{CC}$ = Max.,<br>$V_{IN}$ ≥ $V_{CC}$ – 0.2V or ≤ 0.2V | 5 | 5 | 5 | 5 | 5 | 5 | 10 | 5 | 5 | 10 | mA |

NOTES: All values are maximum guaranteed values.
1. $V_{CC}$ = 3.3V ± 5%

## Capacitance[1] ($T_A$ = +25°C, f = 1.0 MHz)

| Symbol | Parameter | Max. | Unit |
|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 8 | pF |
| $C_{OUT}$ | Output Capacitance | 8 | pF |

NOTE:1. This parameter is determined by device characterization but is not production tested.

## AC Test Conditions

| | |
|---|---|
| Input pulse levels | $V_{SS}$ to 3.0V |
| Input rise and fall times | 2.5 ns |
| Input timing reference levels | 1.5V |
| Output reference levels | 1.5V |
| Output load | See Figures 1 and 2 |

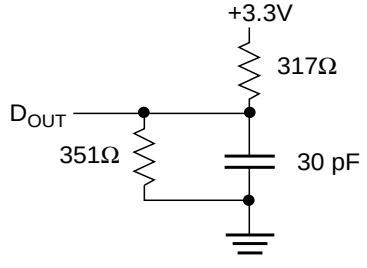



**Figure 1. Output Load Equivalent**

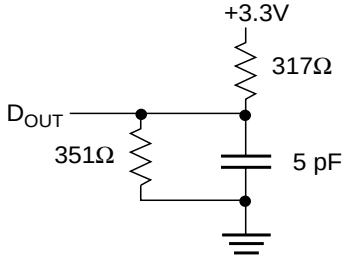
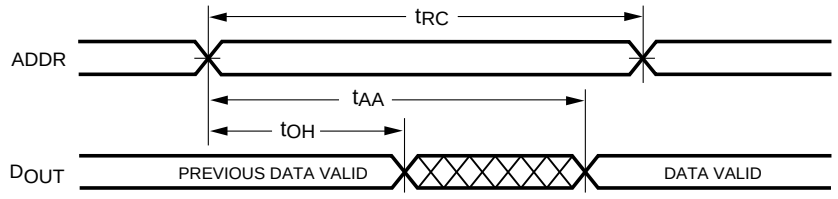
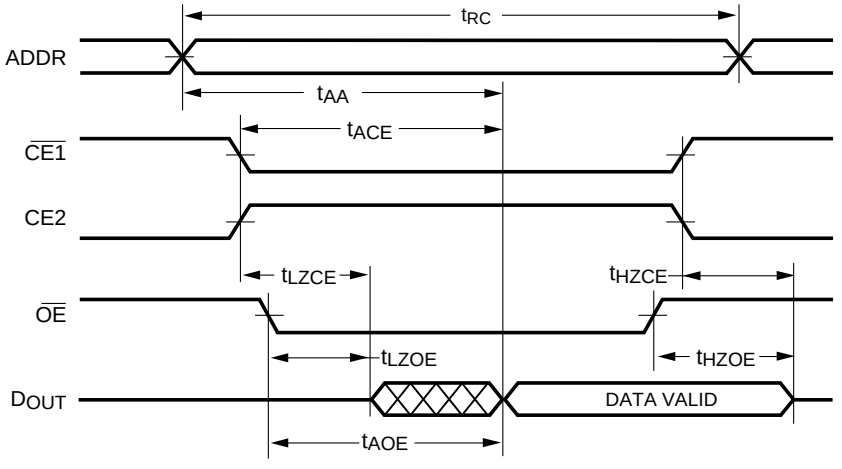



**Figure 2. Output Load Equivalent (for $t_{LZCE}$, $t_{HZCE}$, $t_{LZWE}$, $t_{HZWE}$, $t_{LZOE}$, $t_{HZOE}$)**

## Read Cycle No. 1[4, 5]



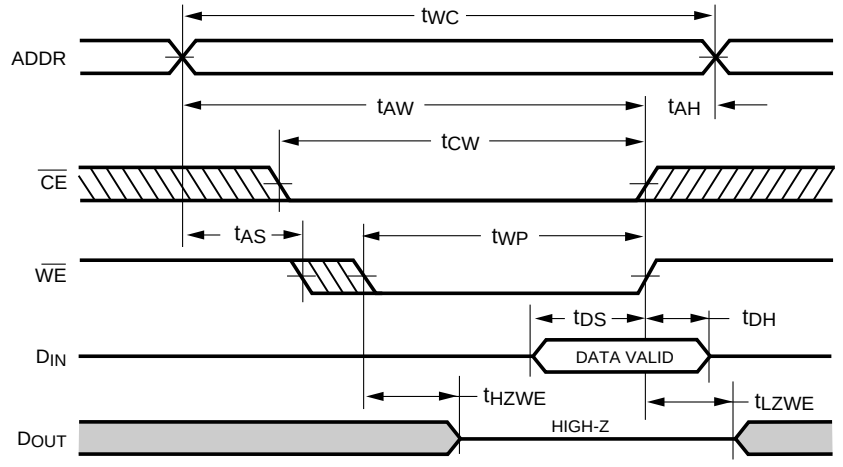

## Read Cycle No. 2[2, 4, 6]



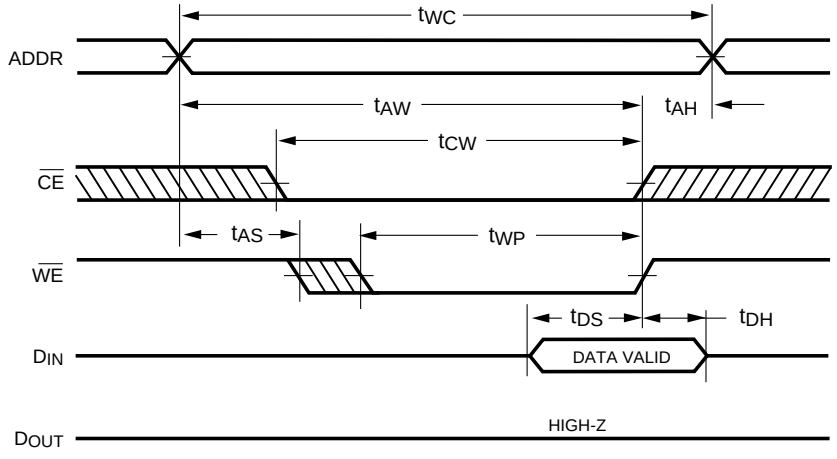

## AC Electrical Characteristics

| Description | | -9 | | -10 | | -12 | | -15 | | -20 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **READ Cycle** | **Sym** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| READ cycle time | $t_{RC}$ | 9 | | 10 | | 12 | | 15 | | 20 | | ns |
| Address access time | $t_{AA}$ | | 9 | | 10 | | 12 | | 15 | | 20 | ns |
| Chip enable access time | $t_{ACE}$ | | 9 | | 10 | | 12 | | 15 | | 20 | ns |
| Output hold from address change | $t_{OH}$ | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| Chip enable to output in low Z[1,3] | $t_{LZCE}$ | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| Chip disable to output in high Z[1,2,3] | $t_{HZCE}$ | | 5 | | 6 | | 7 | | 8 | | 9 | ns |
| Chip enable to power up time[3] | $t_{PU}$ | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Chip disable to power down time[3] | $t_{PD}$ | | 9 | | 10 | | 12 | | 15 | | 20 | ns |
| Output enable access time | $t_{AOE}$ | | 5 | | 6 | | 7 | | 8 | | 9 | ns |
| Output Enable to output in low Z [1,3] | $t_{LZOE}$ | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Output disable to output in high Z[1,3] | $t_{HZOE}$ | | 5 | | 6 | | 7 | | 8 | | 9 | ns |

## Write Cycle No. 1 (Write Enable Controlled)

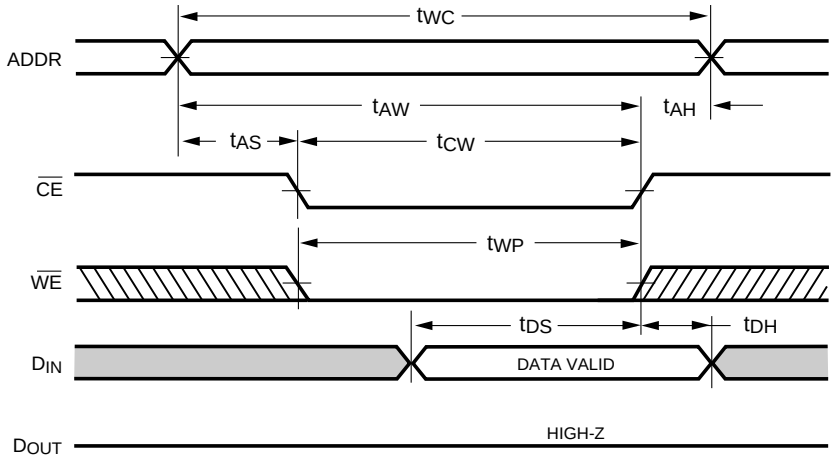



## Write Cycle No. 2 (Write Enable Controlled)




NOTE: Output Enable ($\overline{OE}$) is inactive (high)

## Write Cycle No. 3 (Chip Enable Controlled)




NOTE: Output Enable ($\overline{OE}$) is inactive (high)

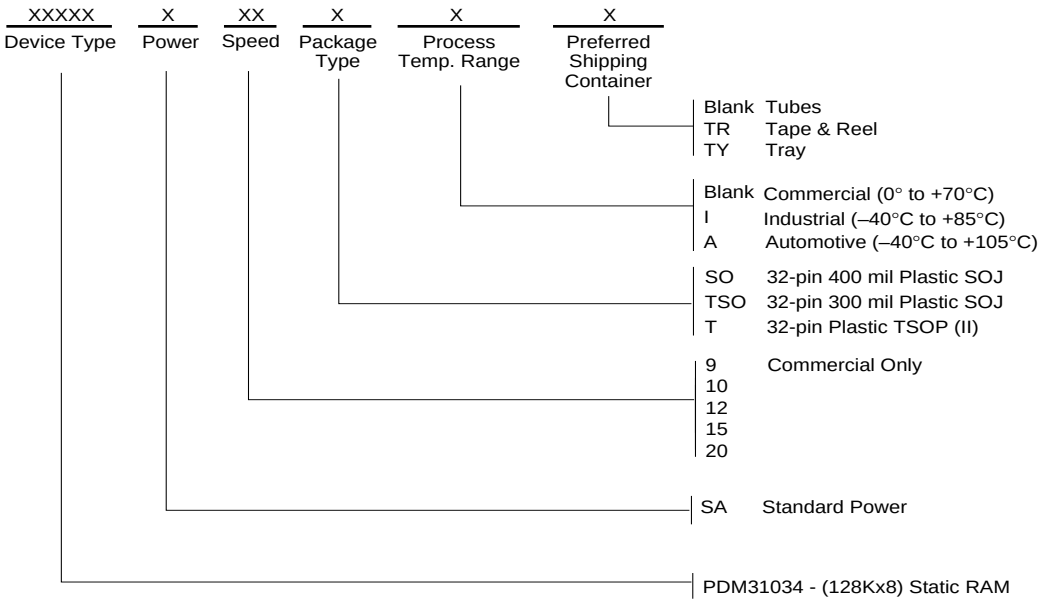
## AC Electrical Characteristics

| Description | | -9 | | -10 | | -12 | | -15 | | -20 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **WRITE Cycle** | **Sym** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| WRITE cycle time | $t_{WC}$ | 9 | | 10 | | 12 | | 15 | | 20 | | ns |
| Chip enable active time | $t_{CW}$ | 8 | | 9 | | 10 | | 11 | | 12 | | ns |
| Address valid to end of write | $t_{AW}$ | 8 | | 9 | | 10 | | 11 | | 12 | | ns |
| Address setup time | $t_{AS}$ | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Address hold from end of write | $t_{AH}$ | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Write pulse width | $t_{WP}$ | 7 | | 8 | | 9 | | 10 | | 11 | | ns |
| Data setup time | $t_{DS}$ | 5 | | 6 | | 7 | | 8 | | 9 | | ns |
| Data hold time | $t_{DH}$ | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Write disable to output in low Z[1,3] | $t_{LZWE}$ | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Write enable to output in high Z[1,3] | $t_{HZWE}$ | | 6 | | 7 | | 7 | | 8 | | 9 | ns |

NOTES: (For two previous Electrical Characteristics tables)

1. The parameter is tested with $C_L$ = 5 pF as shown in Figure 2. Transition is measured ±200 mV from steady state voltage.
2. At any given temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$.
3. This parameter is sampled.
4. $\overline{WE}$ is high for a READ cycle.
5. The device is continuously selected. Chip Enable is held in their active state.
6. The address is valid prior to or coincident with the latest occuring Chip Enable.

## Ordering Information




*Faster Memories for a FasterWorld* ™