AL4CA01
AL4CA02
AL4CA03
AL4CA04
AL4CA05

Data Sheets

Version 1.2

Amendments

07-30-01 Preliminary Version 1.0

10-25-01 Version 1.1, Added DC and AC timing data

01-03-02 Version 1.2, change speed grade to 12ns and change US office address in back page

02-20-03 Company Contact Information updated

AL4CA01/AL4CA02/AL4CA03/AL4CA04/AL4CA05 (512 x9, 1k x9, 2k x9, 4k x9, 8k x9) Asynchronous FIFO

Contents:

1.0 Description ____ *4*
2.0 Features ____ *4*
3.0 Applications ____ *4*
4.0 Chip Information ____ *5*
4.1 Marking Information ____ **5**
4.1 Ordering Information ____ **5**
5.0 Pin-out Diagram ____ *5*
6.0 Block Diagram ____ *6*
7.0 Pin Definition and Description ____ *7*
8.0 Memory Operations ____ *8*
8.1 Inputs and Outputs ____ **8**
8.2 Controls ____ **8**
8.3 Flags ____ **9**
9.0 Multiple Devices Bus Expansion and Cascading ____ *10*
9.1 Width Expansion Configuration ____ **10**
9.2 Depth Expansion ____ **11**
10.0 Electrical Characteristics ____ *13*
10.1 Absolute Maximum Ratings ____ **13**
10.2 Recommended Operating Conditions ____ **13**
10.3 DC Characteristics ____ **13**
10.4 AC Electrical Characteristics ____ **13**
10.5 Timing Diagrams ____ **16**
11.0 Mechanical Drawing ____ *20*
11.1 32-pin PLCC Package ____ **20**

1.0 Description

The AL4CA01/AL4CA02/AL4CA03/AL4CA04/AL4CA05 series memory products are high-performance, low-power 9-bit read/write FIFO (First-In-First-Out) memory chips. They are specially designed to buffer high speed streaming data for a wide range of communication applications, such as optical disk controllers, Local Area Networks (LANs), SONET (Synchronous Optical Network).

The reads and writes are sequential access by using of ring pointers, with no address lines required to write and read data. Data is toggled in and out of the devices through the use of the Write (/W) and Read (/R) ins. The devices have a maximum data access time as fast as 25ns.
The devices utilize a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a party bit for transmission/reception error checking. They also feature a Retransmit (/RT) capability that allows for reset of the read pointer to its initial position when /RT is pulsed LOW to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

The AL4CA01/02/03/04/05 are designed and fabricated using state of the art technology.

2.0 Features

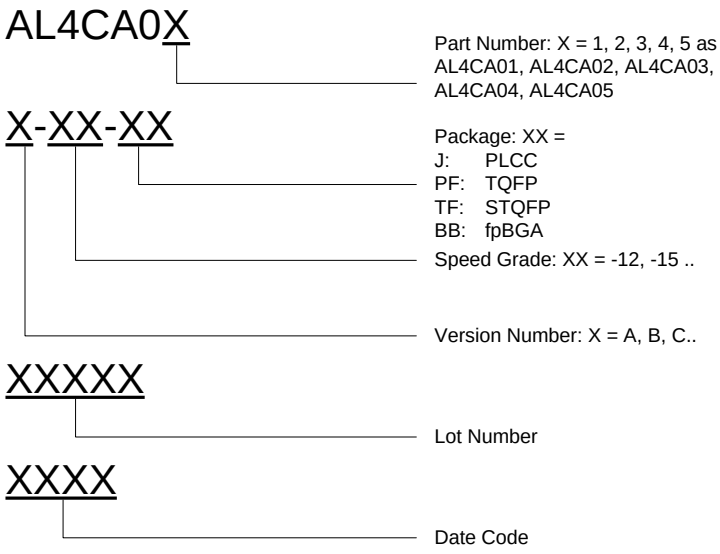
- 512 x9-bit cell array (AL4CA01)
- 1,024 x9-bit cell array (AL4CA02)
- 2,048 x9-bit cell array (AL4CA03)
- 4,096 x9-bit cell array (AL4CA04)
- 8,192 x9-bit cell array (AL4CA05)
- 12 ns read/write cycle time
- Asynchronous data access
- Independent Read and Write operations
- Auto-retransmit support
- Empty, Full and Half-Full flags support
- 3.3V power supply with 5V tolerant
- Available in a 32-pin PLCC

3.0 Applications

- Routers
- ATM switches
- Cable modems
- Wireless base stations
- SONET(Synchronous Optical Network) multiplexers

4.0 Chip Information

4.1 Marking Information



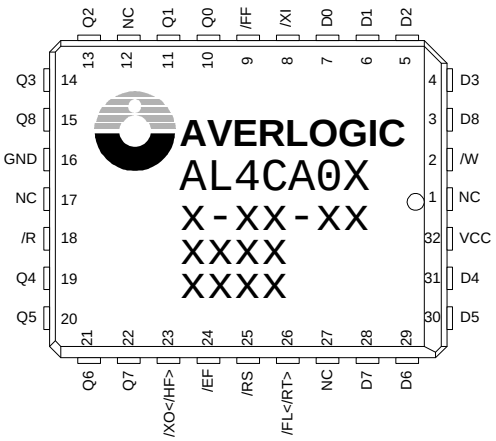
4.1 Ordering Information

The ordering information for AL4CA01/AL4CA02/AL4CA03/AL4CA04/AL4CA05 are:

Part number	Package	Power Supply	Status
AL4CA01/02/03/04/05 (A-12-J)	32-pin plastic PLCC	+3.3V±10%	Sample in Aug., 2001

5.0 Pin-out Diagram

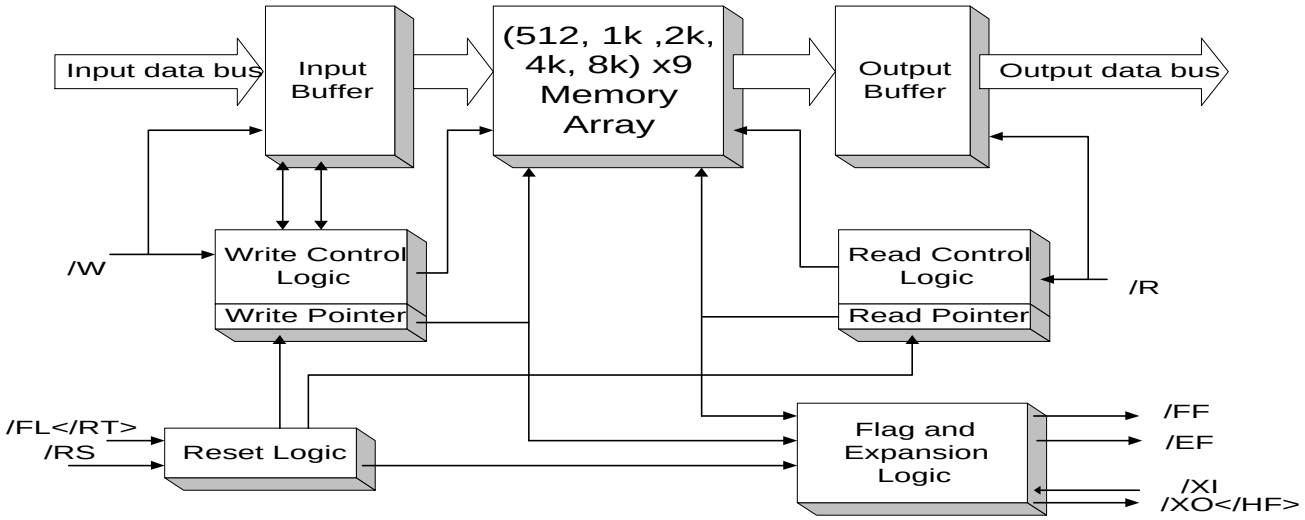
The AL4CA01/AL4CA02/AL4CA03/AL4CA04/AL4CA05 pin-out diagram is following:



PLCC PACKAGE TOP VIEW

6.0 Block Diagram

The internal structure of the AL4CA01/AL4CA02/AL4CA03/AL4CA04/AL4CA05 consists of Input/Output buffers, Read/Write Control Logic and main (512, 1k, 2k, 4k, 8k) x9 different configuration memory cell array and state-of-the-art logic design that takes care of addressing and controlling the read/write data.



AL4CA0x FIFO Block Diagram

7.0 Pin Definition and Description

The pin-out definition and function are described as following:

Write Bus Signals

Pin Symbol	Pin name	Pin number	I/O type	Description
D[8:0]	Data Inputs	3,28,29,30, 31,4,5,6,7	I	9-bit input data bus.
/W	Write Enable	2	I	A write cycle is initiated on the falling edge of Write Enable (/W) if the FIFO Full Flag (/FF) is not asserted. Data setup and hold times must meet respectively to the rising edge of the Write Enable (/W).

Read Bus Signals

Pin symbol	Pin name	Pin number	I/O type	Description
Q[8:0]	Data Outputs	15,22,21,20, 19,14,13,11, 10	O	9-bit output data bus.
/R	Read Enable	18	I	A read cycle is initiated on the falling edge of the Read Enable (/R) if the FIFO Empty Flag (/EF) is not asserted. The valid data is ready at output bus after t_A of the Read Enable (/R) falling edge.

Miscellaneous & Flags Signals

Pin Symbol	Pin name	Pin number	I/O type	Description
/RS	Reset	25	I	When /RS is set LOW, internal read and write pointers are set to the first location of the memory array, /HF, /FF go HIGH, and /EF go LOW. A reset is required before an initial WRITE after power-up.
/FF	Full Flag	9	O	/FF indicates whether or not the FIFO memory is full.
/EF	Empty Flag	24	O	/EF indicates whether or not the FIFO memory is empty.
/XO</HF>	Expansion Out<Half-Full Flag>	23	O	This is a dual-purpose output. In the single device mode, when Expansion In (/XI) is grounded, this pin is Half-Full Flag (/HF). In the multiple chips daisy chain mode, this pin is connected to Expansion In (/XI) of successive chip for depth expansion.
/XI	Expansion	8	O	This pin is connected to ground in the single chip

	In			configuration. This pin (/XI) is connected to Expansion Out (/XO) of the previous device in the Depth Expansion or Daisy Chain Mode.
/FL</RT>	First Load <Retransmit >	26	I	In the Depth Expansion Mode, this pin is grounded to operate as the first loaded. In the Single Device Mode, this pin is the retransmit control input.
NC	No Connect	1,12,17,27	-	No Connect

Power/Ground Signals

Pin Symbol	Pin name	Pin number	I/O type	Description
VCC	Power	32	-	3.3V ± 10% power supply
GND	Ground	16	-	Ground.

8.0 Memory Operations

8.1 Inputs and Outputs

8.1.1 DATA INPUTS (D8 ~ D0)

D8 ~ D0 are 9-bit wide of input data port.

8.1.2 DATA OUTPUTS (Q8-Q0)

Q8 ~ Q0 are 9-bit wide of output data port.

8.2 Controls

8.2.1 Reset (/RS)

Reset takes place when the Reset (/RS) input is LOW. During reset, both internal read and write pointers are set to the staring position. A reset is required to initial internal logic after power-up. Both the Read Enable (/R) and Write Enable (/W) inputs must go HIGH t_{RSS} time period before /RS go HIGH (rising edge) and maintain HIGH t_{RSR} time period after. The Full Flag (/FF) and Half-Full Flag (/HF) will be reset to HIGH after t_{FFH} and t_{HFH} respectively of falling edge of /RS pulse. The Empty Flag (/EF) will be reset to LOW after t_{RSF} of the falling edge of /RS pulse. During reset, the output register is initialized to all zeros.

8.2.2 Write Enable1 (/W)

A write operation occurs on the falling edge of Write Enable (/W) if the Full Flag (/FF) is not set. Data setup and hold times must meet the respect to the rising edge of the Write Enable (/W). Data is stored in the memory array sequentially and independently of any ongoing read operation.
The Half-Full Flag (HF) will be set to LOW after half of the memory is filled and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. To prevent data overflow, the Full Flag (FF) will go LOW, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag (FF) will go HIGH after tRFF, allowing a valid write to begin.

8.2.4 Read Enable (/R)

A read operation occurs on the falling edge of the Read Enable (/R) if the Empty Flag (EF) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operations. After Read Enable (R) goes HIGH, the Data Outputs (Q0 – Q8) will return to a high impedance condition until the next Read operation. When last data has been read from the FIFO, the Empty Flag (EF) will go LOW inhibiting further read operations with the Q0 ~Q8 staying in a high impedance state. Once a valid write operation has been accomplished, the Empty Flag (EF) will go HIGH after tWEF and a valid Read can then begin. The Read Enables (/R) is ignored when the FIFO is empty.

8.2.6 First Load<Retransmit>(/FL</RT>)

This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to operate as the first loaded (see Operating Modes). In the Single Device Mode, this pin is the retransmit control input.

Single Device -

The Single Device Mode is initiated by grounding the Expansion In (/XI). These FIFOs can be made to retransmit data when the Retransmit Enable control (/RT) input goes LOW. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read Enable (/R) and Write Enable (/W) must be HIGH during retransmit single in the LOW state. This feature is useful for one time write and multiple read applications in single device configuration.

Multiple Devices Cascading –

Cascading multiple devices to expand FIFO depth beyond 512/1,024/2,048/4,096/8,192/16,384 respectively is possible. By connecting First Load (/FL) of the first cascading device to ground and First Load (/FL) of other cascading devices to HIGH can expand the FIFO depth and get the longer delay. The retransmit feature is not applicable the Depth Expansion Mode and neither Half-Full Flag (HF) can provide feasible function.

8.2.6 Expansion In (/XI)

This input is a dual-purpose pin. Expansion In (XI) is connected to ground in the single chip configuration. This pin (/XI) is connected to Expansion Out (/XO) of the previous device in the Depth Expansion or Daisy Chain mode.

8.3 Flags

8.3.1 Full Flag (/FF)

The Full Flag (/FF) will go LOW, inhibiting further write operation, when the device is full (Write Pointer is one location less than the read pointer). If no reads are performed after Reset (/RS), the Full Flag (/FF) will go LOW after 512 writes for the AL4CA01, 1,024 writes for the AL4CA02, 2,048 writes for the AL4CA03, 4,096 writes for the AL4CA04 and 8,192 writes for the AL4CA05.

8.3.2 Empty Flag (/EF)

The Empty Flag (/EF) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating the device is empty.

8.3.3 Expansion Out<Half-Full Flag>(/XO</HF>)

This is a dual-purpose output. In the single device mode, when Expansion In (/XI) is grounded, this pin is Half-Full Flag (/HF).

Single Device -

When half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag (/HF) will be set LOW and will remain LOW until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag (/HF) is then reset on the rising edge of the read operation.

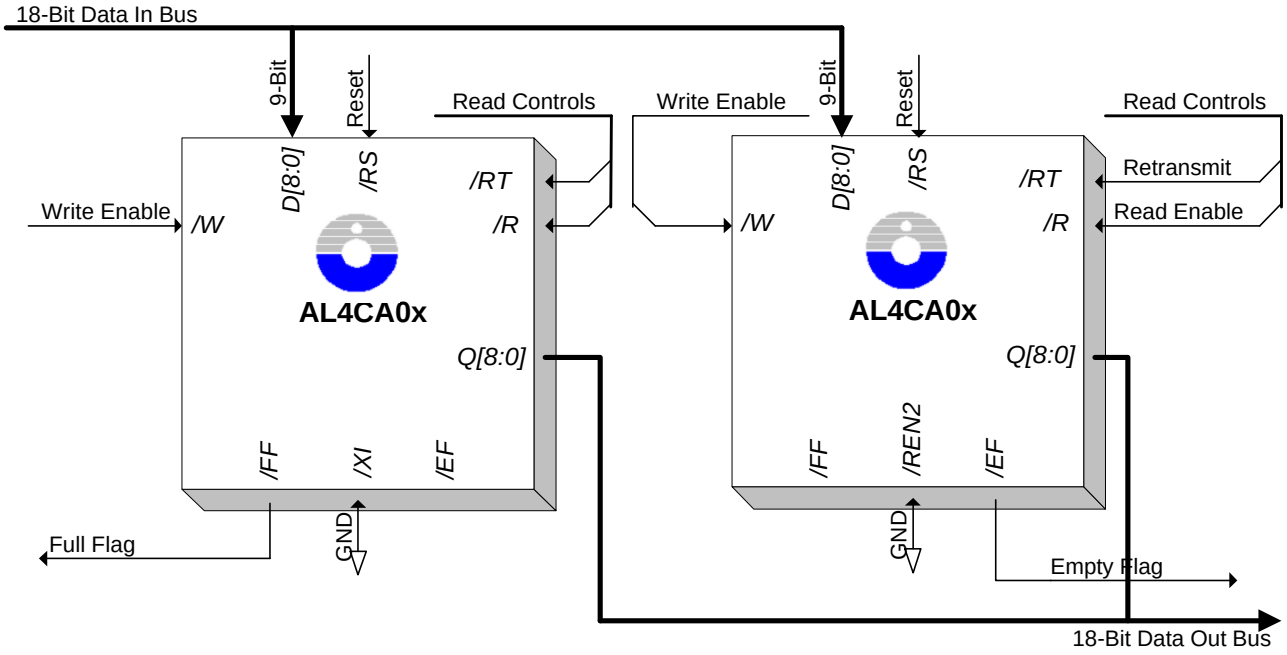
Multiple Devices Cascading –

In the multiple chips daisy chain cascading mode, Expansion Out (/XO) is connected to Expansion In (/XI) of previous chip for depth expansion. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

9.0 Multiple Devices Bus Expansion and Cascading

9.1 Width Expansion Configuration

Simply connecting the corresponding input controls signals of multiple devices may increase data bus width. Status flags (/EF, /HF and /FF) can be reported from any of device. The Expansion In (/XI) is connected to ground for each device working as single device mode.



Multiple FIFO memory Used in Width Expansion Mode

Width Expansion Mode

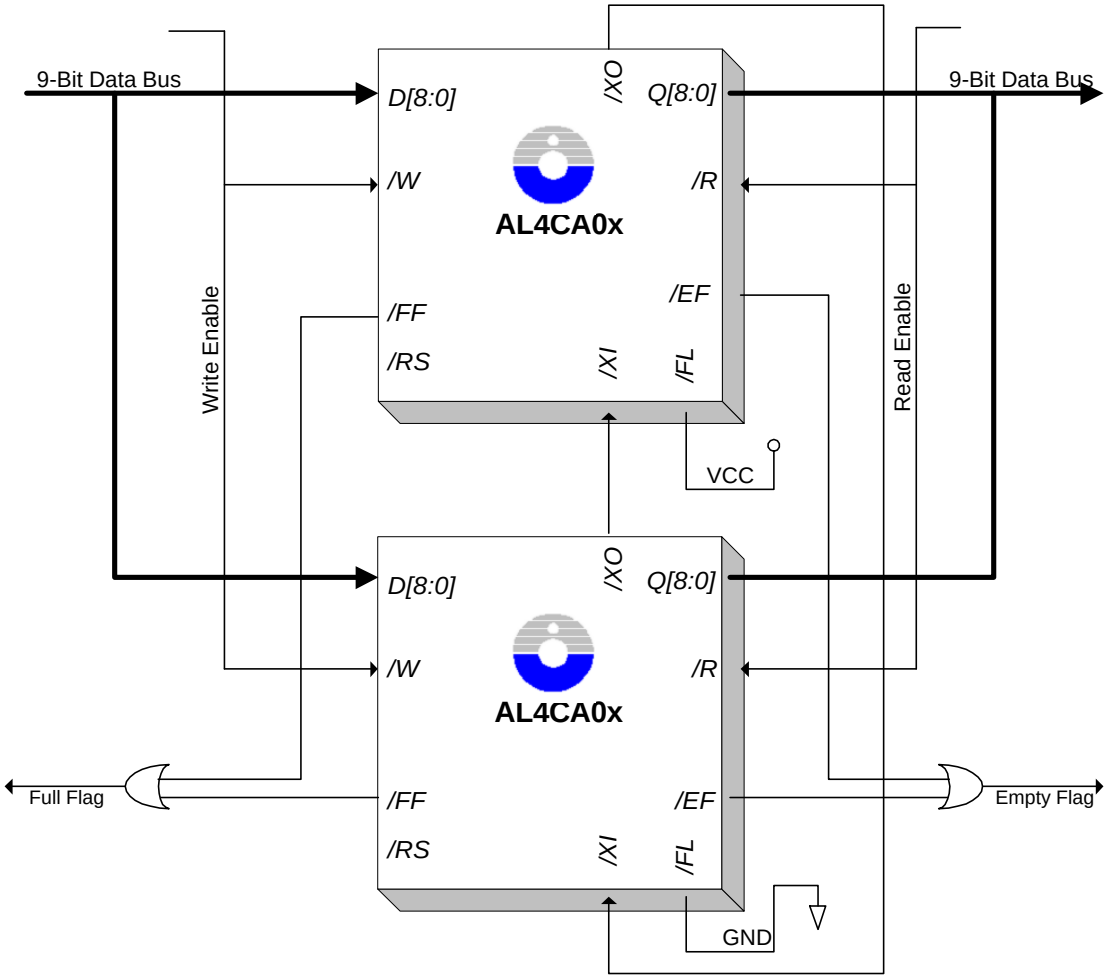
Mode	Inputs	Internal Status	Outputs

	/RS	/RT	/XI	Read Pointer	Write Pointer	/EF	/FF	/HF
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment	Increment	X	X	X

9.2 Depth Expansion

The depth expansion of AL4CA01/02/03/04/05 is also possible. These FIFOs can easily be adapted to applications when the requirements of the FIFO depth are for greater than 512/1,024/2,048/4,096/8,192/16,384 words. These devices operate in the Depth Expansion mode when the following conditions are met:

1. The First Load (/FL) control input of the first device need to be grounded.
2. All other devices must have First Load (/FL) in the HIGH state.
3. The Expansion Out (/XO) pin of each device must be tied to the Expansion In (XI) pin of the next device
4. External logic is needed to generate a composite Full Flag (/FF) and Empty Flag (/EF). By ORing of all /EFs and ORing of all /FFs, all /EFs or /FFs flags must be set to generate the correct composite /EF or /FF.
5. The Retransmit (/RT) function and Half-Full Flag (/HF) are supported in the Depth Expansion Mode.



Multiple FIFO memory used in depth expansion

Depth Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	/RS	/FL	/XI	Read Pointer	Write Pointer	/EF	/FF
Reset First Device	0	0	X	Location Zero	Location Zero	0	1
Reset All Other Device	0	1	X	Location Zero	Location Zero	0	1
Read/Write	1	X	X	X	X	X	X

10.0 Electrical Characteristics

10.1 Absolute Maximum Ratings

Parameter		3.3V Rating	Unit
V_{DD}	Supply Voltage	-0.3 ~ +3.8	V
V_P	Pin Voltage	-0.3 ~ +(V_{DD}+0.3)	V
I_O	Output Current	-20 ~ +20	mA
T_{AMB}	Ambient Op. Temperature	0 ~ +85	°C
T_{stg}	Storage temperature	-40 ~ +125	°C

10.2 Recommended Operating Conditions

Parameter		3.3V Rating			Unit
		Min	Typ	Max	
V_{DD}	Supply Voltage	+3.0	+3.3	+3.6	V
V_{IH}	High Level Input Voltage	0.7 V_{DD}		V_{DD}	V
V_{IL}	Low Level Input Voltage	0		0.3 V_{DD}	V

10.3 DC Characteristics

(V_{DD} = 3.3V, Vss=0V. T_{AMB} = 0 to 70°C)

Parameter		3.3V Rating			Unit
		Min	Typ	Max	
I_{DD}	Operating Current	-	-	16	mA
I_{DDS}	Standby Current	-	1.8	5	mA
V_{OH}	Hi-level Output Voltage	2.4	-	V_{DD}	V
V_{OL}	Lo-level Output Voltage	-	-	+0.4	V
I_{LI}	Input Leakage Current	-2	-	+2	μA
I_{LO}	Output Leakage Current	-10	-	+10	μA

Note: The Operating Current is tested at f = 20 Mhz.

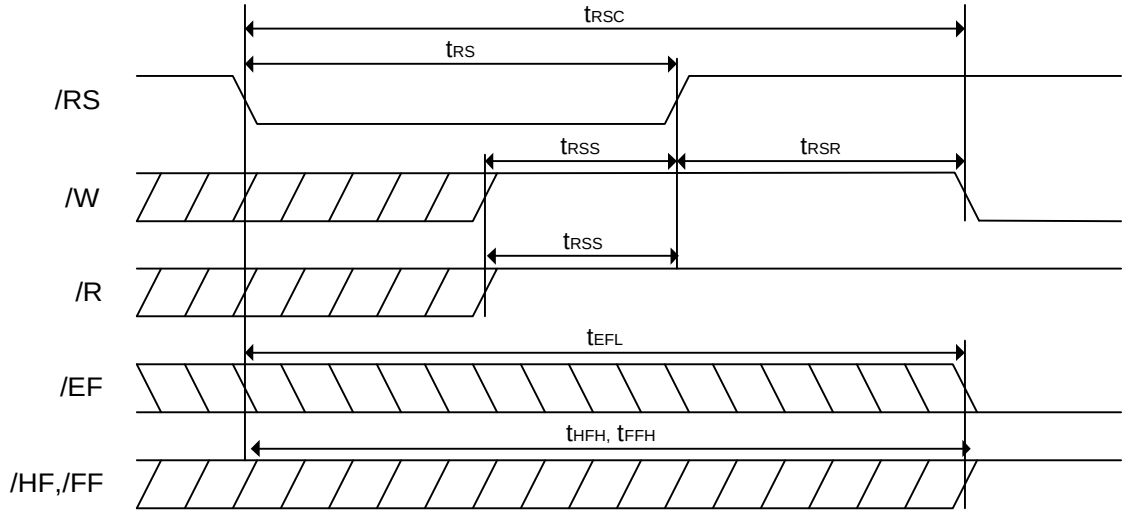
10.4 AC Electrical Characteristics

(V_{DD} = 3.3V, Vss=0V, T_{AMB} = 0 to 70°C)

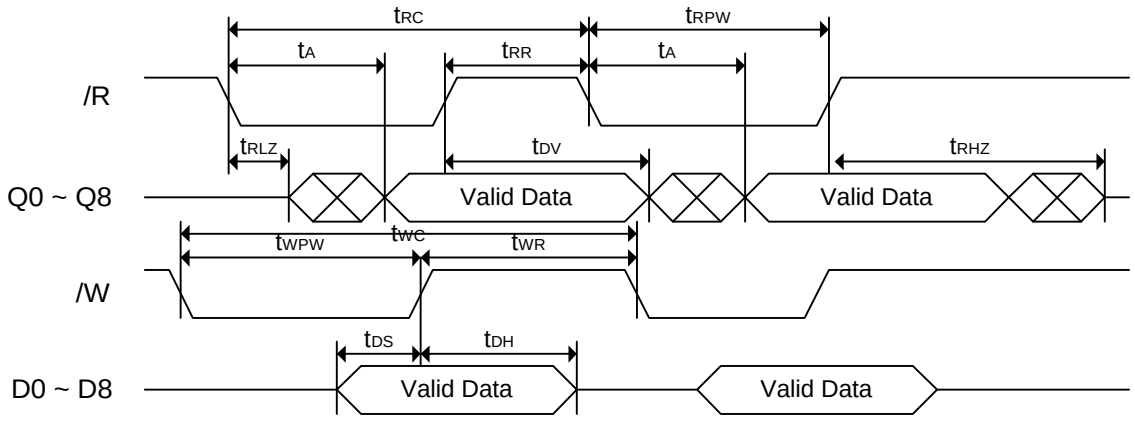
		12ns		
Symbol	Parameter	Min	Max	Unit
t_S	Shift Frequency	-	50	ns
t_{RC}	Read Cycle Time	20	-	ns
t_A	Access Time	-	12	ns
t_{RR}	Read Recovery Time	8	-	ns
t_{RPW}	Read Pulse Width	12	-	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z	3	-	ns
t_{WLZ}	Write pulse High to Data Bus at Low Z	5	-	ns
t_{DV}	Data Valid from Read Pulse High	5	-	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z	-	12	ns
t_{WC}	Write Cycle Time	20	-	ns
t_{WPW}	Write Pulse Width	12	-	ns
t_{WR}	Write Recovery Time	8	-	ns
t_{DS}	Data Setup Time	7	-	ns
t_{DH}	Data Hold Time	2	-	ns
t_{RSC}	Reset Cycle Time	20	-	ns
t_{RS}	Reset Pulse Width	12	-	ns
t_{RSS}	Reset Setup Time	12	-	ns
t_{RSR}	Reset Recovery Time	8	-	ns
t_{RTC}	Retransmit Cycle Time	20	-	ns
t_{RT}	Retransmit Pulse Width	12	-	ns
t_{RTS}	Retransmit Setup Time	12	-	ns
t_{RTR}	Retransmit Recovery Time	8	-	ns
t_{EFL}	Reset to Empty Flag Low	-	12	ns
$t_{HFH,FFH}$	Reset to /HF (Half-Full) and /FF (Full Flag) High	-	17	ns
t_{RTF}	Retransmit Low to Flags Valid	-	20	ns
t_{REF}	Read Low to /EF (Empty Flag) Low	-	12	ns
t_{RFF}	Read High to /FF (Full Flag) High	-	14	ns
t_{RPE}	Read Pulse Width after /EF (Empty Flag) High	12	-	ns
t_{WEF}	Write High to /EF (Empty Flag) High	-	12	ns
t_{WFF}	Write Low to /FF (Full Flag) Low	-	14	ns
t_{WHF}	Write Low to /HF (Half-Full Flag) Low	-	17	ns

t_{RHF}	Read High to /HF (Half-Full Flag) High	-	17	ns
t_{WPF}	Write Pulse Width after /FF (Full Flag) High	12	-	ns
t_{XOL}	Read/Write to /XO (Expansion Out) Low	-	12	ns
t_{XOH}	Read/Write to Expansion Out High	-	12	ns
t_{XI}	/XI (Expansion In) Pulse Width	12	-	ns
t_{XIR}	/XI (Expansion In) Recovery Time	8	-	ns
t_{XIS}	/XI (Expansion In) Setup Time	8	-	ns

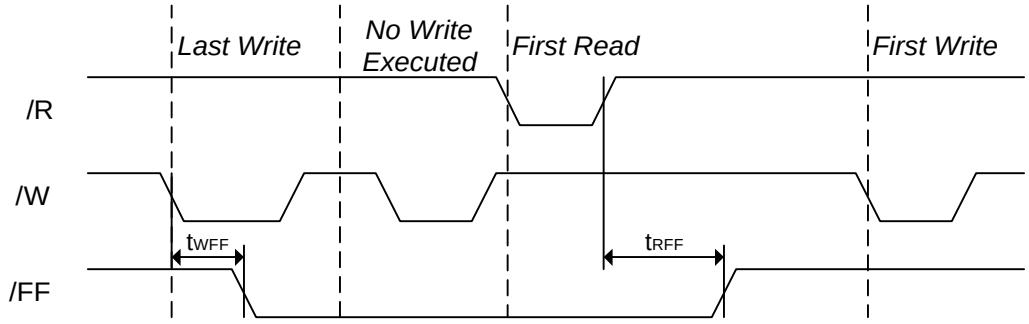
10.5 Timing Diagrams



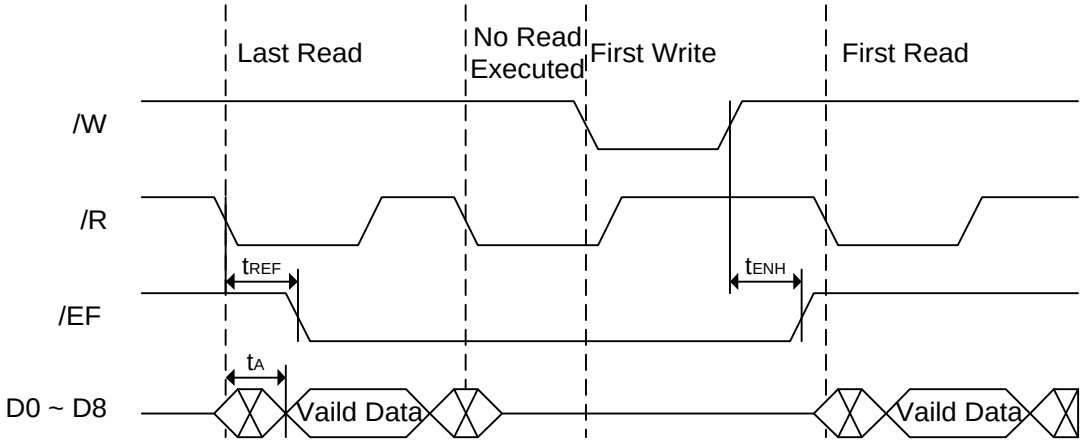
Reset Timing



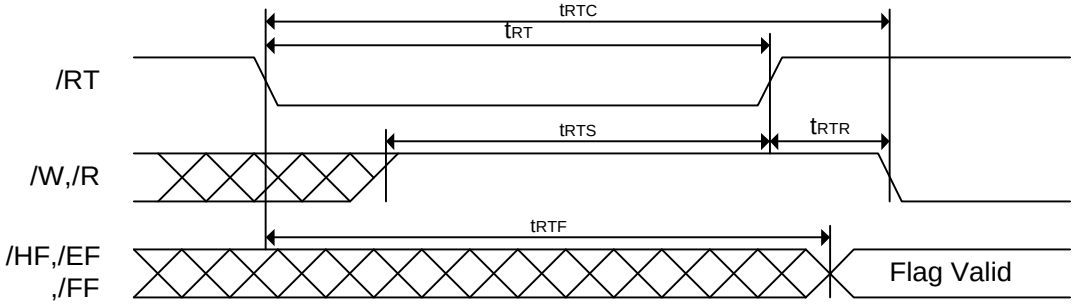
Asynchronous Write and Read Cycle Timing



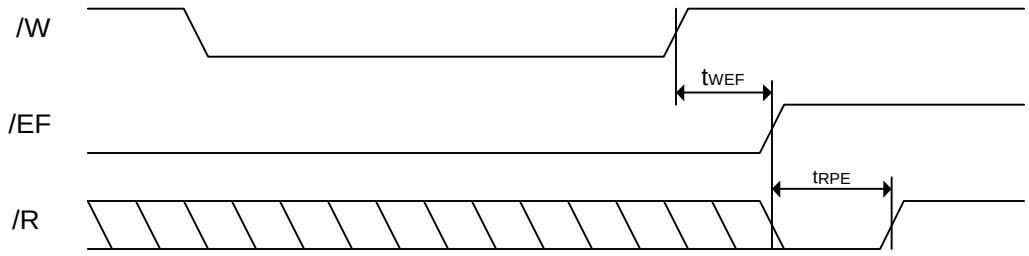
Full Flag Timing



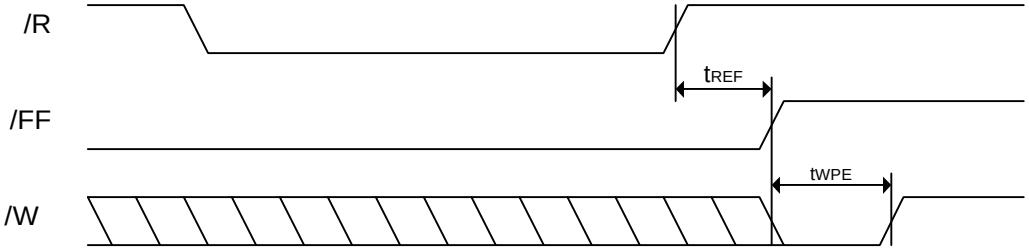
Empty Flag Timing



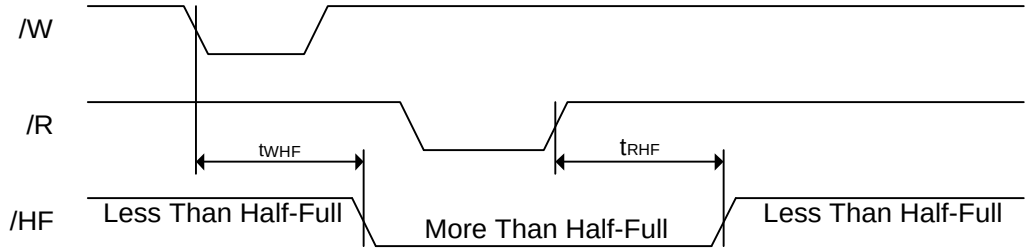
Retranmit



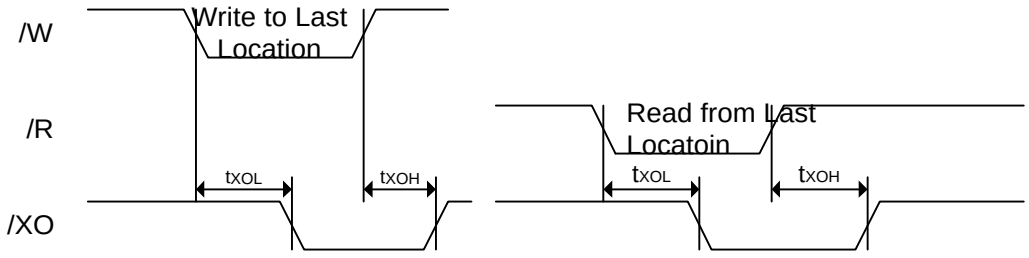
Minimum Timing for an Empty Flag Coincident Read Pulse



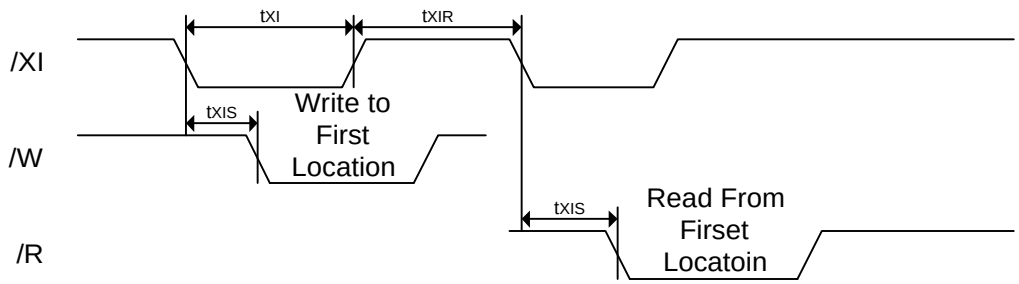
Minimum Timing for an Full Flag Coincident Write Pulse



Half-Full Flag Timing



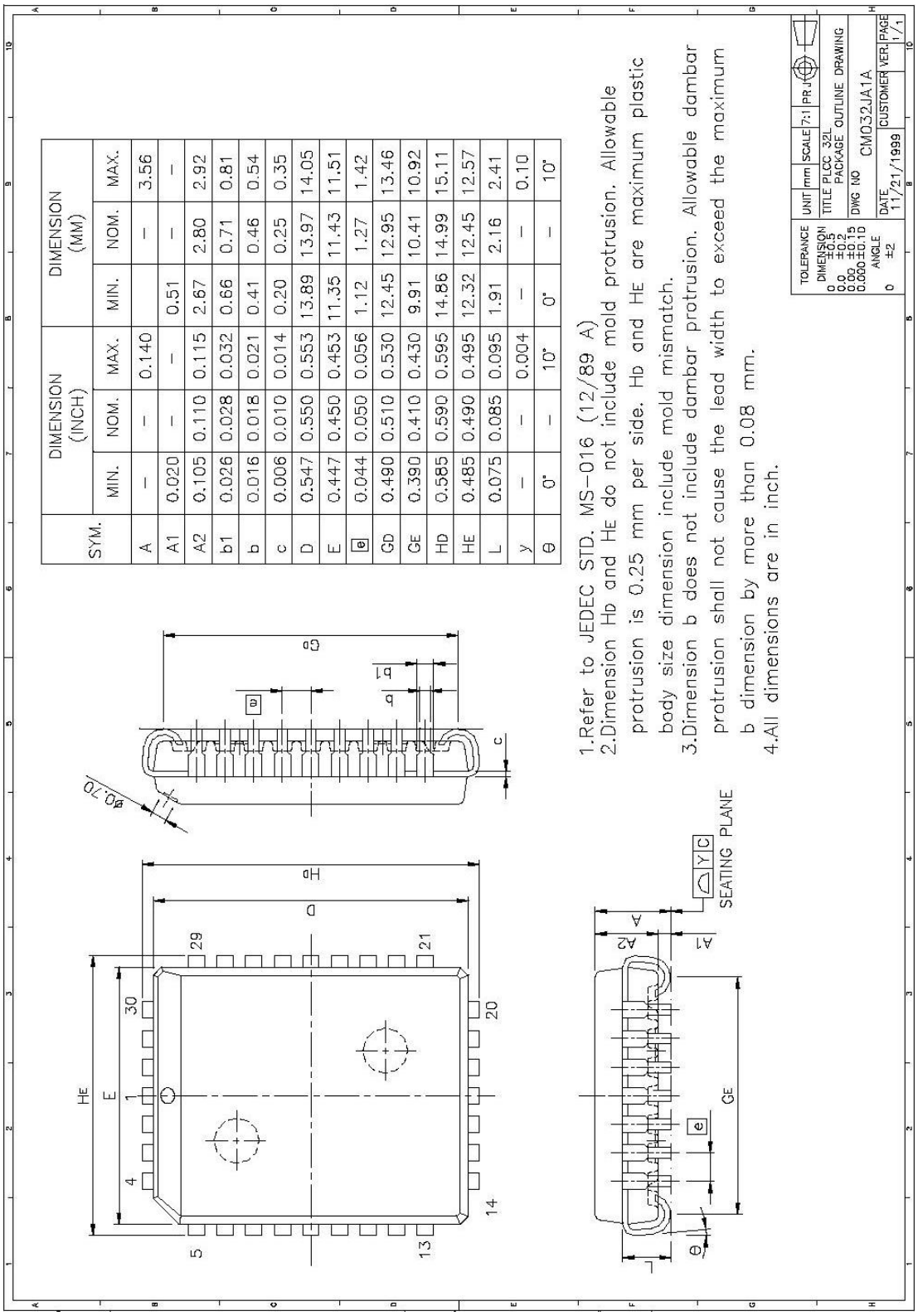
Expansion Out



Expansion In

11.0 Mechanical Drawing

11.1 32-pin PLCC Package



SYM.	DIMENSION (INCH)			DIMENSION (MM)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	0.140		—	3.56
A1	0.020	—	—	0.51	—	—
A2	0.105	0.110	0.115	2.67	2.80	2.92
b1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.021	0.41	0.46	0.54
c	0.006	0.010	0.014	0.20	0.25	0.35
D	0.547	0.550	0.553	13.89	13.97	14.05
E	0.447	0.450	0.453	11.35	11.43	11.51
e	0.044	0.050	0.056	1.12	1.27	1.42
GD	0.490	0.510	0.530	12.45	12.95	13.46
GE	0.390	0.410	0.430	9.91	10.41	10.92
HD	0.585	0.590	0.595	14.86	14.99	15.11
HE	0.485	0.490	0.495	12.32	12.45	12.57
L	0.075	0.085	0.095	1.91	2.16	2.41
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0°	—	10°

CONTACT INFORMATION

Averlogic Technologies Corp.
4F, No. 514, Sec. 2, Cheng Kung Rd., Nei-Hu Dist., Taipei, Taiwan
Tel: +886 2-27915050
Fax: +886 2-27912132
E-mail: sales@averlogic.com.tw
URL: http://www.averlogic.com.tw

Averlogic Technologies, Inc.
90 Great Oaks Blvd. #204, San Jose, CA 95119
USA
Tel: 1 408 361-0400
Fax: 1 408 361-0404
E-mail: sales@averlogic.com
URL: http://www.averlogic.com