5164
HIGH SPEED 8192 x 8-BIT STATIC RAM

	5164-20	5164-25	5164-30	5164-35
Max Access Time (ns)	20	25	30	35
Max Active Current (mA)	120	110	100	100
Max Standby Current (mA)	30	30	30	30

- **Static Operation — No Clock/Refresh Required**
- **Equal Access and Cycle Times — Simplifies System Design**
- **Single +5V Supply**
- **2V Data Retention Option Available**
- **Power Down Mode**
- **TTL Compatible**
- **Common Data Input and Output**
- **28-Pin 300 Mil Plastic Package**

The 5164 is a 65,536-bit high speed static RAM configured as 8K x 8. Easy memory expansion is available with two chip enables ($\overline{CS1}$ and CS2) and an Output Enable ($\overline{OE}$).

The power down feature contributes greatly to system reliability. The device's power consumption is reduced when in this low power standby mode. In fact, 85% system power reduction is achievable in large systems where a majority of the devices are deselected.

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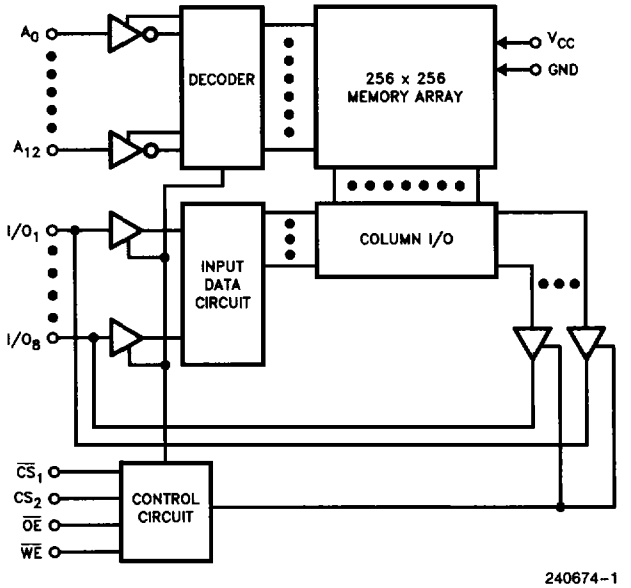
Functional Block Diagram



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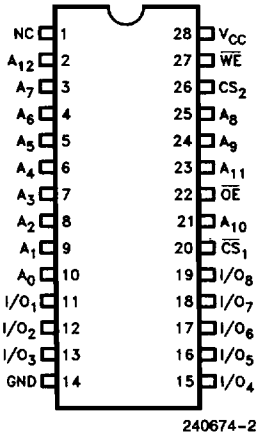
Pin Configurations



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Pin Names

A_0–A_{12}	Address	$\overline{WE}$	Write Enable
I/O_1–I/O_8	Data Input/Output	$\overline{OE}$	Output Enable
$\overline{CS_1}$	Chip Select	GND	Ground
CS_2	Chip Select	V_{CC}	Power

May 1990
Order Number: 240674-002

Device Operation

The 5164 has three control inputs: Two Chip Selects ($\overline{CS1}$, CS2) and Write Enable ($\overline{WE}$). $\overline{WE}$ is the data control pin and should be used to gate data at the I/O pins. When $\overline{CS_1}$ and $\overline{WE}$ inputs are LOW and CS_2 is HIGH, data is written into the memory and reading is accomplished when $\overline{CS_1}$ and $\overline{OE}$ are active LOW, CS_2 active HIGH and $\overline{WE}$ remains inactive or HIGH.

Standby Power

The 5164 is placed in a standby or reduced power consumption mode by applying a high (V_{IH}) to the $\overline{CS_1}$ input or low (V_{IL}) to the CS_2 input. When in standby mode, the device is deselected and the outputs are in a high impedance state, independent of the $\overline{WE}$ input.

Table 1. Mode Selection Truth Table

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	X	Standby	High Z	Standby
X	L	X	X	Standby	High Z	Standby
L	H	L	X	Write	D_{IN}	Active
L	H	H	L	Read	D_{OUT}	Active
L	H	H	H	Read	High Z	Active

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin
Relative to Ground (V_{IN}, V_{OUT}) . . . −1.0V to +7V

Storage Temperature
(Ceramic) (T_{STG}) . . . . . −65°C to +150°C

Power Dissipation (P_D) 1.0W

DC Continuous Output Current (I_{OS}) . . . . . 50 mA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

(Voltage referenced to V_{SS}, T_A = 0°C to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2		V_{CC} + 0.5	V
V_{IL}	Input Low Voltage	−0.5		0.8	V

NOTE:
1. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Min	Max	Unit
C_{IN1}	Input Capacitance (V_{IN} = 0V)		7	pF
C_{OUT}	Output Capacitance (V_{OUT} = 0V)		7	pF

NOTE:
This parameter is sampled and not 100% tested.

D.C. AND OPERATING CHARACTERISTICS

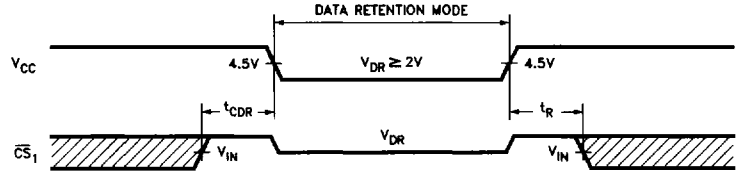
(Recommended Operating Conditions unless otherwise noted)

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{CC}	Operating Current		100	mA	V_{CC} = Max, $\overline{CS}_1$ = V_{IL} CS_2 = V_{IH}, Outputs Open, T_{CYCLE} = Min
I_{SB}	Standby Current		30	mA	V_{CC} = Min to Max $\overline{CS}_1$ = V_{IH} or CS_2 = V_{IL}
I_{SB1}			7	mA	$\overline{CS}_1 \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, V_{CC} = Max
I_{LI}	Input Load Current	−10	10	μA	V_{CC} = Max V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage	−10	10	μA	$\overline{CS}_1$ = V_{IH}, V_{CC} = Max V_{OUT} = GND to V_{CC}
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −4 mA
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 8 mA

DATA RETENTION ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions	
V_{CDR}	Voltage for Data Retention	2			V		
I_{CCDR}	Data Retention Current		95	500	μA	V_{CC} = 2V	$\overline{CS}_1 \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$
			350	750	μA	V_{CC} = 3V	
t_{CDR}	Chip Deselect to Data Retention Time	0			ns		
t_R	Operation Recovery Time	t_{RC}			ns		

Low V_{CC} Data Retention Waveform



A.C. TEST CONDITIONS

Input Pulse Levels ..... GND to 3.0V
Input Rise and Fall Times ..... 5 ns
Timing Reference Level 1.5V

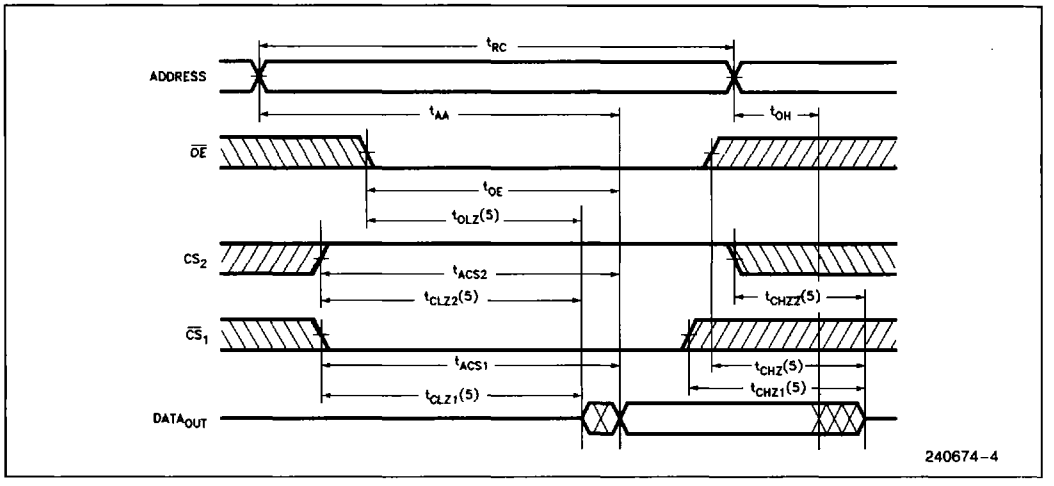
A.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ±10%)

READ CYCLE

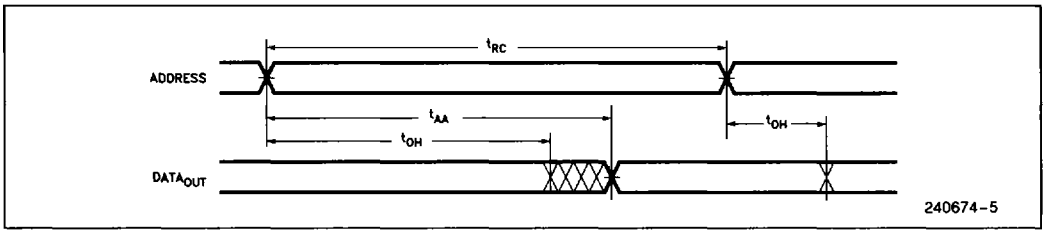
Symbol	Parameter	5164-20		5164-25		5164-30		5164-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	20		25		30		35		ns
t_{AA}	Address Access Time		20		25		30		35	ns
t_{ACS1}	Chip Select 1 Access Time		20		25		30		35	ns
t_{ACS2}	Chip Select 2 Access Time		20		25		30		35	ns
t_{OE}	Output Enable to Output Valid		15		15		20		20	ns
t_{OH}	Output Hold from Address Change	3		3		3		3		ns
t_{CLZ1}	Chip Select 1 to Output in Low Z	5		5		5		5		ns
t_{CLZ2}	Chip Select 2 to Output in Low Z	5		5		5		5		ns
t_{CHZ1}	Chip Select 1 to Output in High Z		15		15		20		20	ns
t_{CHZ2}	Chip Select 2 to Output in High Z		15		15		20		20	ns
t_{OLZ}	Output Enable to Output in Low Z	0		0		0		0		ns
t_{OHZ}	Output Enable to Output in High Z		10		10		15		20	ns
t_{PU}	Chip Selection to Power Up Time	0		0		0		0		ns
t_{PD}	Chip Deselection to Power Down Time		20		25		30		35	ns

NOTES:
1. All Read Cycle timings are referenced from the last valid address to the first transitioning address.
2. At any given temperature and voltage, t_{CHZ}(Max) is less than t_{CLZ}(Min), both for a given device and from device to device.

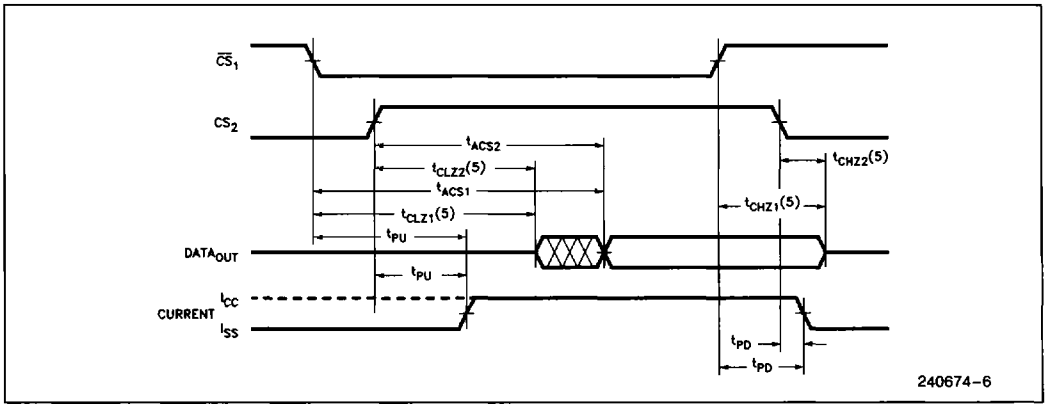
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



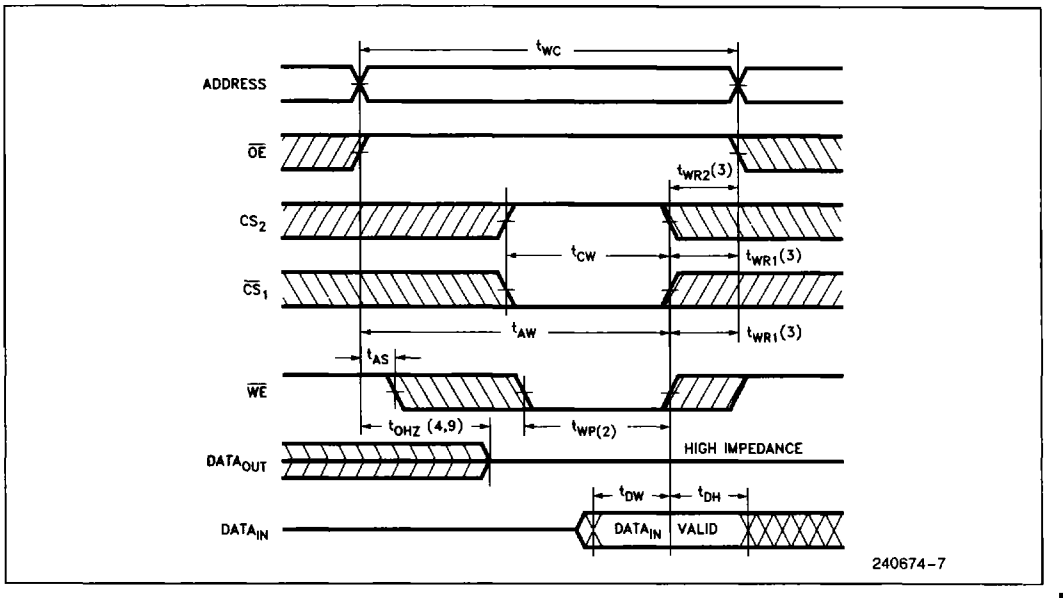
NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{CS}_1$ transition low and CS_2 transition high.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±500 mV from steady state.

A.C. CHARACTERISTICS (Continued)

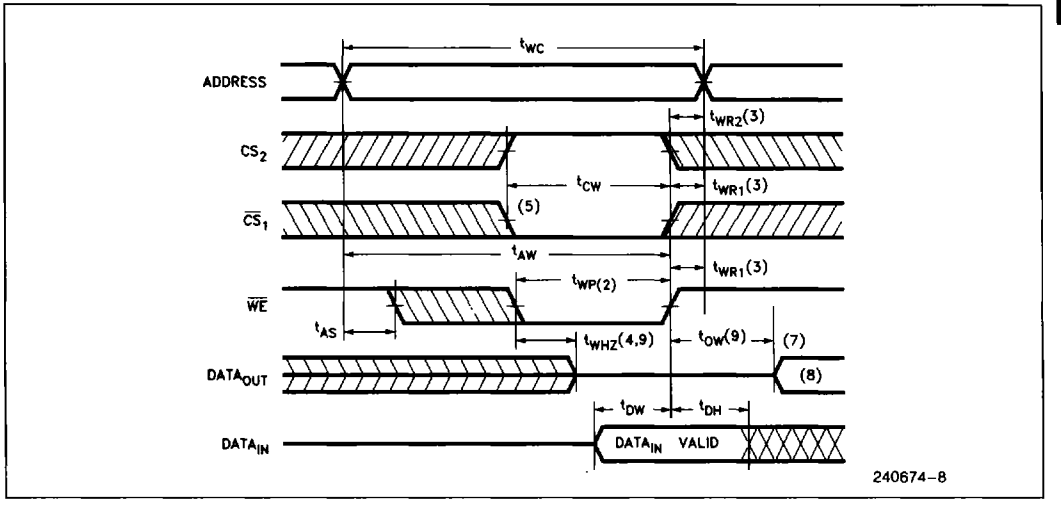
WRITE CYCLE

Symbol	Parameter	5164-20		5164-25		5164-30		5164-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	20		25		30		35		ns
t_{CW1}	Chip Selection 1 to End of Write	15		20		25		30		ns
t_{CW2}	Chip Selection 2 to End of Write	15		20		25		30		ns
t_{AW}	Address Valid to End of Write	15		20		25		30		ns
t_{AS}	Address Set-Up Time	0		0		0		0		ns
t_{WP}	Write Pulse Width	15		20		25		25		ns
t_{WR}	Write Recovery Time	0		0		0		0		ns
t_{DW}	Data Valid to End of Write	15		15		15		15		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{WHZ}	Write Enable to Output in High Z	0	12	0	15	0	15	0	15	ns
t_{OW}	Output Active from End of Write	0		0		0		0		ns

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)



TIMING WAVEFORM OF WRITE CYCLE NO. 2(1,6)



NOTES:
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS_1}$ and a high CS_2.
3. $t_{WR1,2}$ is measured from the earlier of $\overline{CS_1}$ or $\overline{WE}$ going high or CS_2 going low to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS_1}$ low transition or CS_2 high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL}).
7. $DATA_{OUT}$ is the same phase of write data of this write cycle, as long as address does not change.
8. If $\overline{CS_1}$ is low and CS_2 is high during this period, I/O pins are in the output state. Data input signals must not be applied.
9. Transition is measured ± 200 mV from steady state.

28-PIN PLASTIC DIP