8A, 60V, 0.300 Ohm, ESD Rated, Logic Level, P-Channel Power MOSFET

These products are P-Channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA49203.

Ordering Information

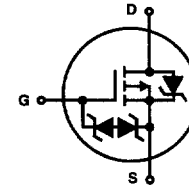
PART NUMBER	PACKAGE	BRAND
RFD8P06LE	TO-251AA	F8P6LE
RFD8P06LESM	TO-252AA	F8P6LE
RFP8P06LE	TO-220AB	FP8P06LE

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in the tape and reel, i.e., RFD8P06LESM9A.

Features

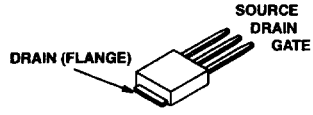
- 8A, 60V
- $r_{DS(ON)} = 0.300\Omega$
- 2kV ESD Protected
- Temperature Compensating PSPICE® Model
- PSPICE Thermal Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature

Symbol

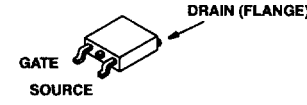


Packaging

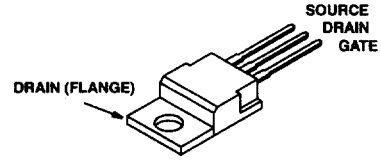
JEDEC TO-251AA



JEDEC TO-252AA



JEDEC TO-220AB



Absolute Maximum Ratings $T_C = 25^oC$ Unless Otherwise Specified

		RFD8P06LE, RFD8P06LESM, RFP8P06LE	UNITS
Drain to Source Voltage	V_{DS}	-60	V
Drain to Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	-60	V
Continuous Drain Current			
$T_C = 25^oC$	I_D	-8	A
$T_C = 100^oC$	I_D	-6.3	A
Pulsed Drain Current	I_{DM}	See Figure 5	
Gate to Source Voltage	V_{GS}	±10	V
Maximum Power Dissipation	P_D	48	W
Dissipation Derating Factor		0.32	W/°C
Single Pulse Avalanche Energy Rating	E_{AS}	See Figure 6	
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	°C
Maximum Lead Temperature for Soldering (0.063in (1.6mm) from case for 10s)	T_L	300	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$ Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 11)		-60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA (Figure 12)		-1	-	-2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -60V, V_{GS} = 0V	$T_J = 25^oC$	-	-	-1	μA
			$T_J = 150^oC$	-	-	-50	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±10V		-	-	±10	μA
On Resistance (Note 1)	$r_{DS(ON)}$	I_D = 8A, V_{GS} = -5V (Figure 9, 10)		-	-	0.300	Ω
		I_D = 8A, V_{GS} = -4.5V (Figure 9, 10)		-	-	0.330	Ω
Turn-On Time	t_{ON}	V_{DD} = -30V, $I_D \cong$ 8A, R_{GS} = 9.1Ω, R_L = 3.75Ω (Figure 13)		-	-	90	ns
Turn-On Delay Time	$t_{d(ON)}$			-	10	-	ns
Rise Time	t_r			-	50	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	30	-	ns
Fall Time	t_f			-	20	-	ns
Turn-Off Time	t_{OFF}			-	-	75	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0 to -10V	V_{DD} = -48V, $I_D \cong$ 8A, R_L = 6Ω, $I_{g(REF)}$ = -0.2mA (Figure 14)	-	25	30	nC
Gate Charge at -5V	$Q_{g(-5)}$	V_{GS} = 0 to -5V		-	15	18	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0 to -1V		-	1.2	1.5	nC
Input Capacitance	C_{ISS}	V_{DS} = -25V, V_{GS} = 0V, f = 1MHz (Figure 15)		-	675	-	pF
Output Capacitance	C_{OSS}			-	175	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	50	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	3.125	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-251AA, TO-252AA		-	-	100	°C/W
		TO-220AB				80	°C/W

Source to Drain Diode Specifications $T_C = 25^oC$ Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 1)	V_{SD}	$T_J = 25^oC$, I_{SD} = -8A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	$T_J = 25^oC$, I_{SD} = -8A, dI_{SD}/dt = 100A/μs	-	-	125	ns

NOTE:

2. Pulse Test: Pulse width ≤300μs, Duty Cycle ≤2%.

Typical Performance Curves Unless Otherwise Specified

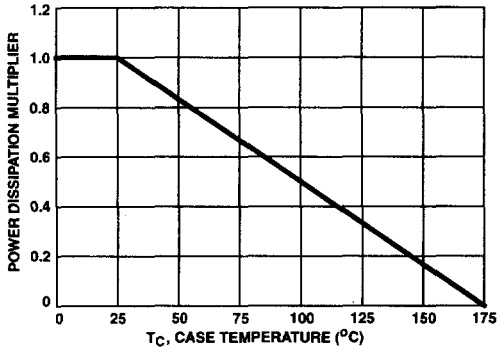


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

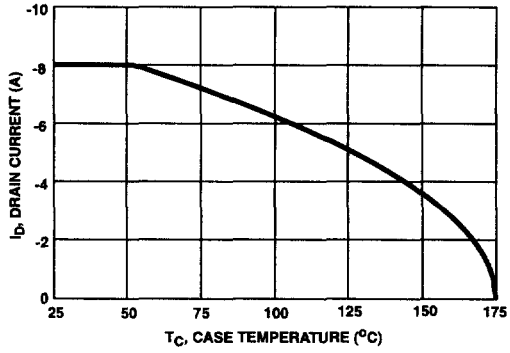


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

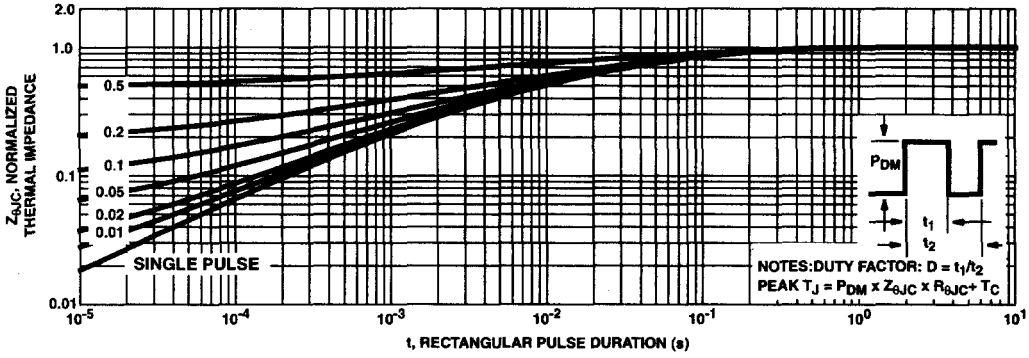


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

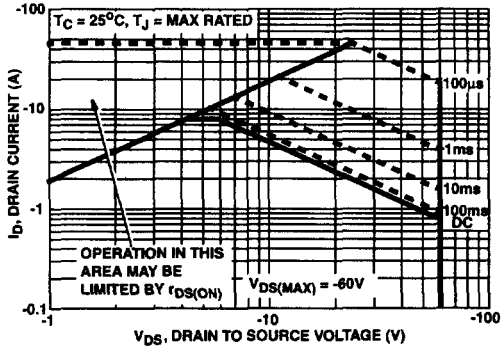


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

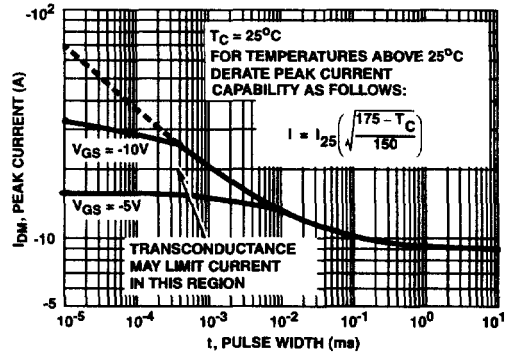
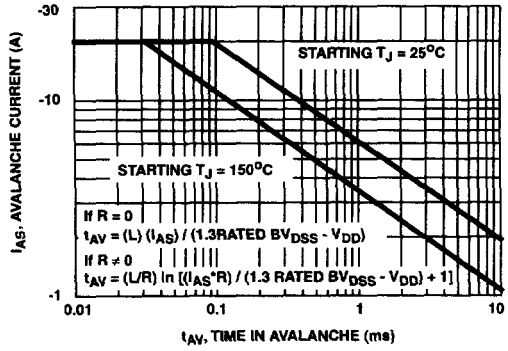


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

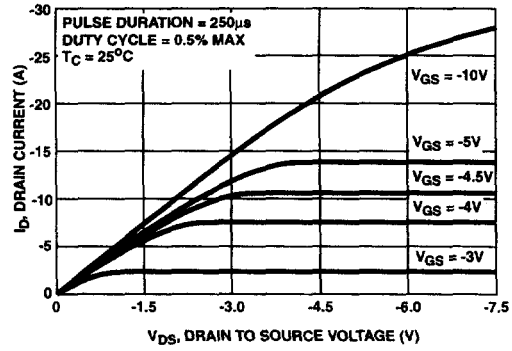


FIGURE 7. SATURATION CHARACTERISTICS

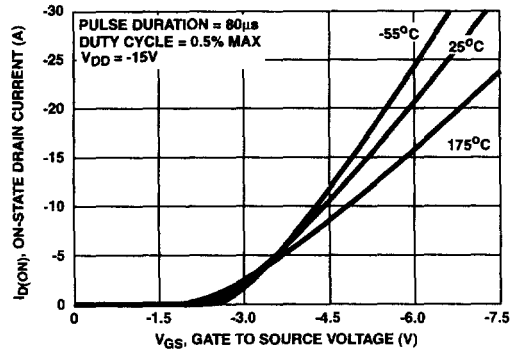


FIGURE 8. TRANSFER CHARACTERISTICS

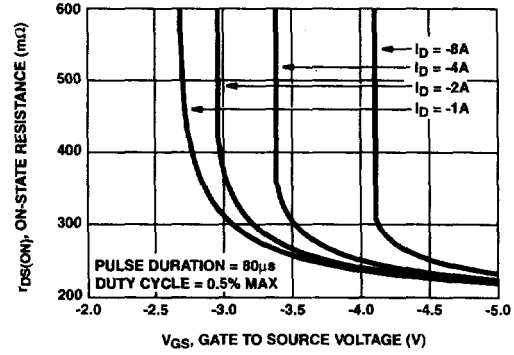


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

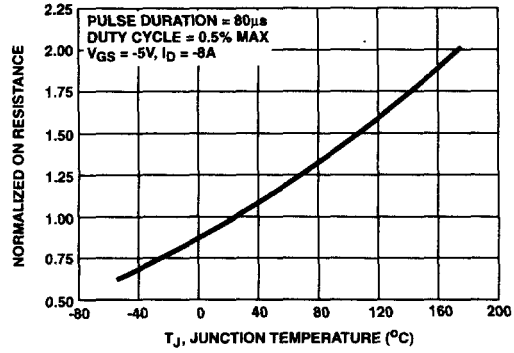


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

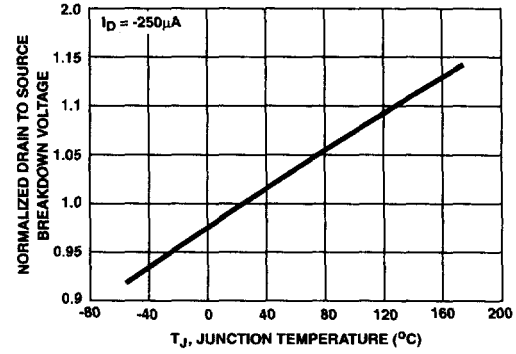


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

7 P-CH LOGIC LEVEL

Typical Performance Curves Unless Otherwise Specified

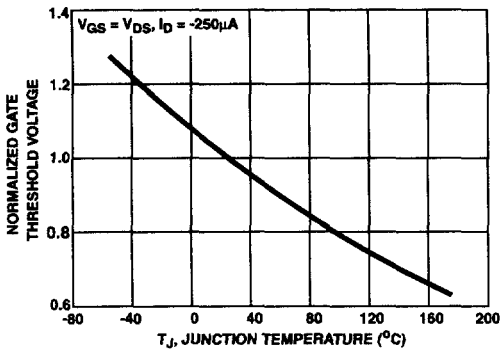


FIGURE 12. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

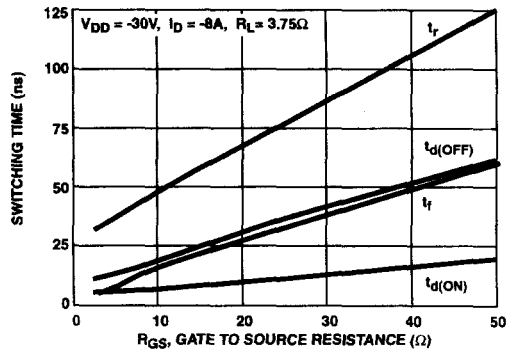
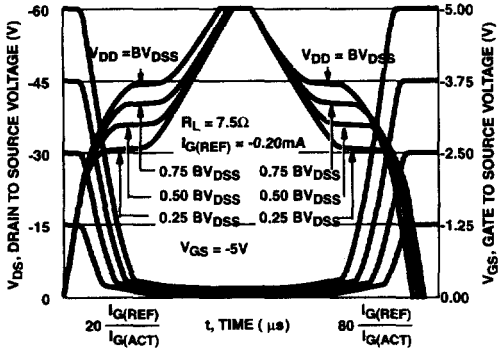


FIGURE 13. SWITCHING TIME AS A FUNCTION OF GATE RESISTANCE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 14. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

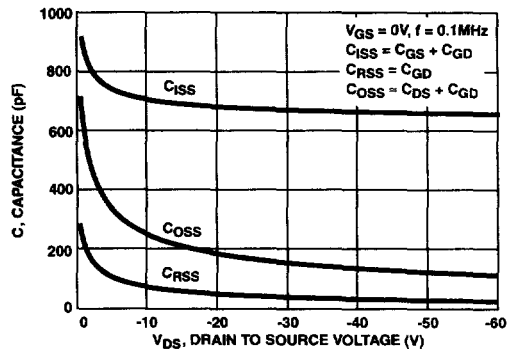


FIGURE 15. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE