M5M5256BP,BFP,BKP-10L-I, -12L-I, -15L-I
-10LL-I,-12LL-I,-15LL-I

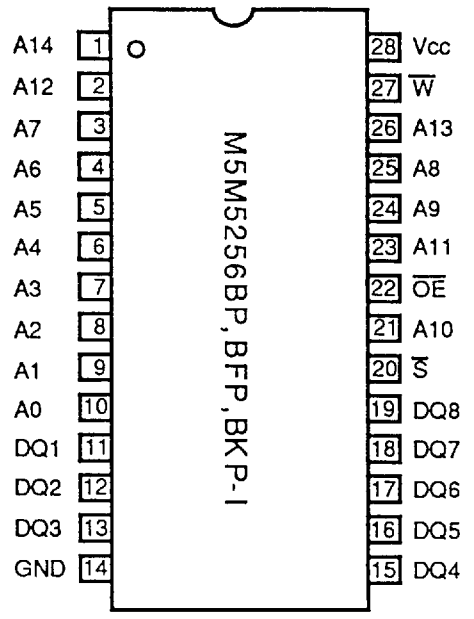
262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

This M5M5256BP,BFP,BKP is a 262,144-bit CMOS static RAM organized as 32,768-words by 8-bits which is fabricated using high-performance double polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high-density and low-power static RAM. It is ideal for the memory systems which require simple interface.

The stand-by current is low enough for a battery back-up application. It is mounted in a standard 28 pin package and configured in an industrial standard 32K×8-bit pinout.

PIN CONFIGURATION (TOP VIEW)



Outline 28P4 (BP)
28P2W-C (BFP)
28P4Y (BKP)

FEATURE

Type	Access time (max)	Power supply current	
		Active (max)	Stand-by (-40~70℃)
M5M5256BP,BFP,BKP-10L-I M5M5256BP,BFP,BKP-12L-I M5M5256BP,BFP,BKP-15L-I	100ns 120ns 150ns	70mA	100 μA (Vcc=5.5v) 50 μA (Vcc=3.0v)
M5M5256BP,BFP,BKP-10LL-I M5M5256BP,BFP,BKP-12LL-I M5M5256BP,BFP,BKP-15LL-I	100ns 120ns 150ns		20 μA (Vcc=5.5v) 10 μA (Vcc=3.0v)

- Single +5V Power Supply
- No Clocks, No Refresh
- Data-Hold on +2V Power Supply
- Directly TTL Compatible: All Inputs and Outputs
- Three-State Outputs: OR-tie Capability
- Simple Memory Expantion by $\overline{S}$
- $\overline{OE}$ Prevents Data Contention in the I/O Bus
- Common Data I/O
- Extended operating temperature (-40~85℃)
- PACKAGE
  - M5M5256BP ..... 28 pin 600 mil DIP
  - M5M5256BKP ..... 28 pin 300 mil DIP
  - M5M5256BFP ..... 28 pin Small Outline Package (SOP)

APPLICATION

Small Capacity Memory Units

M5M5256BP,BFP,BKP-10L-I, -12L-I, -15L-I -10LL-I,-12LL-I,-15LL-I

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FUNCTION

The operation mode of the M5M5256BP,BFP,BKP is determined by a combination of the device control inputs $\overline{S}$,$\overline{W}$ and $\overline{OE}$. Each mode is summariezed in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$,$\overline{S}$,whichever occurs first,requiring the set-up and hold time relative to these edge to be maintained.The output enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level,the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

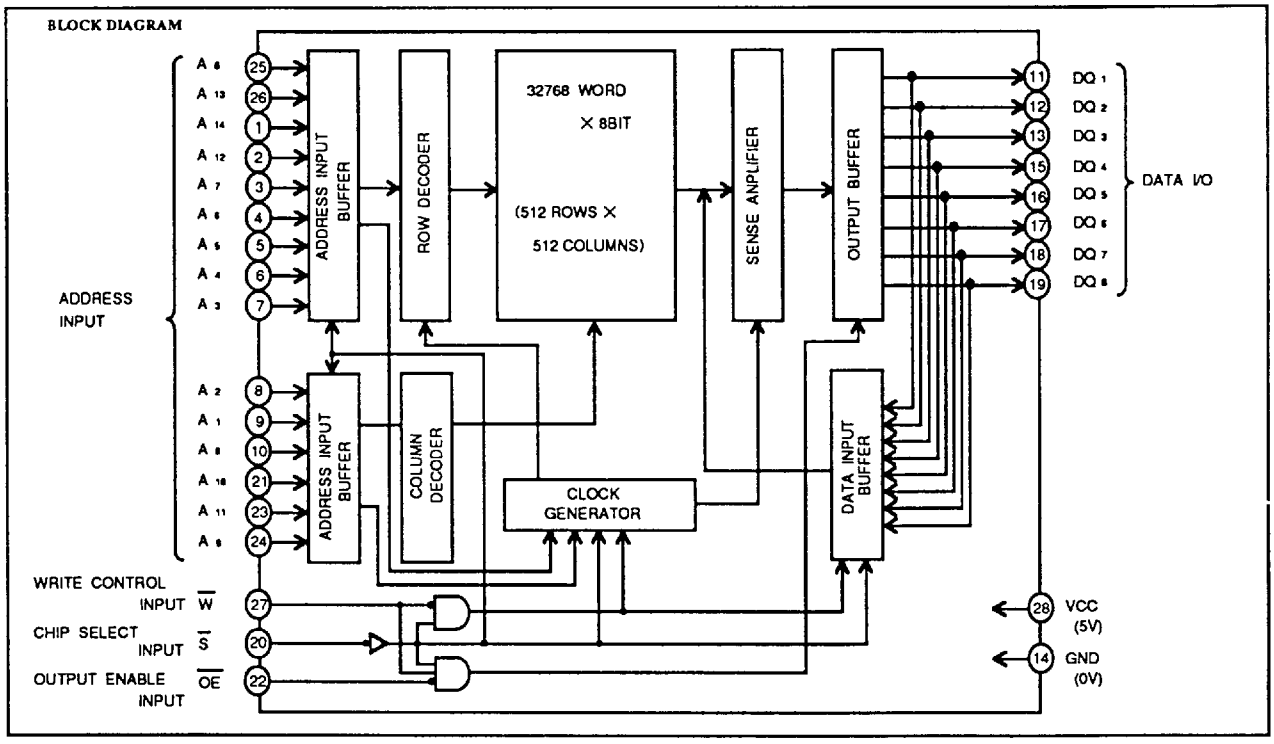
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state.

When setting $\overline{S}$ at a high level,the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expantion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as Icc3 or Icc4, and the memory data can be held +2V power supply,enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Standby
L	L	X	Write	D_{IN}	Active
L	H	L	Read	D_{OUT}	Active
L	H	H		High-impedance	Active

BLOCK DIAGRAM



M5M5256BP,BFP,BKP-10L-I, -12L-I, -15L-I -10LL-I,-12LL-I,-15LL-I

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Units
V_{CC}	Supply voltage	With respect to GND	-0.3~7	V
V_I	Input voltage		-0.3~Vcc+0.3	V
V_O	Output voltage		0~Vcc	V
Pd	Power dissipation	Ta=25℃	700	mW
Topr	Operating temperature		-40~85	℃
Tstg	Storage temperature		-65~150	℃

ELECTRICAL CHARACTERISTICS (Ta=-40~85℃, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Conditions		Limits Min	Limits Typ	Limits Max	Units
V_{IH}	High-level input voltage			2.2		Vcc+0.3V	V
V_{IL}	Low-level input voltage			-0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH}=-1mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL}=2mA				0.4	V
I_I	Input leakage current	V_I=0~Vcc				±1	μA
I_O	Output leakage current	$\overline{S}$=V_{IH} or $\overline{OE}$=V_{IH}, $V_{I/O}$=0-Vcc				±1	μA
I_{CC1}	Active supply current (AC,MOS level)	$\overline{S}$<0.2V,$\overline{W}$>Vcc-0.2V,Output open Other inputs<0.2V or >Vcc-0.3V Min.cycle			30	65	mA
I_{CC2}	Active supply current (AC,TTL level)	$\overline{S}$=V_{IL} ,$\overline{W}$=V_{IH}, Output open Other inputs=V_{IH} or V_{IL} Min.cycle			35	70	mA
I_{CC3}	Stand by supply current	$\overline{S}$≧Vcc-0.2V Other inputs=0~Vcc	BP,BFP.BKP-L			100 *1	μA
			-I			200 *2	μA
			BP,BFP,BKP-LL			20 *1	μA
			-I			40 *2	μA
I_{CC4}	Stand by supply current	$\overline{S}$=V_{IH},Other inputs=0~Vcc				3	mA
C_I	Input capacitance (Ta=25℃)	V_I=GND,V_I=25mVrms,f=1MHz				6	pF
C_O	Output capacitance (Ta=25℃)	V_O=GND,V_o=25mVrms,f=1MHz				8	pF

*1: Ta=-40~70℃
*2: Ta=70~85℃

Note 1: Direction for current flowing into IC is indicated as positive (no mark)
Note 2: Typical value is Vcc=5V,Ta=25℃

SWITCHING CHARACTERISTICS (Ta=-40~85°C, Vcc=5V±10%, unless otherwise noted)

READ CYCLE

Symbol	Parameter	M5M5256-10L-I M5M5256-10LL-I		M5M5256-12L-I M5M5256-12LL-I		M5M5256-15L-I M5M5256-15LL-I		Units
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	100		120		150		ns
$t_{a(A)}$	Address access time		100		120		150	ns
$t_{a(S)}$	Chip select access time		100		120		150	ns
$t_{a(OE)}$	Output enable access time		50		60		75	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high		35		40		45	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		35		40		45	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	10		10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	10		10		10		ns
$t_{v(A)}$	Data valid time after address	20		20		20		ns

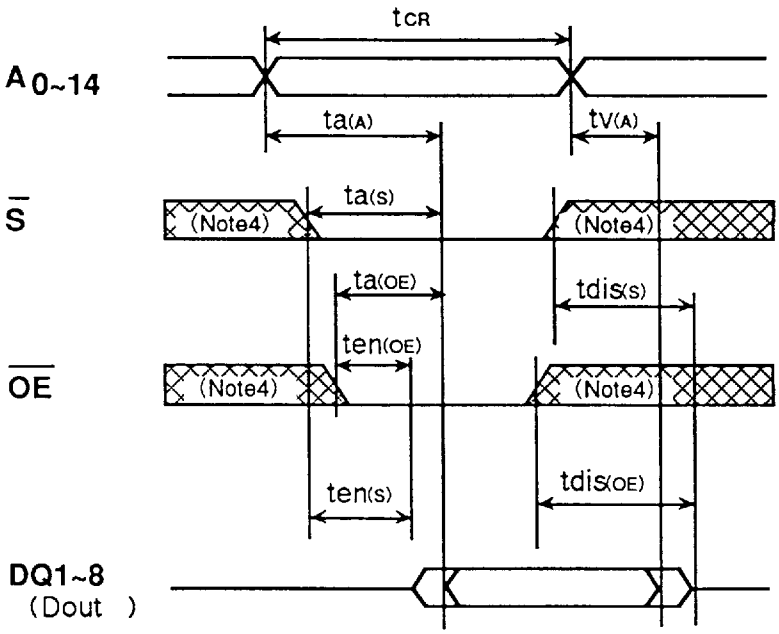
TIMING REQUIREMENTS (Ta=-40~85°C, Vcc=5V±10%, unless otherwise noted)

WRITE CYCLE

Symbol	Parameter	M5M5256-10L-I M5M5256-10LL-I		M5M5256-12L-I M5M5256-12LL-I		M5M5256-15L-I M5M5256-15LL-I		Units
		Min	Max	Min	Max	Min	Max	
t_{cw}	Write cycle time	100		120		150		ns
$t_{w(W)}$	Write pulse width	60		70		80		ns
$t_{su(A)}$	Address set up time	0		0		0		ns
$t_{su(A-\overline{WH})}$	Address set up time with respect to $\overline{W}$ high	80		85		90		ns
$t_{su(S)}$	Chip select set up time	80		85		90		ns
$t_{su(D)}$	Data set up time	35		40		50		ns
$t_{h(D)}$	Data hold time	0		0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		0		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low		35		40		45	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		35		40		45	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	10		10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	10		10		10		ns

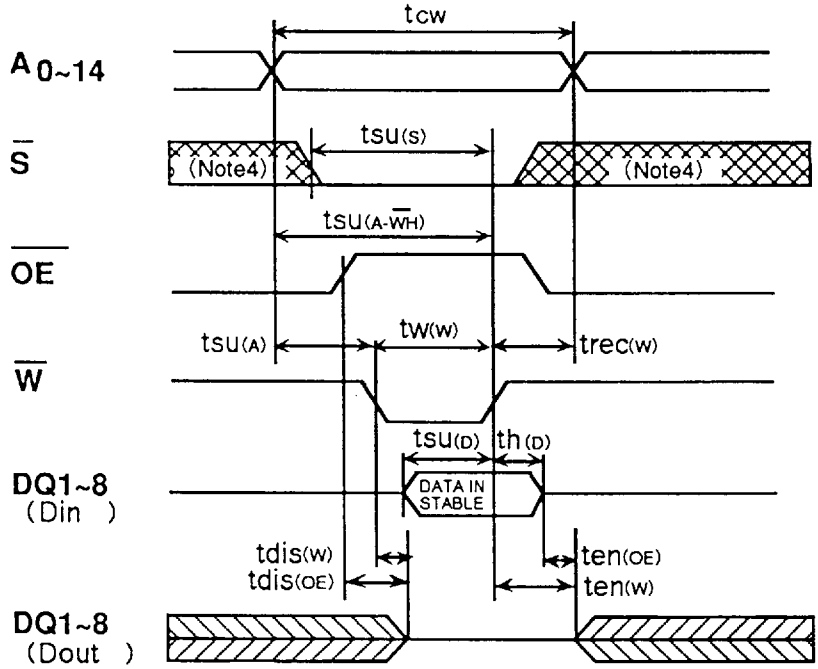
TIMING DIAGRAMS

Read cycle

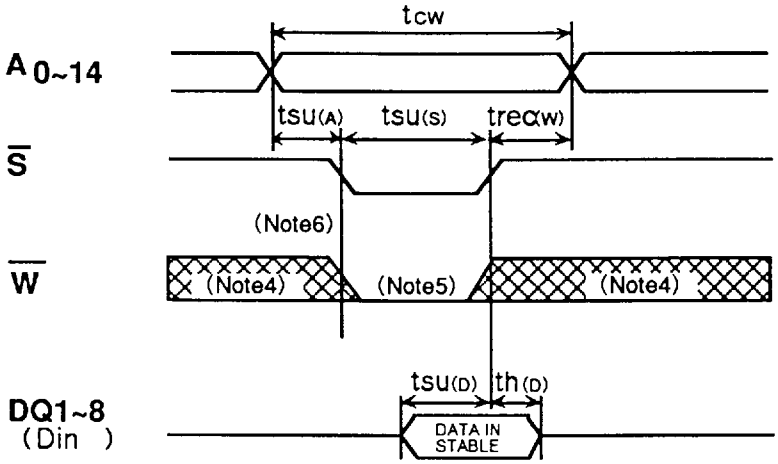


W="H" level

Write cycle (W control mode)



Write cycle ($\overline{S}$ control mode)



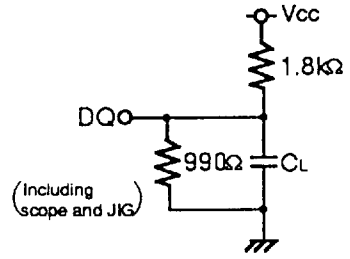


Fig.1 Output load

Note 3: Test condition

Input pulse level.... V_{IH} =2.4V, V_{IL} =0.6V

Input rise and fall time.... 10ns

Reference level.... V_{OH} = V_{OL} =1.5V

Transition is measured ±500mV from steady state voltage. (for t_{en}, t_{dis})

Output loads..... Fig.1, C_L =100pf (BP,BFP,BKP-10L-I,-12L-I,-15L-I,-10LL-I, -12LL-I,-15LL-I)

C_L =5pf (for t_{en}, t_{dis})

Note 4: Hatching indicates the state isdon't care.

Note 5: Writing is executed in overlap of $\overline{S}$ and $\overline{W}$ low.

Note 6: If $\overline{W}$ goes low simultaneously with or prior to S,the output remains in the high-impedance state.

Note 7: Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (Ta=-40~85℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Units
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S})}$	Chip select input $\overline{S}$	2.2V≦$V_{CC(PD)}$		2.2			V
		2V≦$V_{CC(PD)}$≦2.2V			$V_{CC(PD)}$		
$I_{CC(PD)}$	Power down supply current	V_{CC}=3V Other inputs=3V	BP,BFP,BKP-L -I			50 *1	μA
						100*2	μA
			BP,BFP,BKP-LL -I			* 10 *1	μA
						20*2	μA

* Ta=25℃,$I_{CC(PD)}$=1 μA

*1: Ta=-40~70℃
*2: Ta=70~85℃

TIMING REQUIREMENTS (Ta=-40~85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Units
			Min	Typ	Max	
$t_{su(PD)}$	Power down set up time		0			ns
$t_{rec(PD)}$	Power down recovery time		t_{CR}			ns

POWER DOWN CHARACTERISTICS