CD74FCT543T, CD74FCT544T, CD74FCT2543T

December 1996

Fast CMOS Latched Transceivers

Features

- **Advanced 0.8 micron CMOS Technology**
- **These Devices are Pin Compatible With Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption**
- **25Ω Series Resistor on All Outputs (CD74FCT2543T)**
- **TTL Input and Output Levels**
- **Low Ground Bounce Outputs**
- **Extremely Low Static Power**
- **Hysteresis on All Inputs**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT543ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT543ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT543CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT543CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT543DTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT543DTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT543TM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT543TQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT544ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT544ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT544CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT544CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT544TM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT544TQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2543ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2543ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2543CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2543CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2543TM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2543TQM	-40 to 85	24 Ld QSOP	M24.15-P

NOTE: QSOP is commonly known as SSOP.

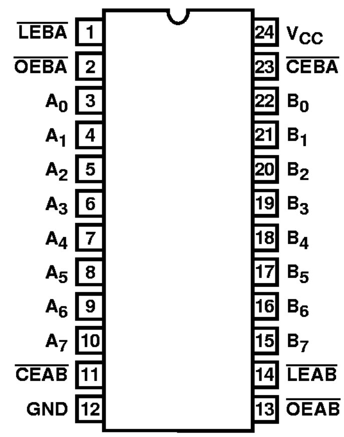
When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Description

The devices are 8-bit wide non-inverting transceivers designed with two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from A_0-A_7 or to take data from B_0-B_7, as indicated in the Truth Table. With $\overline{CEAB}$ LOW, a LOW signal makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the three-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs. The CD74FCT543T is a non-inverting version of the CD74FCT544T.

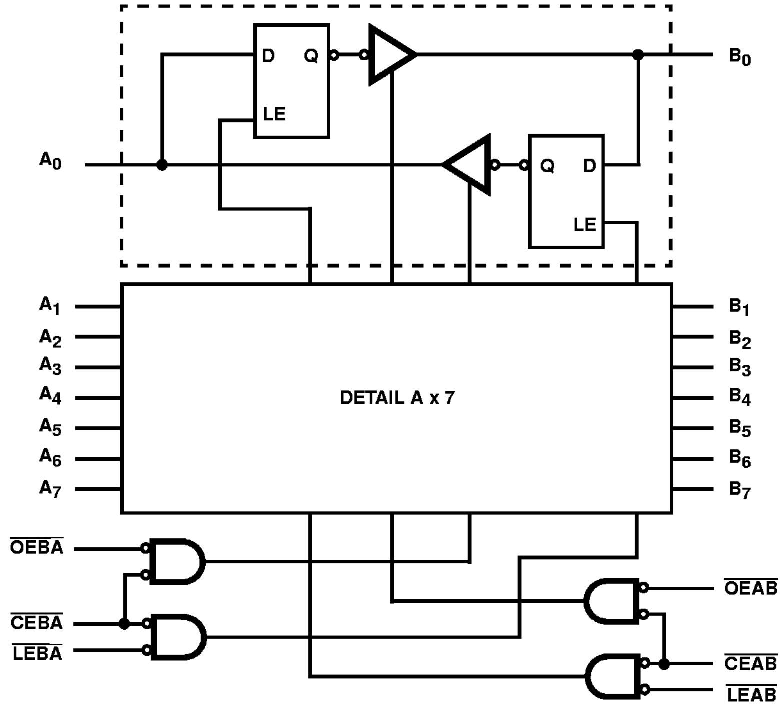
Pinout

CD74FCT543T, CD74FCT544T, CD74FCT2543T
(QSOP, SOIC)
TOP VIEW



Functional Block Diagram

CD74FCT543T, CD74FCT2543T



TRUTH TABLE (NON-INVERTING)

For A-to-B (Symmetric with B-to-A) (NOTES 1, 2)

INPUTS			LATCH STATUS	OUTPUT BUFFERS
$\overline{\text{CEAB}}$	$\overline{\text{LEAB}}$	$\overline{\text{OEAB}}$	A-TO-B	B_0-B_7
H	-	-	Storing	High-Z
-	H	-	Storing	-
-	-	H	-	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs (Note 3)

NOTES:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   - = Don't Care or Irrelevant
2. A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$ and $\overline{\text{OEBA}}$.
3. Before $\overline{\text{LEAB}}$ LOW-to-HIGH Transition

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{\text{OEAB}}$	A-to-B Output Enable Input (Active LOW)
$\overline{\text{OEBA}}$	B-to-A Output Enable Input (Active LOW)
$\overline{\text{CEAB}}$	A-to-B Enable Input (Active LOW)
$\overline{\text{CEBA}}$	B-to-A Enable Input (Active LOW)
$\overline{\text{LEAB}}$	A-to-B Latch Enable Input (Active LOW)
$\overline{\text{LEBA}}$	B-to-A Latch Enable Input (Active LOW)
A_0-A_7	A-to-B Data Inputs or B-to-A Three-State Outputs
B_0-B_7	B-to-A Data Inputs or A-to-B Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only. . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 4) θ_{JA} (°C/W)
SOIC Package 75
QSOP Package 100
Maximum Junction Temperature . . . . 150°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.3	0.50	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA (25Ω Only)	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max (Except I/O Pins)	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max (Except I/O Pins)	V_{IN} = GND	-	-	-1	µA
Input HIGH Current	I_{IH}	(I/O Pins Only) V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	(I/O Pins Only) V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Ouput Current	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V			1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V			-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 7), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 8)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 8)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Curretn per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 9)	-	0.5	2.0	mA

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
Supply Current per Input per MHz (Note 10)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/ MHz
Total Power Supply Current (Note 12)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz (LEAB) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} f_I = 5MHz One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	1.5	3.5 (Note 11)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	2.0	5.5 (Note 11)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz (LEAB) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} Eight Bits Toggling f_I = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	3.8	7.3 (Note 11)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	6.0	16.3 (Note 11)	mA

Switching Specifications Over Operating Range

PARAMETER	SYM-BOL	(NOTE 13) TEST CONDITIONS	T		AT		CT		DT		UNITS
			(NOTE 14) MIN	MAX	(NOTE 14) MIN	MAX	(NOTE 14) MIN	MAX	(NOTE 14) MIN	MAX	
CD74FCT543T											
Propagation Delay Transparent Mode A_N to B_N or B_N to A_N	t_{PLH}, t_{PHL}	C_L = 50 pF R_L = 500Ω	2.5	8.5	2.5	6.5	2.5	5.3	2.5	4.4	ns
Propagation Delay $\overline{LEBA}$ to A_N, $\overline{LEAB}$ to B_N	t_{PLH}, t_{PHL}	C_L = 50 pF R_L = 500Ω	2.5	12.5	2.5	8.0	2.5	7.0	2.5	5.0	ns
Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn $\overline{CEBA}$ or $\overline{CEAB}$ to A_N or B_N	t_{PZH}, t_{PZL}	C_L = 50 pF R_L = 500Ω	2.0	12.0	2.0	9.0	2.0	8.0	2.0	5.4	ns
Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_N or B_N $\overline{CEBA}$ or $\overline{CEAB}$ to A_N or B_N (Note 15)	t_{PZH}, t_{PZL}	C_L = 50 pF R_L = 500Ω	2.0	9.0	2.0	7.5	2.0	6.5	2.0	4.3	ns
Setup Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$	t_{SU}	C_L = 50 pF R_L = 500Ω	3.0	-	2.0	-	2.0	-	1.5	-	ns
Hold Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$	t_H	C_L = 50 pF R_L = 500Ω	2.0	-	2.0	-	2.0	-	1.5	-	ns
$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW (Note 15)	t_W	C_L = 50 pF R_L = 500Ω	5.0	-	5.0	-	5.0	-	3.0	-	ns
CD74FCT544T, CD74FCT2543T											
Propagation Delay Transparent Mode A_N to B_N or B_N to A_N	t_{PLH}, t_{PHL}	C_L = 50 pF R_L = 500Ω	2.5	8.5	2.5	6.5	2.5	5.3	-	-	ns
Propagation Delay $\overline{LEBA}$ to A_N, $\overline{LEAB}$ to B_N	t_{PLH}, t_{PHL}	C_L = 50 pF R_L = 500Ω	2.5	12.5	2.5	8.0	2.5	7.0	-	-	ns

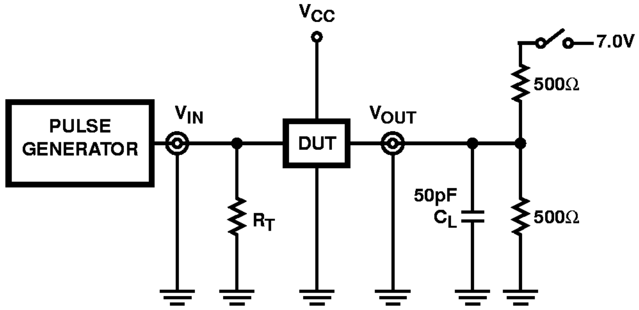
Switching Specifications Over Operating Range (Continued)

PARAMETER	SYM-BOL	(NOTE 13) TEST CONDITIONS	T (NOTE 14) MIN	T MAX	AT (NOTE 14) MIN	AT MAX	CT (NOTE 14) MIN	CT MAX	DT (NOTE 14) MIN	DT MAX	UNITS
Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn $\overline{CEBA}$ or $\overline{CEAB}$ to A_N or B_N	t_{PZH}, t_{PZL}	C_L = 50 pF R_L = 500Ω	2.0	12.0	2.0	9.0	2.0	8.0	-	-	ns
Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_N or B_N $\overline{CEBA}$ or $\overline{CEAB}$ to A_N or B_N (Note 15)	t_{PZH}, t_{PZL}	C_L = 50 pF R_L = 500Ω	2.0	9.0	2.0	7.5	2.0	6.5	-	-	ns
Setup Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$	t_{SU}	C_L = 50 pF R_L = 500Ω	3.0	-	2.0	-	2.0	-	-	-	ns
Hold Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$	t_H	C_L = 50 pF R_L = 500Ω	2.0	-	2.0	-	2.0	-	-	-	ns
$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW (Note 15)	t_W	C_L = 50 pF R_L = 500Ω	5.0	-	5.0	-	5.0	-	-	-	ns

NOTES:

5. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
6. Typical values are at V_{CC} = 5.0V, 25^{o}C ambient and maximum loading.
7. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
8. This parameter is determined by device characterization but is not production tested.
9. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
13. See test circuit and wave forms.
14. Minimum limits are guaranteed but not tested on Propagation Delays.
15. This parameter is guaranteed but not production tested.

Test Circuits and Waveforms



NOTE:

16. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

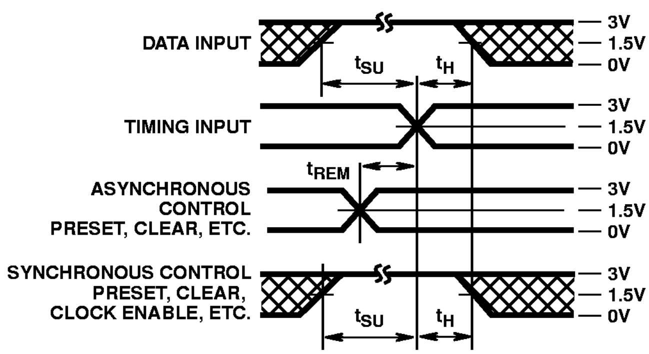


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

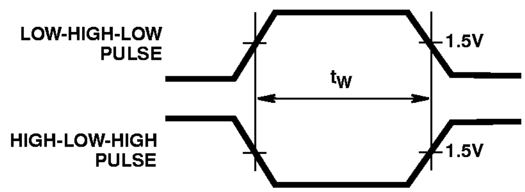


FIGURE 3. PULSE WIDTH

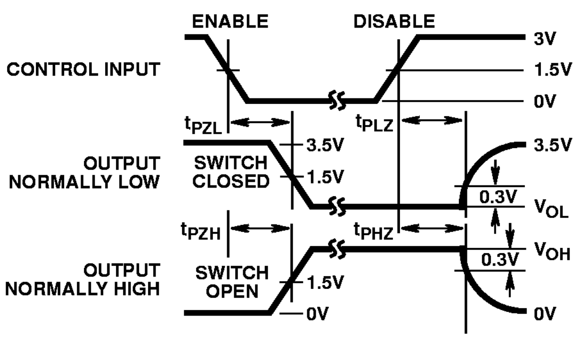


FIGURE 4. ENABLE AND DISABLE TIMING

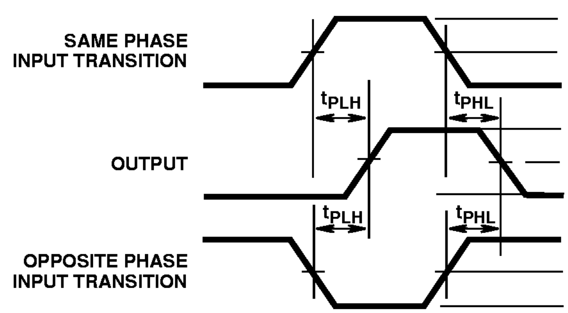


FIGURE 5. PROPAGATION DELAY