ANALOG DEVICES

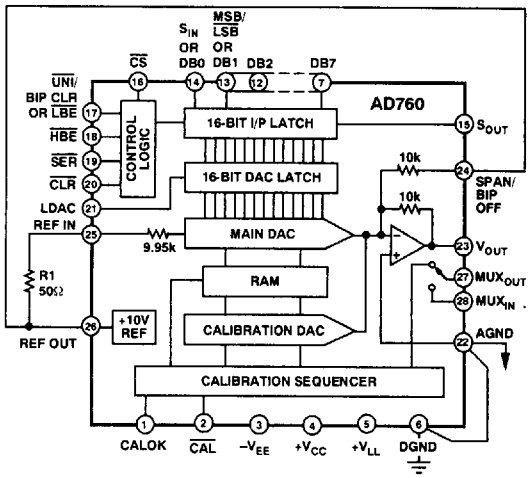
16-Bit Self-Calibrating Serial/Byte DACPORT

AD760

FEATURES

- ±0.00076% Integral and Differential Linearity
- ±0.00038% Unipolar Offset, Bipolar Zero
- 17-Bit Monotonic
- Complete 16-Bit D/A Function
  - On-Chip Output Amplifier
  - On-Chip Buried Zener Voltage Reference
- Microprocessor Compatible
  - Serial or Byte Input
  - Double Buffered Latches
  - Fast (40 ns) Write Pulse
  - Asynchronous Clear (to 0 V) Function
- Serial Output Pin Facilitates Daisy Chaining
- Pin Strappable Unipolar or Bipolar Output
- Low Glitch: 15 nV-sec
- Low THD+N: 0.009%
- Output Control on Power-Up & Power-Down

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD760 is a complete 16-bit self-calibrating monolithic DAC (DACPORT®) with onboard voltage reference, double buffered latches and output amplifier. It is manufactured on Analog Devices' BiMOS II process. This process allows the fabrication of low power CMOS logic functions on the same chip as high precision bipolar linear circuitry.

Self-calibration is initiated by simply bringing the $\overline{CAL}$ pin low. The CALOK pin indicates when calibration has been successfully completed. The output multiplexer (MUX_{OUT}) can be used to isolate the load from the movement of the DAC output during calibration. The INL and DNL errors are less than ±0.5 LSB or ±0.00076% after calibration. Unipolar offset or bipolar zero is less than ±0.25 LSB or ±0.00038%. This level of performance is unmatched by any other monolithic DAC.

Data can be loaded into the AD760 in serial mode or as two 8-bit bytes. This is made possible by two digital input pins which have dual functions (Pins 13 and 14). The serial mode input format is pin selectable, to be MSB or $\overline{LSB}$ first. In byte mode the user can similarly define whether the high byte or low byte is loaded first. The serial output (S_{OUT}) pin allows the user to daisy chain several AD760s by shifting the data through the input latch into the next DAC thus minimizing the number of control lines required in a multiple DAC application. The double buffered latch structure eliminates data skew errors and provides for simultaneous updating of DACs in a multi-DAC system.

The asynchronous $\overline{CLR}$ function can be configured to clear the output to unipolar or bipolar zero depending on the state of LBE (another dual-use pin) when $\overline{CLR}$ is strobed. The AD760 also powers up or down with the output in a predetermined state by means of a digital and analog power supply detection circuit which is built in to the output multiplexer. This is particularly useful for robotic and industrial control applications.

The AD760 is available in three grades. AN and AP versions are specified from −40°C to +85°C and are packaged in a 28-pin 600 mil plastic DIP and a 28-pin PLCC. The SD version is packaged in a 28-pin 600 mil cerdip package and is also available compliant to MIL-STD-883. Refer to the AD760/883B data sheet for specifications and test conditions.

DACPORT is a registered trademark of Analog Devices, Inc.

PRODUCT HIGHLIGHTS

1. Complete, true 16-bit, self-calibrating DAC, with a voltage reference, double-buffered latches and output amplifier on a single chip.
2. Pin programmable output can provide a unipolar output range of 0 V to +10 V or a bipolar output range of −10 V to +10 V. No external components required.
3. Asynchronous $\overline{CLR}$ function can send the output to unipolar or bipolar zero.
4. MUX_{OUT} is switched to a user defined input when powering up or down.
5. The AD760 is both dc and ac specified. DC specifications include ±0.5 LSB INL and DNL errors. AC specifications include 0.009% THD+N and 83 dB SNR.

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD760—SPECIFICATIONS (T_A = +25°C, V_{CC} = +15 V, V_{EE} = −15 V, V_{LL} = +5 V unless otherwise stated)

Model	AD760AN/AP Min	AD760AN/AP Typ	AD760AN/AP Max	AD760SQ Min	AD760SQ Typ	AD760SQ Max	Units
RESOLUTION[1]	16			16			Bits
TRANSFER FUNCTION CHARACTERISTICS[2]							
WITH CALIBRATION @ T_{CAL} ± 20°C[3]							
Integral Nonlinearity			±0.5			*	LSB
Differential Nonlinearity			±0.5			*	LSB
Monotonicity	17			*			Bits
Unipolar Offset			±0.25			*	LSB
Bipolar Zero Error			±0.25			*	LSB
WITHOUT CALIBRATION							
Integral Nonlinearity			±2			*	LSB
T_{MIN} to T_{MAX}			±4			*	LSB
Differential Nonlinearity			±2			*	LSB
T_{MIN} to T_{MAX}			±4			*	LSB
Monotonicity Over Temperature	14			*			Bits
Unipolar Offset			±5			*	mV
Unipolar Offset Drift (T_{MIN} to T_{MAX})			5			*	ppm/°C
Bipolar Zero Error			±15			*	mV
Bipolar Zero Error Drift (T_{MIN} to T_{MAX})			12			*	ppm/°C
Gain Error[4, 5]			±0.10			±0.15	% of FSR
Gain Drift[5] (T_{MIN} to T_{MAX})			15			25	ppm/°C
DAC Gain Error[6]			TBD			*	% of FSR
DAC Gain Drift[6] (T_{MIN} to T_{MAX})			TBD			*	ppm/°C
INPUT RESISTANCE							
REFIN	7	10	13	*	*	*	kΩ
SPAN/BIP OFF	7	10	13	*	*	*	kΩ
REFERENCE OUTPUT							
Voltage	9.98	10.00	10.02	*	*	*	V
Drift			15			25	ppm/°C
External Current[7]	2	4		*	*		mA
Capacitive Load			1000			*	pF
Short Circuit Current		25			*		mA
Long Term Stability		TBD			*		ppm/1000 Hrs.
OUTPUT CHARACTERISTICS[2]							
Output Voltage Range							
Unipolar Configuration	0		+10	*		*	V
Bipolar Configuration	−10		+10	*		*	V
Output Current	5			*			mA
Capacitive Load			1000			*	pF
Short Circuit Current		25			*		mA
MUX_{OUT} Resistance	TBD		TBD	*		*	kΩ
DIGITAL INPUTS (T_{MIN} to T_{MAX})							
V_{IH} (Logic "1")	2.0		5.5	*		*	V
V_{IL} (Logic "0")	0		0.8	*		*	V
I_{IH} (V_{IH} = 5.5 V)			±10			*	μA
I_{IL} (V_{IL} = 0 V)			±10			*	μA
DIGITAL OUTPUTS (T_{MIN} to T_{MAX})							
V_{OH} (I_{OH} = −0.6 mA)	2.4			*			V
V_{OL} (I_{OL} = 1.6 mA)			0.4			*	V
POWER SUPPLIES							
Voltage							
V_{CC}[8]	+13.5		+16.5	*		*	V
V_{EE}[8]	−16.5		−13.5	*		*	V
V_{LL}	+4.5		+5.5	*		*	V
Current (No Load)							
I_{CC}		+16	+21		*	*	mA
I_{EE}	−21	−16		*	*		mA
I_{LL}							
@ V_{IH}, V_{IL} = 5 V, 0 V		0.3	2		*	*	mA
@ V_{IH}, V_{IL} = 2.4 V, 0.4 V		3	7.5		*	*	mA
Power Supply Sensitivity with V_{OUT} = 10 V		1	3		*	*	ppm/%
Power Dissipation (Static, No Load)		495	725		*	*	mW
TEMPERATURE RANGE							
Specified Performance (A)	−40		+85				°C
Specified Performance (S)				−55		+125	°C

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

NOTES
[1]For 16-bit resolution, 1 LSB = 0.0015% of FSR. For 15-bit resolution, 1 LSB = 0.003% of FSR. For 14-bit resolution, 1 LSB = 0.006% of FSR. FSR stands for full-scale range and is 10 V in unipolar mode and 20 V in bipolar mode.
[2]Characteristics are guaranteed at V_{OUT} Pin (23).
[3]T_{CAL} is the calibration temperature.
[4]Gain Error is measured with a fixed 50 Ω resistor as shown in Figure 4a and Figure 5a.
[5]Gain Error and gain drift are measured with the internal reference. The internal reference is the main contributor to the gain drift. If lower drift is required the AD760 can be used with a precision external reference such as the AD587, AD586 or AD688.
[6]DAC Gain Error is measured without the on-chip voltage reference. It represents the performance that can be obtained with an external precision reference.
[7]External current is defined as the current available in addition to that supplied to REF IN and SPAN/BIPOLAR OFFSET on the AD760.
[8]Operation on ±12 V supplies is possible using an external reference such as the AD586 and reducing the output range. Refer to the Internal/External Reference section.
*Indicates that the specification is the same as the AD760AN.
Specifications subject to change without notice.

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AC PERFORMANCE CHARACTERISTICS

With the exception of Total Harmonic Distortion + Noise and Signal-to-Noise Ratio, these characteristics are included for design guidance only and are not subject to test. THD+N and SNR are 100% tested. ($T_{MIN} < T_A < T_{MAX}$, V_{CC} = +15 V, V_{EE} = −15 V, V_{LL} = +5 V, tested at V_{OUT} except where stated.)

Parameter	Limit	Units	Test Conditions/Comments
Output Settling Time	13	µs max	20 V Step, T_A = +25°C
(Time to +0.0008% FS, with	8	µs typ	20 V Step, T_A = +25°C
2 kΩ, 1000 pF Load)	10	µs typ	20 V Step
	6	µs typ	10 V Step, T_A = +25°C
	8	µs typ	10 V Step
	2.5	µs typ	1 LSB Step
MUX_{OUT} Settling Time			Settling Time is referenced to the rising edge of CALOK,
(Time to +0.0008% FS, with			when the multiplexer switches from MUX_{IN} to V_{OUT}.
100 pF Load)	TBD	µs max	20 V Step, T_A = +25°C
	TBD	µs typ	20 V Step, T_A = +25°C
	TBD	µs typ	20 V Step
	TBD	µs typ	10 V Step, T_A = +25°C
	TBD	µs typ	10 V Step
Total Harmonic Distortion + Noise			
A, S Grade	0.009	% max	0 dB, 1001 Hz. Sample Rate = 100 kHz. T_A = +25°C
A, S Grade	0.07	% max	−20 dB, 1001 Hz. Sample Rate = 100 kHz. T_A = +25°C
A, S Grade	7.0	% max	−60 dB, 1001 Hz. Sample Rate = 100 kHz. T_A = +25°C
Signal-to-Noise Ratio	83	dB min	T_A = +25°C
Digital-to-Analog Glitch Impulse	15	nV sec typ	DAC Alternatively Loaded with 8000_H and $7FFF_H$
MUX_{OUT} Glitch Impulse	TBD	nV sec typ	100 pF Load
Digital Feedthrough	2	nV sec typ	DAC Alternatively Loaded with 0000_H and $FFFF_H$. $\overline{CS}$ High
Output Noise Voltage Density (1 kHz–1 MHz)	60	nV/√Hz typ	Measured at V_{OUT}, 20 V Span, Excludes Reference
Reference Noise (1 kHz–1 MHz)	125	nV/√Hz typ	Measured at REF OUT

Specifications are subject to change without notice.

TIMING CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, V_{LL} = +5 V, V_{HI} = 2.4 V, V_{LO} = 0.4 V)

Parameter	Limit +25°C	Limit −40°C to +85°C	Limit −55°C to +125°C	Units
(Figure 1a)				
t_{CS}	50	50	50	ns min
t_{DS}	50	60	70	ns min
t_{DH}	10	10	10	ns min
t_{BES}	40	50	50	ns min
t_{BEH}	0	10	10	ns min
t_{LH}	140	200	200	ns min
t_{LW}	50	60	60	ns min
(Figure 1b)				
t_{CLK}	80	100	100	ns min
t_{LO}	30	50	50	ns min
t_{HI}	30	50	50	ns min
t_{DS}	50	60	70	ns min
t_{DH}	10	10	10	ns min
t_{LH}	140	200	200	ns min
t_{LW}	40	50	50	ns min
(Figure 1c)				
t_{CLR}	90	100	100	ns min
t_{SET}	80	100	100	ns min
t_{HOLD}	0	0	0	ns min
(Figure 1d)				
t_{PROP}	60	100	100	ns max
(Figure 1e)				
t_{CAL}	30	30	30	ns min
t_{BUSY}	200	200	200	ms max
t_{CD}	150	180	180	ns max
t_{CS}	140	180	180	ns max
t_{CV}	120	150	150	ns max

Specifications subject to change without notice.

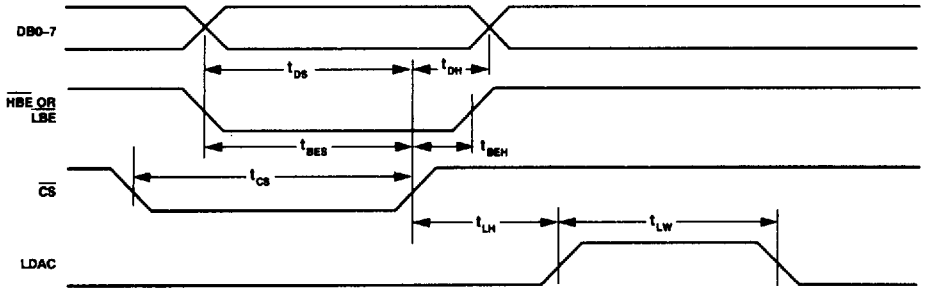


Figure 1a. AD760 Byte Load Timing

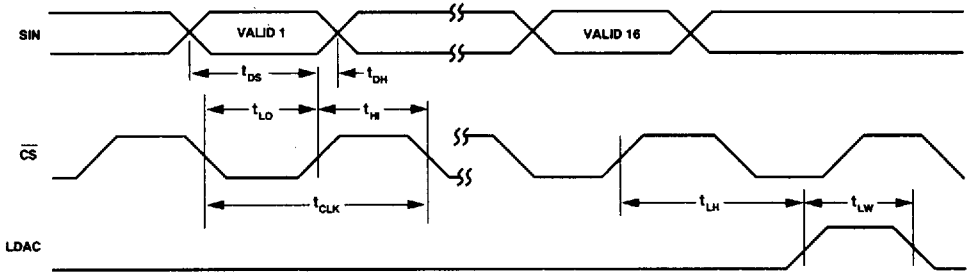


Figure 1b. AD760 Serial Load Timing

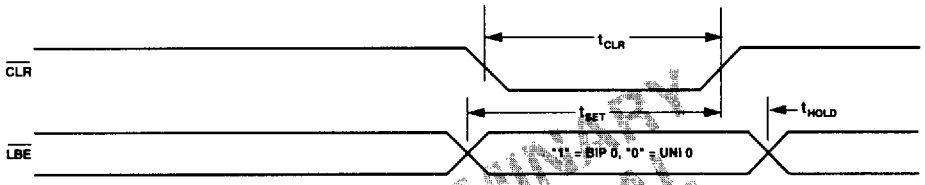


Figure 1c. Asynchronous Clear to Bipolar or Unipolar Zero

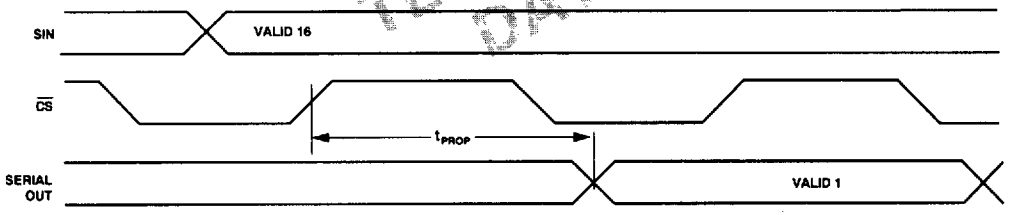


Figure 1d. Serial Out Timing

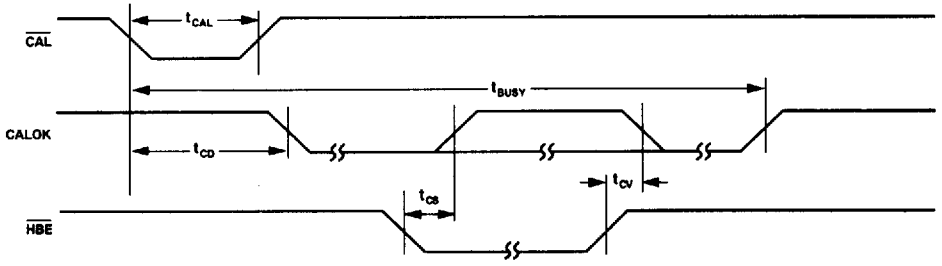


Figure 1e. Calibration Timing

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD760 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to AGND . . . . . −0.3 V to +17.0 V
V_{EE} to AGND . . . . . +0.3 V to −17.0 V
V_{LL} to DGND . . . . . −0.3 V to +7 V
AGND to DGND . . . . . ±1 V
Digital Inputs (Pins 2, 7–14, and 16–21)
to DGND . . . . . −1.0 V to +7.0 V
REF IN to AGND . . . . . ±10.5 V
Span/Bipolar Offset to AGND . . . . . ±10.5 V
REF OUT, V_{OUT}, MUX_{OUT}, MUX_{IN} . . . . Indefinite Short to AGND, DGND, V_{CC}, V_{EE}, and V_{LL}
Power Dissipation (Any Package)
To +60°C . . . . . 1000 mW
Derates above +60°C . . . . . 8.7 mW/°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

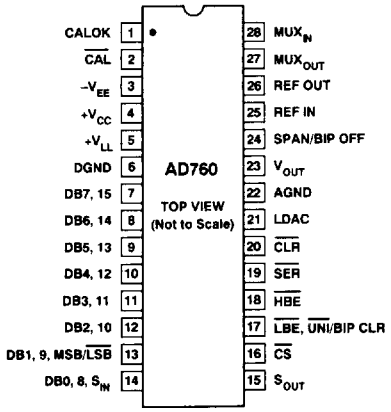
ORDERING GUIDE

Model	Temperature Range	Linearity Error Max T_{CAL} ± 20°C	Unipolar Offset T_{CAL} ± 20°C	Gain TC max ppm/°C	Package Description	Package Option*
AD760AN	−40°C to +85°C	±0.5 LSB	±0.25 LSB	15	Plastic DIP	N-28
AD760AP	−40°C to +85°C	±0.5 LSB	±0.25 LSB	15	PLCC	P-28A
AD760SQ	−55°C to +125°C	±0.5 LSB	±0.25 LSB	25	Cerdip	Q-28
AD760SQ/883B**	−55°C to +125°C	±0.5 LSB	**	**	**	**

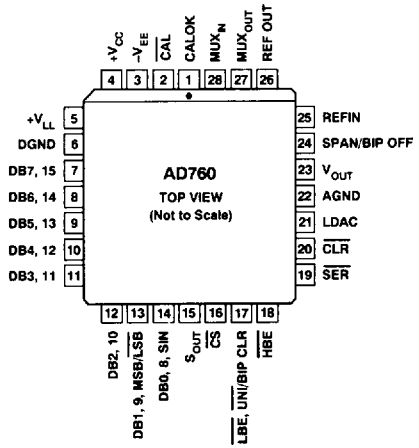
NOTES
*For outline information see Package Information section.
**Refer to the AD760/883B military data sheet.

PIN CONFIGURATION

DIP



PLCC



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DEFINITIONS OF SPECIFICATIONS

INTEGRAL NONLINEARITY: Analog Devices defines integral nonlinearity as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn from 0 to FS–1 LSB) for any bit combination. This is also referred to as relative accuracy.

DIFFERENTIAL NONLINEARITY: Differential nonlinearity is the measure of the change in the analog output, normalized to full scale, associated with a 1 LSB change in the digital input code. Monotonic behavior requires that the differential linearity error be greater than or equal to −1 LSB over the temperature range of interest.

MONOTONICITY: A DAC is monotonic if the output either increases or remains constant for increasing digital inputs with the result that the output will always be a single-valued function of the input.

GAIN ERROR: Gain error is a measure of the output error between an ideal DAC and the actual device output with all 1s loaded after offset error has been adjusted out.

OFFSET ERROR: Offset error is a combination of the offset errors of the voltage-mode DAC and the output amplifier and is measured with all 0s loaded in the DAC.

BIPOLAR ZERO ERROR: When the AD760 is connected for bipolar output and 10 . . . 000 is loaded in the DAC, the deviation of the analog output from the ideal midscale value of 0 V is called the bipolar zero error.

DRIFT: Drift is the change in a parameter (such as gain, offset and bipolar zero) over a specified temperature range. The drift temperature coefficient, specified in ppm/°C, is calculated by measuring the parameter at T_{MIN}, 25°C and T_{MAX} and dividing the change in the parameter by the corresponding temperature change.

TOTAL HARMONIC DISTORTION + NOISE: Total harmonic distortion + noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the values of the harmonics and noise to the value of the fundamental input frequency. It is usually expressed in percent (%).

THD+N is a measure of the magnitude and distribution of linearity error, differential linearity error, quantization error and noise. The distribution of these errors may be different, depending upon the amplitude of the output signal. Therefore, to be the most useful, THD+N should be specified for both large and small signal amplitudes.

SIGNAL-TO-NOISE RATIO: The signal-to-noise ratio is defined as the ratio of the amplitude of the output when a full-scale signal is present to the output with no signal present. This is measured in dB.

DIGITAL-TO-ANALOG GLITCH IMPULSE: This is the amount of charge injected from the digital inputs to the analog output when the inputs change state. This is measured at half scale when the DAC switches around the MSB and as many as possible switches change state, i.e., from 011 . . . 111 to 100 . . . 000.

DIGITAL FEEDTHROUGH: When the DAC is not selected (i.e., $\overline{CS}$ is held high), high frequency logic activity on the digital inputs is capacitively coupled through the device to show up as noise on the V_{OUT} pin. This noise is digital feedthrough.

THEORY OF OPERATION

The AD760 uses autocalibration circuitry to produce a true 16-bit DAC with less than 0.5 LSB Integral and Differential Linearity Error and 0.25 LSB Offset Error. The block diagram in Figure 2 shows the circuit components needed for calibration.

The MAIN DAC uses an array of bipolar current sources with MOS current steering switches to develop a current proportional to the applied digital word, ranging from 0 to 2 mA. A segmented architecture is used, where the most significant four data bits are thermometer decoded to drive 15 equal current sources. The lesser bits are scaled using a R-2R ladder, then applied together with the segmented sources at the summing node of the output amplifier. An extra LSB is added to the MAIN DAC, for use during calibration.

The self calibration architecture of the AD760 attempts to reduce the linearity errors of its transfer function. The algorithm measures and removes the carry errors (DNL errors) associated with the upper 64 codes, including the zero offset.

In normal operation the top six bits of a code entering the MAIN DAC simultaneously address the RAM, calling up a correction code which is then applied to the CALDAC. The output currents of both the MAIN DAC and CALDAC are combined in the summing amplifier to produce the corrected output voltage.

In the first step of calibration the output of the MAIN DAC is set to the code just below the code to be calibrated. The extra LSB in the MAIN DAC is turned on to find the extrapolated value for the next code. The comparator is then nulled using the TRANSFER STD DAC. The voltage at V_{OUT} has in effect been sampled at the code to be calibrated.

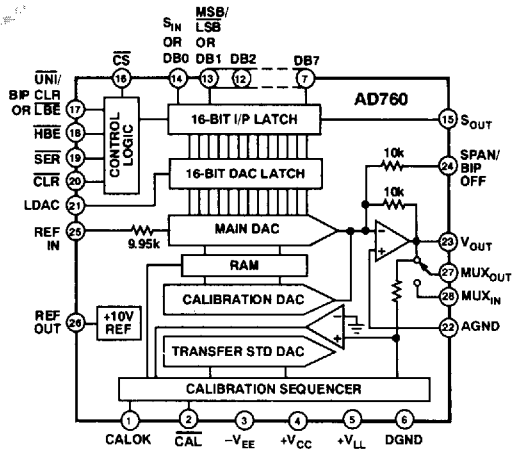


Figure 2. Functional Block Diagram

Next, the extra LSB is turned off and the MAIN DAC code is incremented by one LSB. The comparator is once again nulled, this time with the CALDAC, until the V_{OUT} is adjusted to equal the previously sampled output. The CALDAC code is stored in RAM and the process is repeated for the next code.

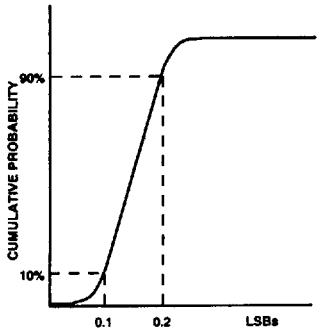


Figure 3. INL Statistics

Calibration repeatability is limited by thermal noise and the finite resolution of the two adjusting DACs. Over many recalibrations the AD760 will produce less than 0.2 LSB of peak INL for 90% of calibrations (0.5 LSB at a 30 ppm reject rate). A cumulative probability plot of the peak INL is shown in Figure 3.

ANALOG CIRCUIT CONNECTIONS

Internal scaling resistors provided in the AD760 may be connected to produce a unipolar output range of 0 V to +10 V or a bipolar output range of −10 V to +10 V. Gain and offset drift are minimized in the AD760 because of the thermal tracking of the scaling resistors with other device components.

UNIPOLAR CONFIGURATION

The configuration shown in Figure 4a will provide a unipolar 0 V to +10 V output range. In this mode a 50 Ω resistor is tied between REF OUT (Pin 26) and REF IN (Pin 25). It is possible to use the AD760 without any external components by tying Pin 26 directly to Pin 25. Eliminating this resistor will increase the gain error by 0.50% of FSR.

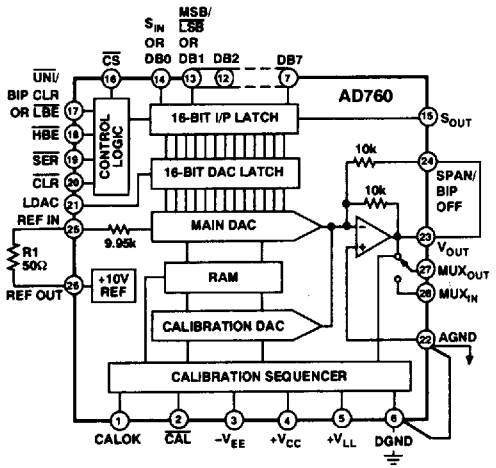


Figure 4a. 0 V to +10 V Unipolar Voltage Output

If it is desired to adjust the gain error to zero, this can be accomplished using the circuit shown in Figure 4b. The adjustment procedure is as follows:

STEP1 . . . ZERO ADJUST

Initiate calibration sequence. CALOK (Pin 1) must remain high throughout Gain Adjust.

STEP 2 . . . GAIN ADJUST

Turn all bits ON and adjust gain trimmer, R1, until the output is 9.999847 volts. (Full scale is adjusted to 1 LSB less than the nominal full scale of 10.000000 volts).

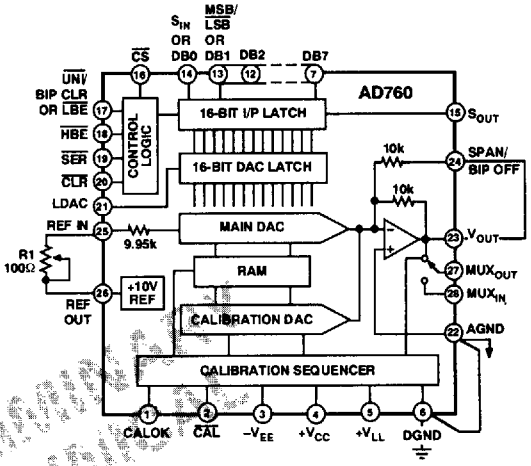


Figure 4b. 0 V to +10 V Unipolar Voltage Output with Gain Adjust

BIPOLAR CONFIGURATION

The circuit shown in Figure 5a will provide a bipolar output voltage from −10.000000 V to +9.999694 V with positive full scale occurring with all bits ON. As in the unipolar mode, resistor R1 may be eliminated altogether to provide AD760 bipolar operation without any external components. Eliminating this resistor will increase the gain error by 0.50% of FSR in the bipolar mode.

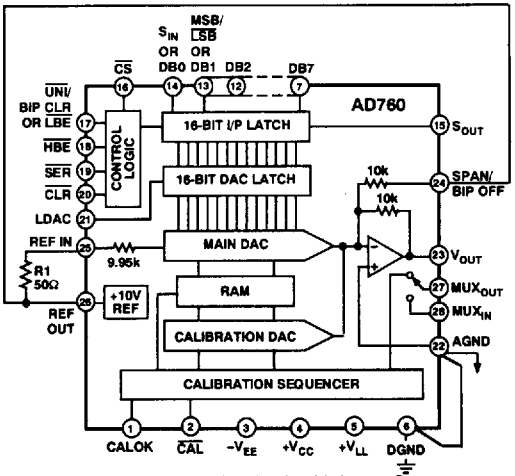


Figure 5a. ±10 V Bipolar Voltage Output

Gain Error can be adjusted to zero using the circuit shown in Figure 5b.

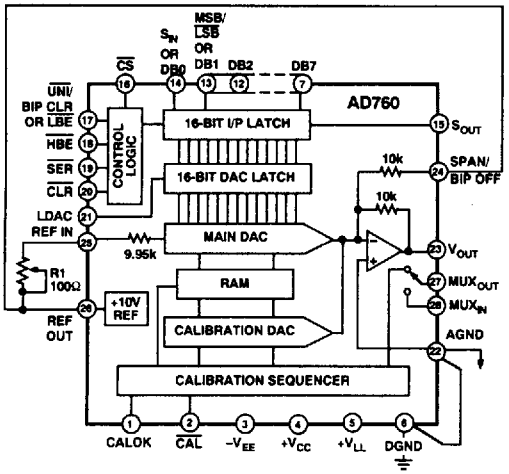


Figure 5b. ±10 V Bipolar Voltage Output Gain Adjustment

It should be noted that using external resistors will introduce a small temperature drift component beyond that inherent in the AD760. The internal resistors are trimmed to ratio-match and temperature-track other resistors on chip, even though their absolute tolerances are ±20% and absolute temperature coefficients are approximately −50 ppm/°C. In the case that external resistors are used, the temperature coefficient mismatch between internal and external resistors, multiplied by the sensitivity of the circuit to variations in the external resistor value, will be the resultant additional temperature drift.

INTERNAL/EXTERNAL REFERENCE USE

The AD760 has an internal low noise buried Zener diode reference which is trimmed for absolute accuracy and temperature coefficient. This reference is buffered and optimized for use in a high speed DAC and will give long-term stability equal or superior to the best discrete Zener diode references. The performance of the AD760 is specified with the internal reference driving the DAC and with the DAC alone (for use with a precision external reference).

The internal reference has sufficient buffering to drive external circuitry in addition to the reference currents required for the DAC (typically 1 mA to REF IN and 1 mA to BIPOLAR OFFSET). A minimum of 2 mA is available for driving external loads. The AD760 reference output should be buffered with an external op amp if it is required to supply more than 4 mA total current. The reference is tested and guaranteed to ±0.2% max error.

It is also possible to use external references other than 10 volts with slightly degraded linearity specifications. The recommended range of reference voltages is +5 V to +10.24 V, which allows 5 V, 8.192 V and 10.24 V ranges to be used. For example, by using the AD586 5 V reference, outputs of 0 V to +5 V unipolar or ±5 V bipolar can be realized. Using the AD586 voltage reference makes it possible to operate the AD760 with ±12 V supplies with 10% tolerances.

Figure 6 shows the AD760 using the AD586 precision 5 V reference in the bipolar configuration. The highest grade AD586MN is specified with a drift of 2 ppm/°C which is a 7.5× improvement over the AD760's internal reference. This circuit includes an optional potentiometer that can be used to adjust the gain error in a manner similar to that described in the BIPOLAR CONFIGURATION section. Use −5.000000 V and +4.999847 as the output values.

The AD760 can also be used with the AD587 10 V reference, using the same configuration shown in Figure 6 to produce a ±10 V output. The highest grade AD587LR, N is specified at 5 ppm/°C, which is a 3× improvement over the AD760's internal reference.

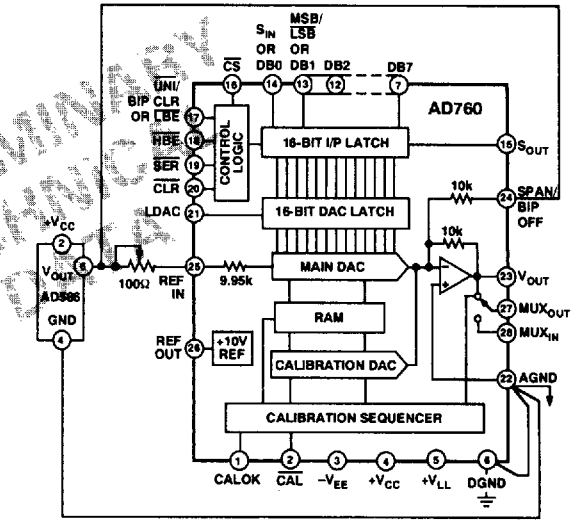
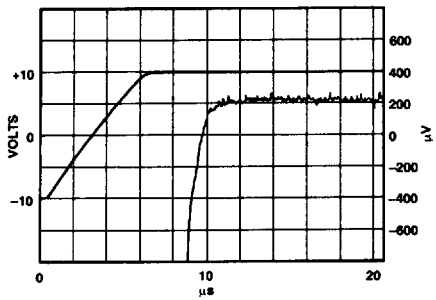


Figure 6. Using the AD760 with the AD586 5 V Reference

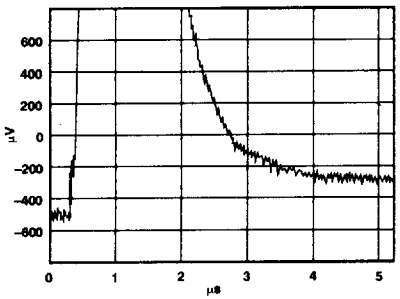
OUTPUT SETTLING AND GLITCH

The AD760's output buffer amplifier typically settles to within 0.0008% FS (1/2 LSB) of its final value in 8 μs for a full-scale step. Figures 7a and 7b show settling for a full-scale and an LSB step, respectively, with a 2 kΩ, 1000 pF load applied. The guaranteed maximum settling time at +25°C for a full-scale step is 13 μs with this load. The typical settling time for a 1 LSB step is 2.5 μs.

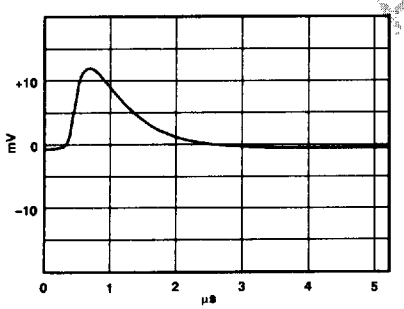
The digital-to-analog glitch impulse is specified as 15 nV-s typical. Figure 7c shows the typical glitch impulse characteristic at the code 011 . . . 111 to 100 . . . 000 transition when loading the second rank register from the first rank register.



a. −10 V to +10 V Full-Scale Step Settling



b. LSB Step Settling



c. D-to-A Glitch Impulse

Figure 7. Output Characteristics

DIGITAL CIRCUIT DETAILS

The AD760 has several "dual-use" pins which allow flexible operation while maintaining the lowest possible pin count and consequently the smallest package size. The following information is useful when applying the AD760.

The AD760 uses an internal **Output Multiplexer** to disconnect the DAC output from MUX_{OUT} (Pin 27) when the device is uncalibrated or when a calibration sequence is in progress. At those times MUX_{OUT} is switched to MUX_{IN} (Pin 28) so the user can force a predetermined output voltage.

A **Power On-Reset** feature senses whenever any power supply is low enough to jeopardize the integrity of the calibration data in the RAM. At power-up or in the event of a power supply transient, CALOK (Pin 1) is low and the MUX_{OUT} pin is switched to MUX_{IN}.

Self-Calibration is initiated by bringing the $\overline{CAL}$ pin low. The CALOK pin will go low and the MUX_{OUT} pin is connected to MUX_{IN}. After successful completion of calibration CALOK will go high and MUX_{OUT} is switched to V_{OUT}. The status of the calibration may be determined by taking the $\overline{HBE}$ pin low. CALOK either switches high if the calibration is in progress or CALOK remains low if a power supply voltage transient caused the AD760 to be set to the uncalibrated state.

Serial Mode Operation is enabled by bringing the $\overline{SER}$ (Pin 19) low. All unused data bits, DB2–DB7 must be tied low. This changes the function of DB0 (Pin 14) to that of the serial input pin, SIN. It also changes the function of DB1 (Pin 13) to a control input, MSB/$\overline{LSB}$ that tells the AD760 which bit is going to be loaded first.

In serial mode the byte controls $\overline{HBE}$ (Pin 18) and $\overline{LBE}$ (Pin 17) are disabled, and Pin 17's function changes to control how the asynchronous clear function works: a low when $\overline{CLR}$ is strobed sends the DAC to unipolar zero, a high sends it to bipolar zero.

Data is clocked into the input shift register on the rising edge of $\overline{CS}$ as shown in Figure 1b. The data is then resident in the first rank latch and can be loaded into the DAC by taking the LDAC pin high. This will cause the DAC to change to the appropriate output value. The second rank latch controlled by LDAC is a Transparent latch. Changes in the first rank latch will be reflected in the DAC output immediately, as long as LDAC remains high.

It should be noted that the clear function clears the DAC latch but does not clear the first rank latch. Therefore, the data that was previously resident in the first rank latch can be reloaded by simply bringing LDAC high again. Alternatively, new data can be loaded into the first rank latch if desired.

The serial out pin (S_{OUT}) can be used to daisy chain several DACs together in multi-DAC applications to minimize the number of data lines required. The first rank latch simply acts like a 16-bit shift register, and repeated strobing of $\overline{CS}$ will shift the data out through S_{OUT} and into the next DAC. Each DAC in the chain will require its own LDAC signal unless all of the DACs are to be updated simultaneously.

Byte Mode Operation is enabled by setting $\overline{SER}$ high, which configures DB0–DB7 as data inputs. In this mode $\overline{HBE}$ and $\overline{LBE}$ are used to identify the data as either the high byte or the low byte of the 16-bit word. The user can load the data in either order into the first rank latch using the rising edge of the $\overline{CS}$ signal as shown in Figure 1a. The status of Pin 17, when $\overline{CLR}$ is strobed determines whether the AD760 clears to unipolar or bipolar zero. (But it can not be hardwired to the desired state, as in the serial mode.)

NOTE: $\overline{CS}$ and $\overline{CAL}$ are edge triggered. $\overline{HBE}$, $\overline{LBE}$, $\overline{CLR}$, $\overline{SER}$, and LDAC are level triggered.

AD760 TO MC68HC11 (SPI BUS) INTERFACE

The AD760 interface to the Motorola SPI (serial peripheral interface) is shown in Figure 8. The MOSI, SCK, and $\overline{SS}$ pins of the HC11 are respectively connected to the BIT0, $\overline{CS}$ and LDAC pins of the AD760. The $\overline{SER}$ pin of the AD760 is tied low causing the first rank latch to be transparent. The majority of the interfacing issues are taken care of in the software initialization. A typical routine such as the one shown below begins

by initializing the state of the various SPI data and control registers.

The most significant data byte (MSBY) is then retrieved from memory and processed by the SENDAT subroutine. The $\overline{SS}$ pin is driven low by indexing into the PORTD data register and clear Bit 5. This causes the 2nd rank latch of the AD760 to become transparent. The MSBY is then set to the SPI data register where it is automatically transferred to the AD760.

The HC11 generates the requisite 8 clock pulses with data valid on the rising edges. After the most significant byte is transmitted, the least significant byte (LSBY) is loaded from memory and transmitted in a similar fashion. To complete the transfer, the LDAC pin is driven high latching the complete 16-bit word into the AD760.

```
INIT    LDAA #$2F     ;SS = 1; SCK = 0; MOSI = 1
        STAA PORTD    ;SEND TO SPI OUTPUTS
        LDAA #$38     ;SS, SCK,MOSI = OUTPUTS
        STAA DDRD     ;SEND DATA DIRECTION INFO
        LDAA #$50     ;DABL INTRPTS,SPI IS MASTER & ON
        STAA SPCR     ;CPOL=0, CPHA = 0,1MHZ BAUD RATE
NEXTPT  LDAA MSBY     ;LOAD ACCUM W/UPPER 8 BITS
        BSR  SENDAT   ;JUMP TO DAC OUTPUT ROUTINE
        JMP  NEXTPT   ;INFINITE LOOP
SENDAT  LDY  #$1000   ;POINT AT ON-CHIP REGISTERS
        BCLR $08,Y,$20 ;DRIVE SS (LDAC) LOW
        STAA SPDR     ;SEND MS-BYTE TO SPI DATA REG
WAIT1   LDAA SPSR     ;CHECK STATUS OF SPIE
        BPL  WAIT1    ;POLL FOR END OF X-MISSION
        LDAA LSBY     ;GET LOW 8 BITS FROM MEMORY
        STAA SPDR     ;SEND LS-BYTE TO SPI DATA REG
WAIT2   LDAA SPSR     ;CHECK STATUS OF SPIE
        BPL  WAIT2    ;POLL FOR END OF X-MISSION
        BSET $08,Y,$20 ;DRIV SS HIGH TO LATCH DATA
        RTS
```

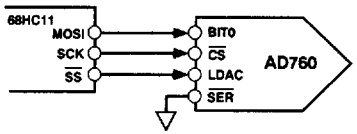


Figure 8. AD760 to 68HC11 (SPI) Interface

AD760 TO MICROWIRE INTERFACE

The flexible serial interface of the AD760 is also compatible with the National Semiconductor MICROWIRE* interface. The MICROWIRE interface is used on microcontrollers such as the COP400 and COP800 series of processors. A generic interface to the MICROWIRE interface is shown in Figure 9. The G1, SK, and SO pins of the MICROWIRE interface are respectively connected to the LDAC, $\overline{CS}$ and BIT0 pins of the AD760.

*MICROWIRE is a registered trademark of National Semiconductor.

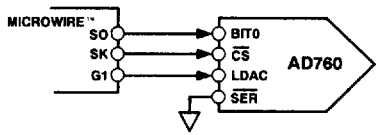


Figure 9. AD760 to MICROWIRE Interface

NOISE

In high resolution systems, noise is often the limiting factor. A 16-bit DAC with a 10 volt span has an LSB size of 153 μV (−96 dB). Therefore, the noise floor must remain below this level in the frequency range of interest. The AD760's noise spectral density is shown in Figures 10 and 11. Figure 12 shows the DAC output noise voltage spectral density for a 20 V span excluding the reference. This figure shows the 1/f corner frequency at 100 Hz and the wideband noise to be below 120 nV/$\sqrt{Hz}$. Figure 13 shows the reference noise voltage spectral density. This figure shows the reference wideband noise to be below 125 nV/$\sqrt{Hz}$.

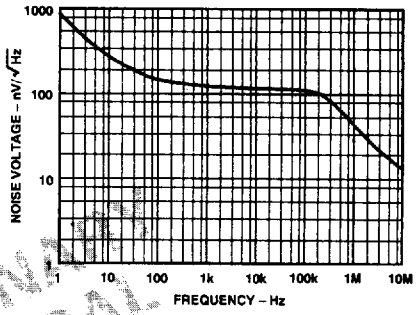


Figure 10. DAC Output Noise Voltage Spectral Density

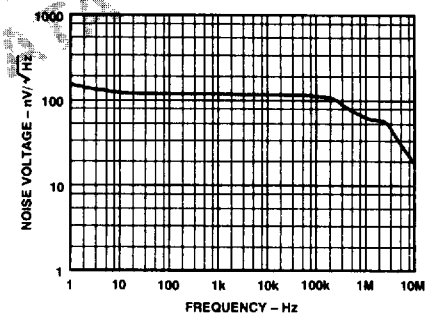


Figure 11. Reference Noise Voltage Spectral Density

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is the first issue. A 306 μA current through a 0.5 Ω trace will develop a voltage drop of 153 μV, which is 1 LSB at the 16-bit level for a 10 V full-scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals. Finally, power supplies need to be decoupled in order to filter out ac noise.

Analog and digital signals should not share a common path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes should also be used, with a single interconnection point to minimize ground loops. Analog signals should be routed as far as possible from digital signals and should cross them at right angles.

One feature that the AD760 incorporates to help the user layout is that the analog pins (V_{CC}, V_{EE}, REF OUT, REF IN, SPAN/BIP OFFSET, V_{OUT}, MUX_{OUT}, MUX_{IN} and AGND) are adjacent to help isolate analog signals from digital signals.

SUPPLY DECOUPLING

The AD760 power supplies should be well filtered, well regulated, and free from high frequency noise. Switching power supplies are not recommended due to their tendency to generate spikes which can induce noise in the analog system.

Decoupling capacitors should be used in very close layout proximity between all power supply pins and ground. A 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor provides adequate decoupling. V_{CC} and V_{EE} should be bypassed to analog ground, while V_{LL} should be decoupled to digital ground.

An effort should be made to minimize the trace length between the capacitor leads and the respective converter power supply and common pins. The circuit layout should attempt to locate the AD760, associated analog circuitry and interconnections as far as possible from logic circuitry. A solid analog ground plane around the AD760 will isolate large switching ground currents. For these reasons, the use of wire wrap circuit construction is not recommended; careful printed circuit construction is preferred.

GROUNDING

The AD760 has two pins, designated analog ground (AGND) and digital ground (DGND.) The analog ground pin is the "high quality" ground reference point for the device. Any external loads on the output of the AD760 should be returned to analog ground. If an external reference is used, this should also be returned to the analog ground.

If a single AD760 is used with separate analog and digital ground planes, connect the analog ground plane to AGND and the digital ground plane to DGND keeping lead lengths as short as possible. Then connect AGND and DGND together at the AD760. If multiple AD760s are used or the AD760 shares analog supplies with other components, connect the analog and digital returns together once at the power supplies rather than at each chip. This single interconnection of grounds prevents large ground loops and consequently prevents digital currents from flowing through the analog ground.