Octal bus transceiver/register (3-State) 74LVC646A

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Flow-through pin-out architecture
- In accordance with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- 5 Volt tolerant inputs/outputs, for interfacing with 5 Volt logic

DESCRIPTION

The 74LVC646A is a high performance, low-power, low-voltage Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5.0V devices. In 3-State operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC646A consist of non-inverting bus transceiver circuits with 3-State outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the 'A' or 'B' bus will be clocked in the internal registers, as the appropriate clock (CPAB or CPBA) goes to a HIGH logic level. Output enable ($\overline{OE}$) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the 'A' or 'B' register, or in both. The select source inputs (SAB and SBA) can multiplex stored and real-time (transparent mode) data.

The direction (DIR) input determines which bus will receive data when $\overline{OE}$ is active (LOW). In the isolation mode (OE = HIGH), 'A' data may be stored in the 'B' register and/or 'B' data may be stored in the 'A' register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, 'A' or 'B' may be driven at a time.

The '646A' is functionally identical to the '648A' but has non-inverting data paths.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Yn	C_L = 50pF V_{CC} = 3.3V	3.9	ns
f_{max}	Maximum clock frequency		250	MHz
C_I	Input capacitance		5.0	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1, 2	26	pF

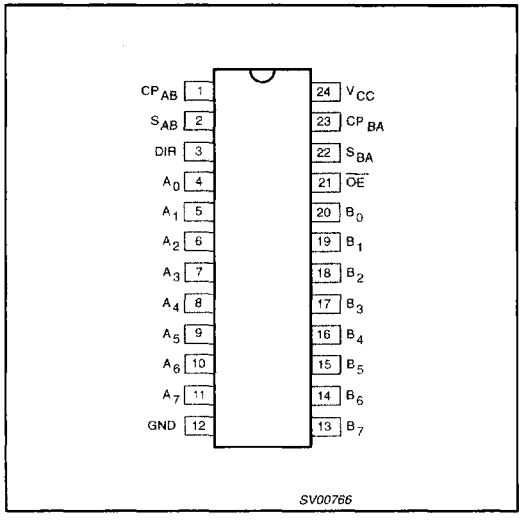
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
24-Pin Plastic SO	–40°C to +85°C	74LVC646A D	74LVC646A D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC646A DB	74LVC646A DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC646A PW	7LVC646APW DH	SOT355-1

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	CP_{AB}	'A' to 'B' clock input (LOW-to-HIGH, edge-triggered)
2	S_{AB}	Select 'A' to 'B' source input
3	DIR	*Direction control input*
4, 5, 6, 7, 8, 9, 10, 11	A_0 to A_7	'A' data inputs/outputs
12	GND	Ground (0V)
20, 19, 18, 17, 16, 15, 14, 13	B_0 to B_7	'B' data inputs/outputs
21	$\overline{OE}$	Output enable input (active LOW)
22	S_{BA}	Select 'B' to 'A' source input
23	CP_{BA}	'B' to 'A' clock input (LOW-to-HIGH, edge-triggered)
24	V_{CC}	Positive supply voltage

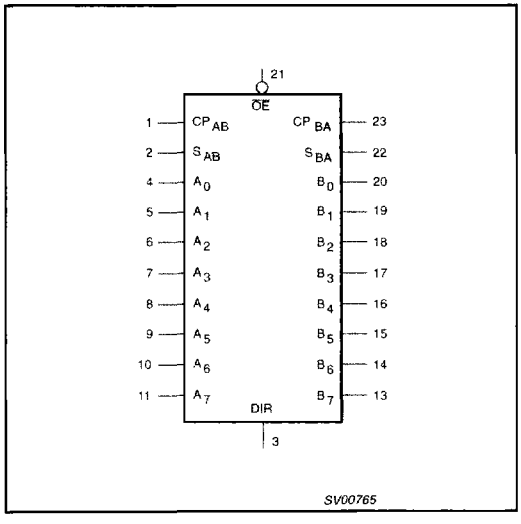
FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A_0 to A_7	B_0 to B_7	
X X	X X	↑ X	X ↑	X X	X X	input un *	un * input	store A, B unspecified * store B, A unspecified *
H H	X X	↑ H or L	↑ H or L	X X	X X	input	input	store A and B data, isolation hold storage
L L	L L	X X	X H or L	X X	L H	output	input	real-time B data to A bus stored B data to A bus
L L	H H	X H or L	X X	L H	X X	input	output	real-time A data to B bus stored A data to B bus

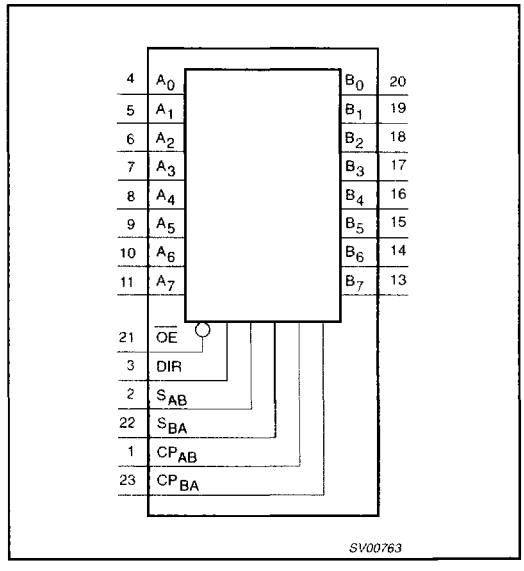
* The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH level transition

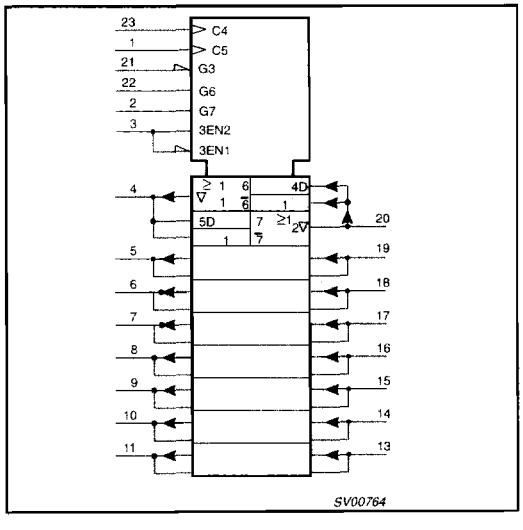
LOGIC SYMBOL



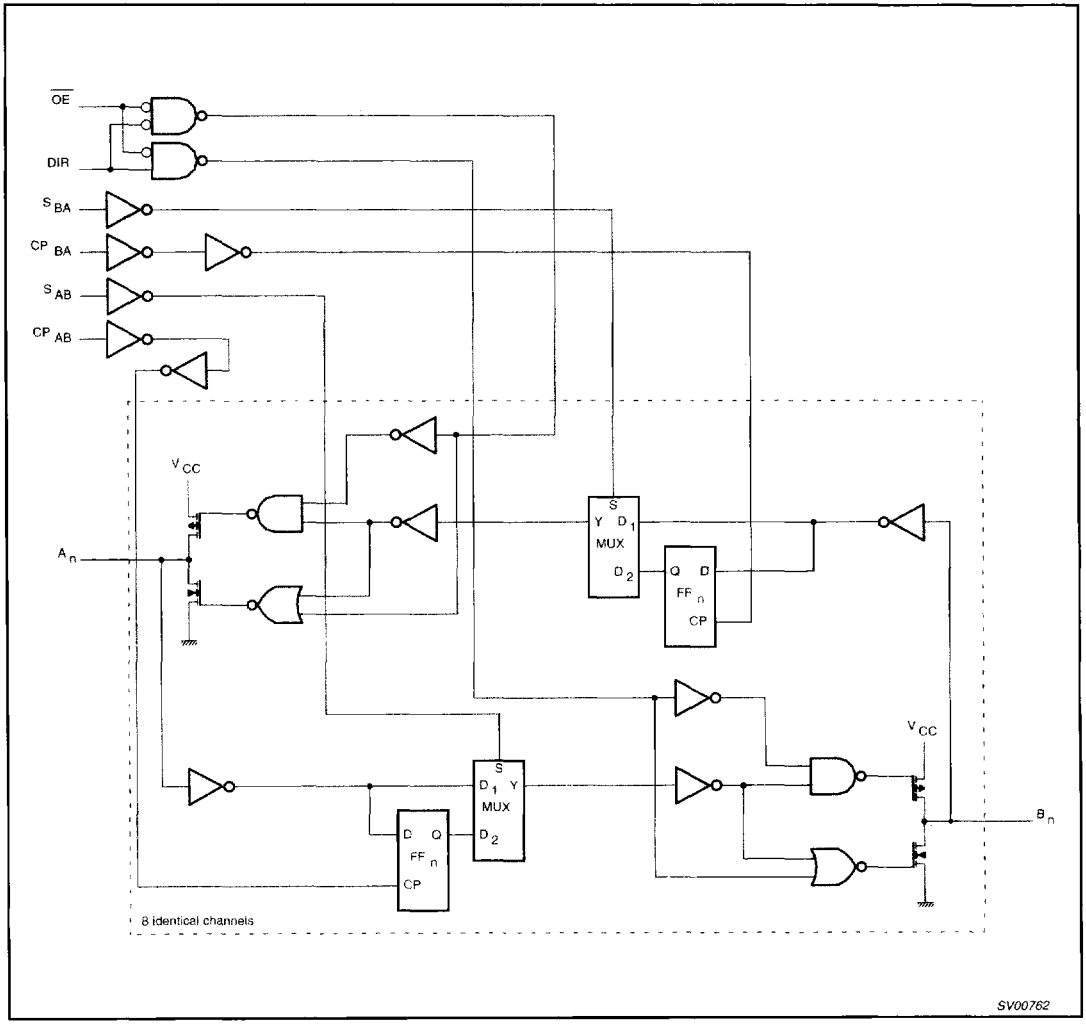
FUNCTIONAL DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating free-air temperature range		−40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage	Note 2	−0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage; output HIGH or LOW	Note 2	−0.5 to V_{CC} +0.5	V
	DC output voltage; output 3-State	Note 2	−0.5 to 6.5	
I_O	DC output diode current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = −12mA	V_{CC} − 0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = −100µA	V_{CC} − 0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = −18mA	V_{CC} − 0.6			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = −24mA	V_{CC} − 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND | Not for I/O pins		±0.1	±5	µA
I_{IHZ}/I_{ILZ}	Input current for common I/O pins	V_{CC} = 3.6V; V_I = V_{CC} or GND		±0.1	±15	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; V_I = V_{IH} or V_{IL}; V_O = 5.5V or GND		0.1	±10	µA
I_{OFF}	Power off leakage current	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} −0.6V; I_O = 0		5	500	µA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL}/t_{PLH}	Propagation delay An, Bn to Bn, An	Figures 1, 6	1.5	3.9	6.8	1.5	7.8	15	ns
t_{PHL}/t_{PLH}	Propagation delay CP_{AB}, CP_{BA} to B_n, A_n	Figures 2, 6	1.5	4.6	7.6	1.5	8.6	19	ns
t_{PHL}/t_{PLH}	Propagation delay S_{AB}, S_{BA} to B_n, A_n	Figures 3, 6	1.5	4.9	8.5	1.5	9.5	19	ns
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}$n to An, Bn	Figures 4, 6	1.5	4.5	7.8	1.5	8.8	20	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}$n to An, Bn	Figures 4, 6	1.5	3.9	6.1	1.5	7.1	10	ns
t_{PZH}/t_{PZL}	3-State output enable time DIR to An, Bn	Figures 5, 6	1.5	4.6	7.9	1.5	8.9	20	ns
t_{PHZ}/t_{PLZ}	3-State output disable time DIR to An, Bn	Figures 5, 6	1.5	3.5	6.0	1.5	7.0	12	ns
t_W	Clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	Figure 1, 3	3.3	1.9	–	3.3	–	–	ns
t_{su}	Set-up time An, Bn to CP_{AB}, CP_{BA}	Figure 2	1.6	0.35	–	1.6	–	–	ns
t_h	Hold time An, Bn to CP_{AB}, CP_{BA}	Figure 2	1.0	–0.3	–	1.0	–	–	ns
f_{max}	Maximum clock pulse frequency	Figure 2	150	250	–	125	–	–	ns

NOTE:

1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V
V_M = 0.5V * V_{CC} at V_{CC} < 2.7V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V
$V_X = V_{OL}$ + 0.1V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ − 0.3V at $V_{CC} \geq$ 2.7V
$V_Y = V_{OH}$ − 0.1V_{CC} at V_{CC} < 2.7V

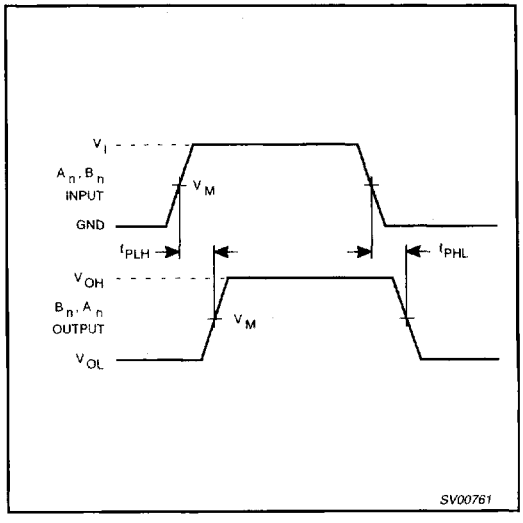


Figure 1. Input An, Bn to output Bn, An propagation delays.

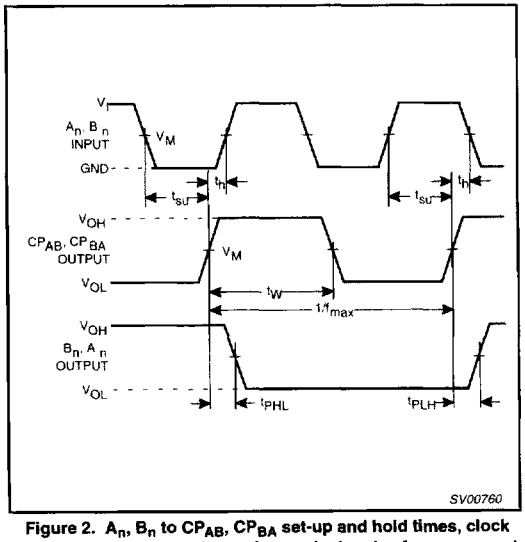


Figure 2. A_n, B_n to CP_{AB}, CP_{BA} set-up and hold times, clock CP_{AB}, CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB}, CP_{BA} to output B_n, A_n propagation delays.

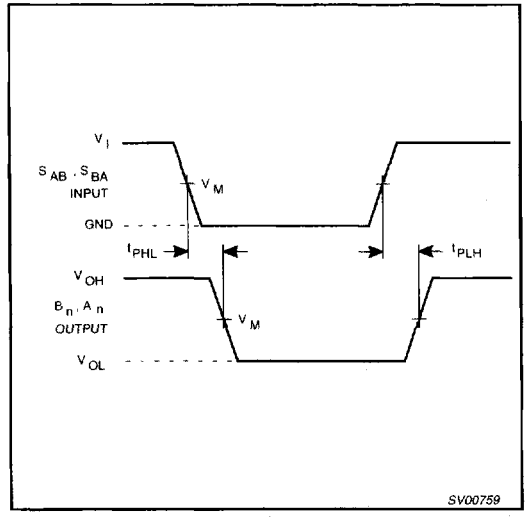


Figure 3. Input S_{AB}, S_{BA} to output B_n, A_n propagation delay times.

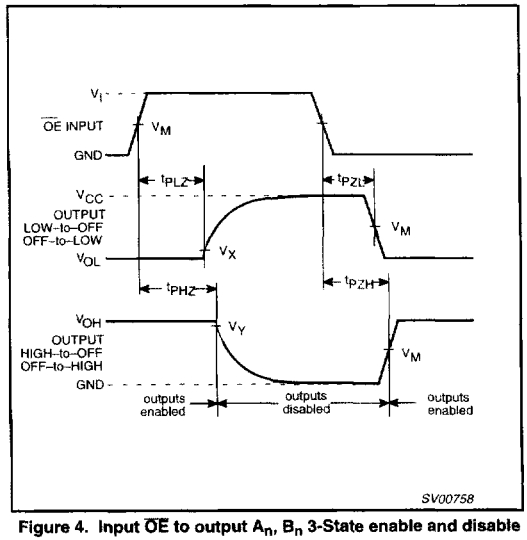


Figure 4. Input $\overline{OE}$ to output A_n, B_n 3-State enable and disable times.

AC WAVEFORMS (*Continued*)

V_M = 1.5V at $V_{CC} \geq$ 2.7V
V_M = 0.5V * V_{CC} at V_{CC} < 2.7V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V
$V_X = V_{OL}$ + 0.1V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ – 0.3V at $V_{CC} \geq$ 2.7V
$V_Y = V_{OH}$ – 0.1V_{CC} at V_{CC} < 2.7V

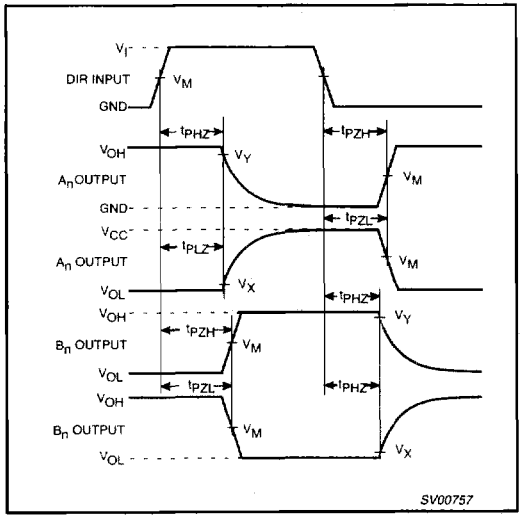
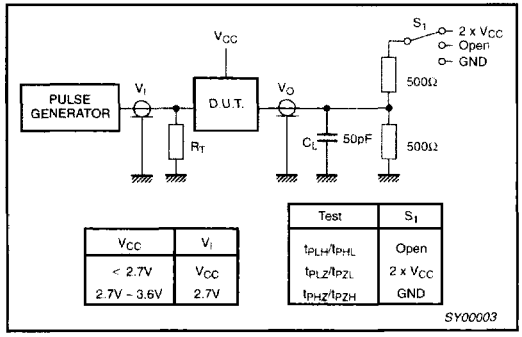


Figure 5. Input DIR to output A_n, B_n 3-State enable and disable times.

TEST CIRCUIT



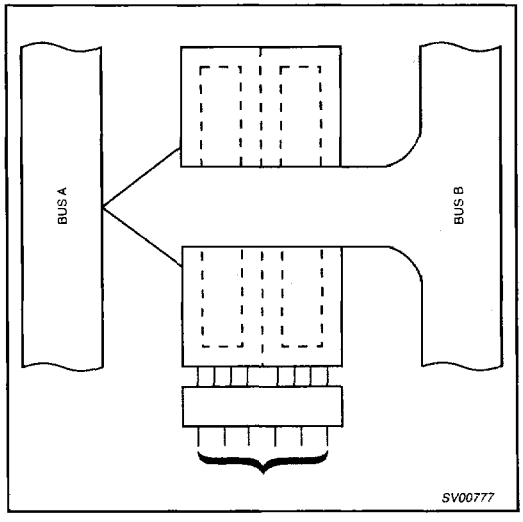
V_{CC}	V_I
< 2.7V	V_{CC}
2.7V – 3.6V	2.7V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

Figure 6. Load circuitry for switching times.

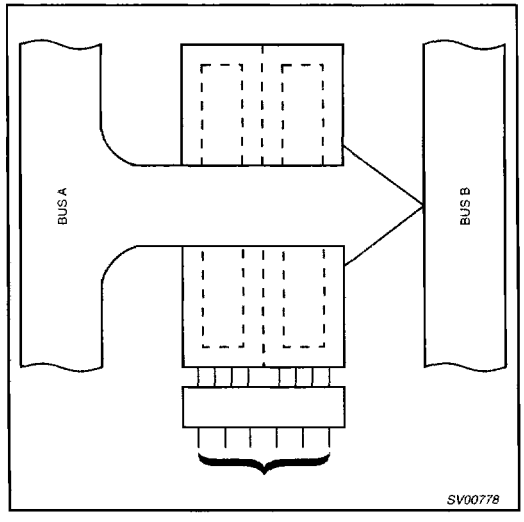
APPLICATION INFORMATION

Real-time transfer; bus B to bus A



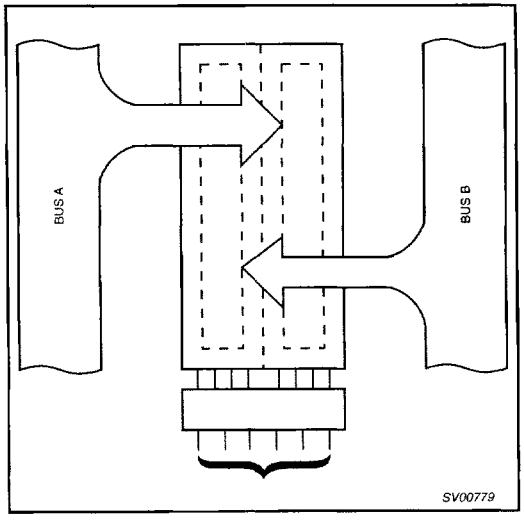
(1)	(14)	(28)	(16)	(27)	(15)
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	L	X	X	X	L

Real-time transfer; bus A to bus B



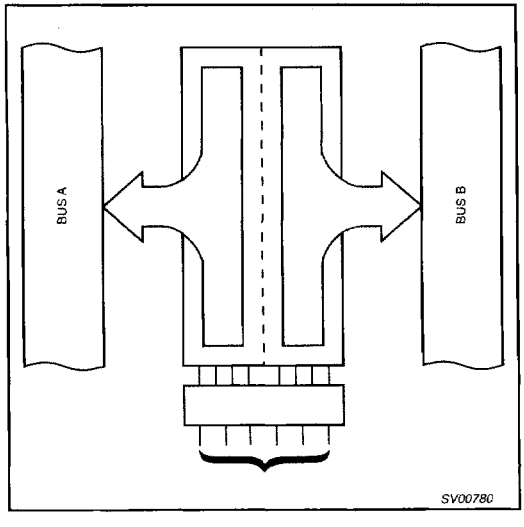
(1)	(14)	(28)	(16)	(27)	(15)
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	H	X	X	L	X

Storage from A, B or A and B



(1)	(14)	(28)	(16)	(27)	(15)
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
X	X	↑	X	X	X
X	X	X	↑	X	L
H	X	↑	↑	X	X

Transfer storage data to A or B



(1)	(14)	(28)	(16)	(27)	(15)
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	L	X	H or L	X	H
L	H	H or L	X	H	X