1M × 16 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM416C1200L/LL-7	70ns	20ns	130ns
KM416C1200L/LL-8	80ns	20ns	150ns
KM416C1200L/LL-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **2 $\overline{CAS}$ Byte/Word Read/Write operation**
- **Self Refresh Capability (LL-version)**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Triple +5V±10% power supply**
- **1024 cycles 128ms refresh**
- **Power Dissipation**
  - **Standby : 1.65mW**
  - **Active(70/80/100) : 880/770/660mW**
- **JEDEC Standard pinout**
- **Available in Plastic SOJ and TSOP II Packages**

GENERAL DESCRIPTION

The Samsung KM416C1200L/LL is a CMOS high speed 1,048,576 bit × 16 Dynamic Random Access Memory. It's design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM416C1200L/LL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM416C1200L/LL is fabricated using Samsung's advanced CMOS process.

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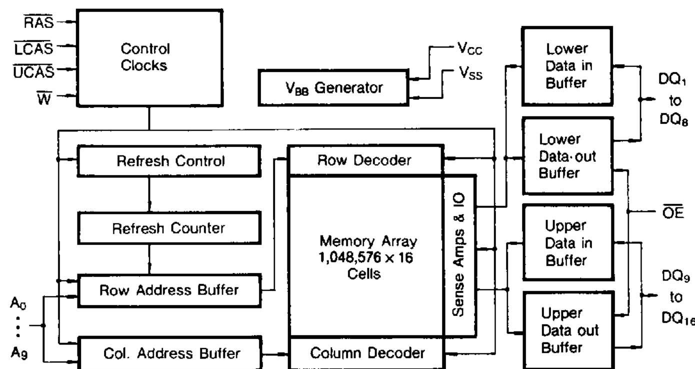
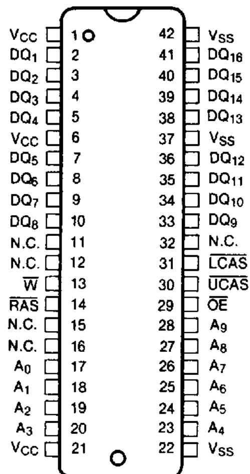
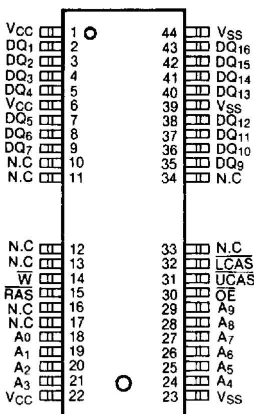
FUNCTIONAL BLOCK DIAGRAM



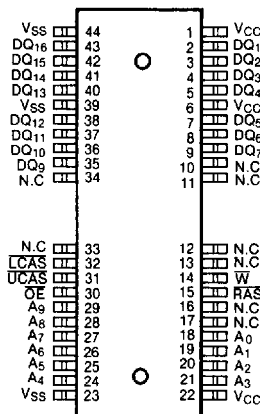
• KM416C1200LJ/LLJ



• KM416C1200LT/LLT



• KM416C1200LTR/LLTR



Pin Names	Pin Function
A_0-A_9	Address Inputs
DQ_{1-16}	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
V_{CC}	Power (+5V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN},V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{STG}	-55 to + 150	°C
Power Dissipation	P_D	700	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to + 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current ($\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{RC}=min.)	KM416C1200L/LL-7	I_{CC1}	—	160	mA
	KM416C1200L/LL-8		—	140	mA
	KM416C1200L/LL-10		—	120	mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$)		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{UCAS}$=$\overline{LCAS}$, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM416C1200L/LL-7	I_{CC3}	—	160	mA
	KM416C1200L/LL-8		—	140	mA
	KM416C1200L/LL-10		—	120	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{PC}=min.)	KM416C1200L/LL-7	I_{CC4}	—	140	mA
	KM416C1200L/LL-8		—	120	mA
	KM416C1200L/LL-10		—	100	mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$≥V_{CC}-0.2V)		I_{CC5}	—	300	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ Cycling @t_{RC}=min.)	KM416C1200L/LL-7	I_{CC6}	—	160	mA
	KM416C1200L/LL-8		—	140	mA
	KM416C1200L/LL-10		—	120	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode Input High Voltage (V_{IH})=V_{CC}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=125μS, T_{RAS}=T_{RAS}min~1μS	KM416C1200L	I_{CC7}	—	500	μA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=V_{IL} $\overline{W}$=$\overline{OE}$=A0~A11 : V_{CC}-0.2V or 0.2V DQ1~16=V_{CC}-0.2V, 0.2V or Open	KM416C1200LL	I_{CCS}	—	500	μA
Input Leakage Current* (Any input 0≤V_{IN}≤6.5V, all other pins not under test =0V)		I_{IL}	-10	10	μA
Output Leakage Current* (Date out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once while $\overline{UCAS}$ and $\overline{UCAS}$=V_{IH}.

CAPACITANCE (T_A=25℃)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_{16})	C_{DQ}	—	7	pF

AC CHARACTERISTICS (0 ℃≤T_A≤70 ℃, V_{CC}=5.0V±10%, See notes 1, 2)

Parameter	Symbol	KM416C1200L/LL-7		KM416C1200L/LL-8		KM416C1200L/LL-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	185		205		245		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	

AC CHARACTERISTICS (0 ℃≤T_A≤70 ℃, V_{CC}=5.0V±10%, See notes 1, 2)

Parameter	Symbol	KM416C1200L/LL-7		KM416C1200L/LL-8		KM416C1200L/LL10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (1024 cycles)	t_{REF}		128		128		128	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	50		50		60		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	100		110		135		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	65		70		85		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		55	ns	3
Fast page mode cycle time	t_{PC}	45		50		60		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	100		105		125		ns	
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	70	100K	80	100K	100	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	45		45		55		ns	
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		20		25		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self rsfresh)	t_{RASS}	100		100		100		μs	19
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self rsfresh)	t_{RPS}	130		150		180		ns	19
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self rsfresh)	t_{CHS}	0		0		0		ns	19

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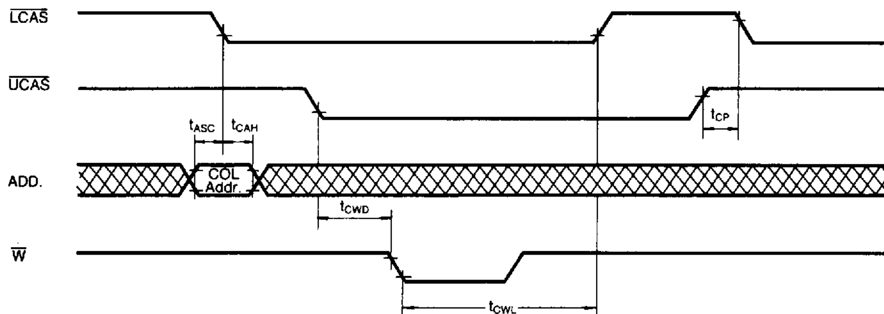
KM416C1200L/LL Truth Table

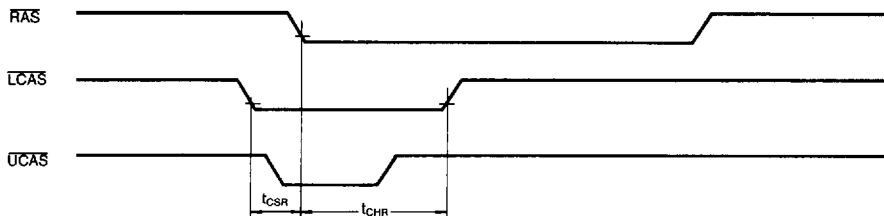
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ_{1-8}	DQ_{9-16}	State
H	H	H	H	H	Hi-Z	Hi-Z	Standby
L	H	H	H	H	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Lower Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	—

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{\text{RAS}}$-only or $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating aprameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{\text{CAS}}$ falling edge.
13. t_{CP} is specified from the last $\overline{\text{CAS}}$ rising edge in the previous cycle to the first $\overline{\text{CAS}}$ falling edge in the next cycle.
14. t_{CWD} is referenced to the later $\overline{\text{CAS}}$ falling edge at word read-modify-write cycle.
15. t_{CWL} is specified from $\overline{\text{W}}$ falling edge to the earlier $\overline{\text{CAS}}$ rising edge.



16. t_{CSR} is referenced to earlier $\overline{\text{CAS}}$ falling low before $\overline{\text{RAS}}$ transition low.
17. t_{CHR} is referenced to the later $\overline{\text{CAS}}$ rising high after $\overline{\text{RAS}}$ transition low.



18. t_{DS}, t_{DH} is independetly specified for lower byte $D_{in(1\sim8)}$, upper byte $D_{in(9\sim16)}$

19. 2048 cycle of Burst Refresh must be executed within 32 ms before and after self refresh, in order to meet refresh specification.

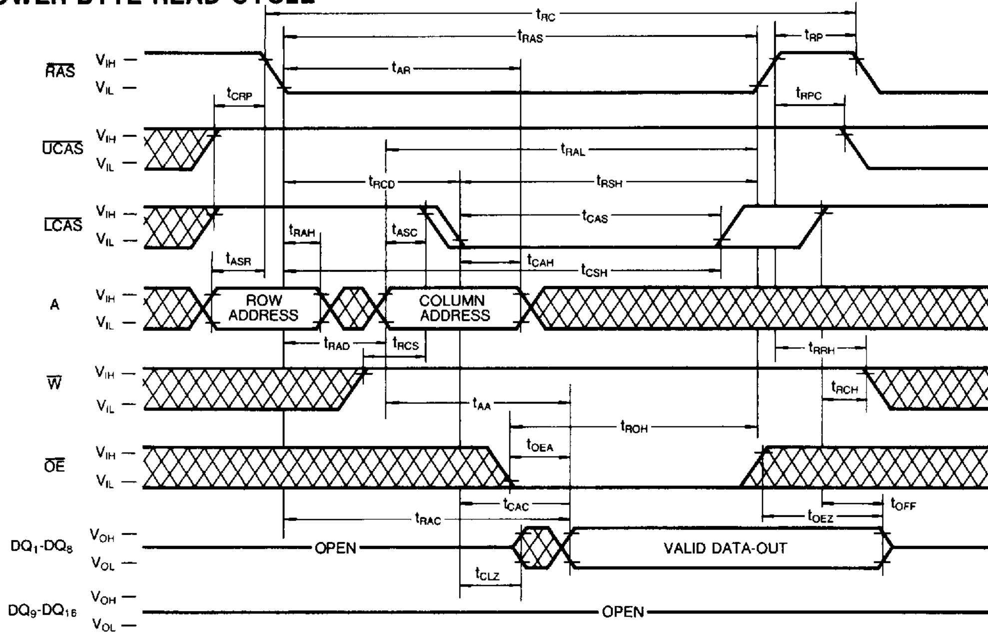
TIMING DIAGRAMS

WORD READ CYCLE

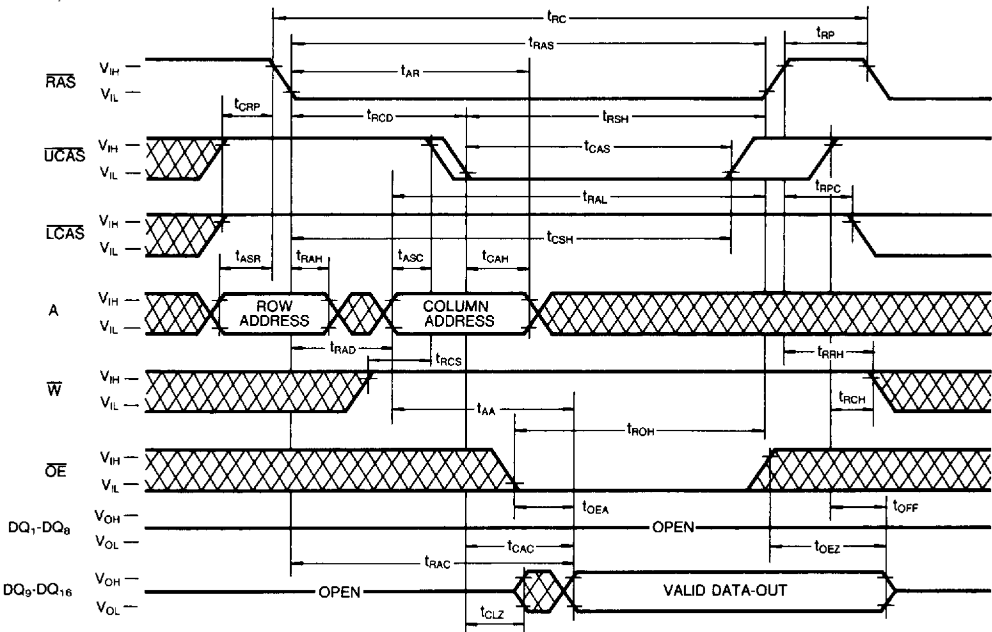
DON'T CARE

TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE



UPPER BYTE READ CYCLE



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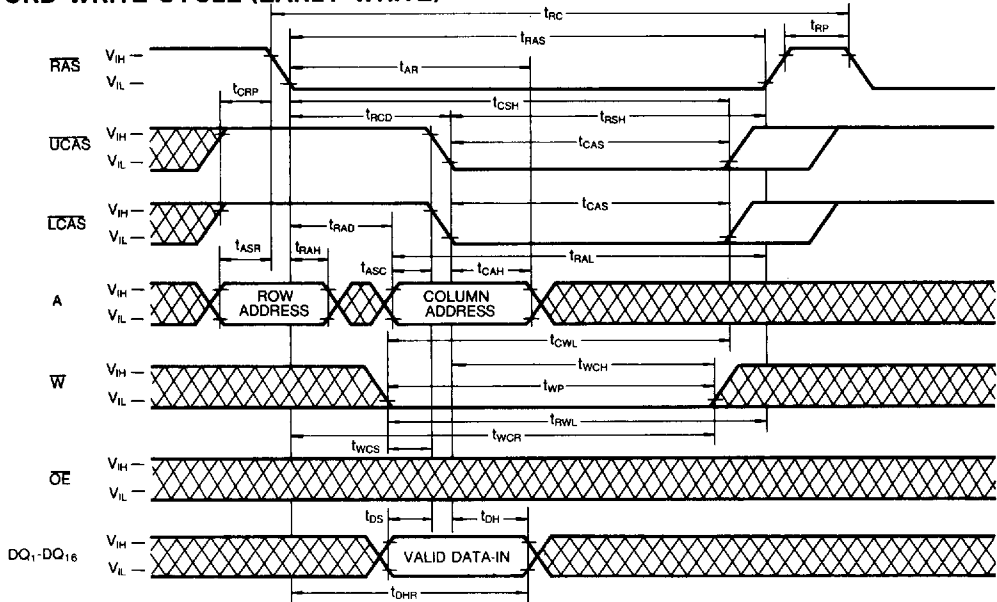
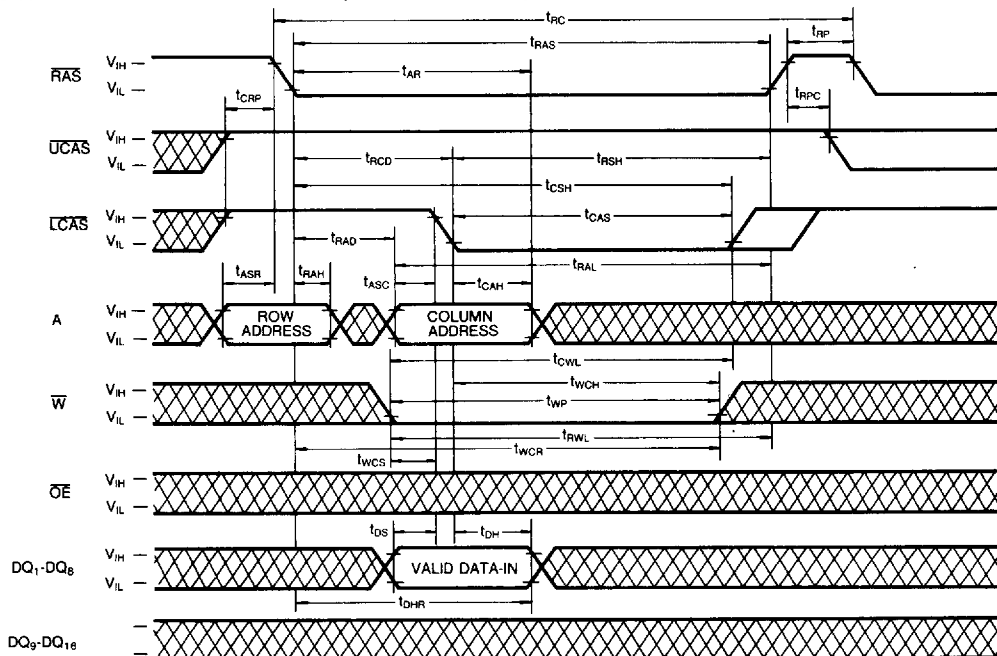
TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)

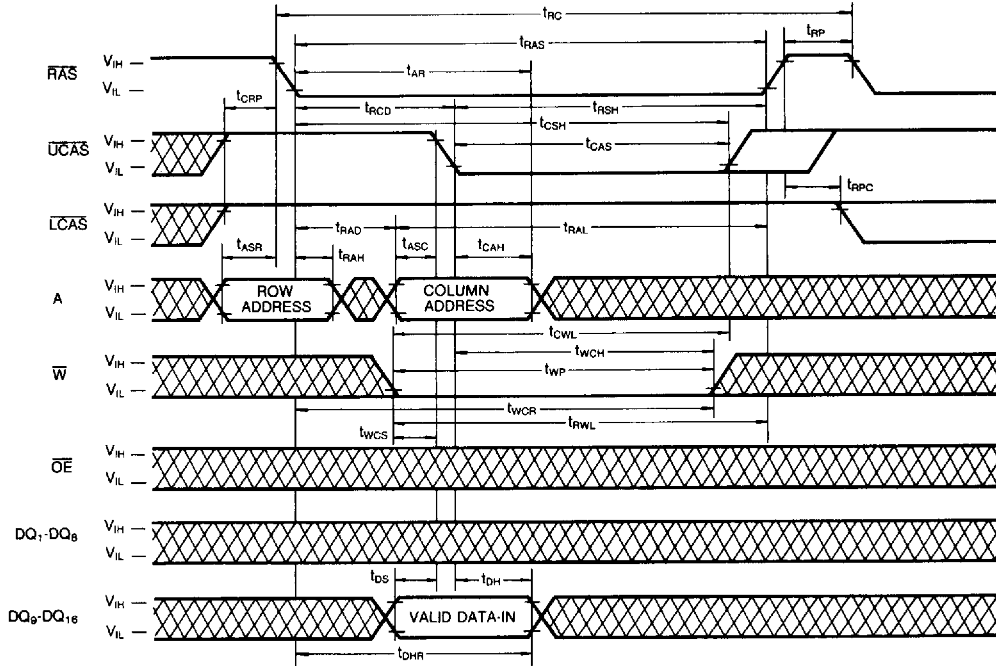


LOWER BYTE WRITE CYCLE (EARLY WRITE)

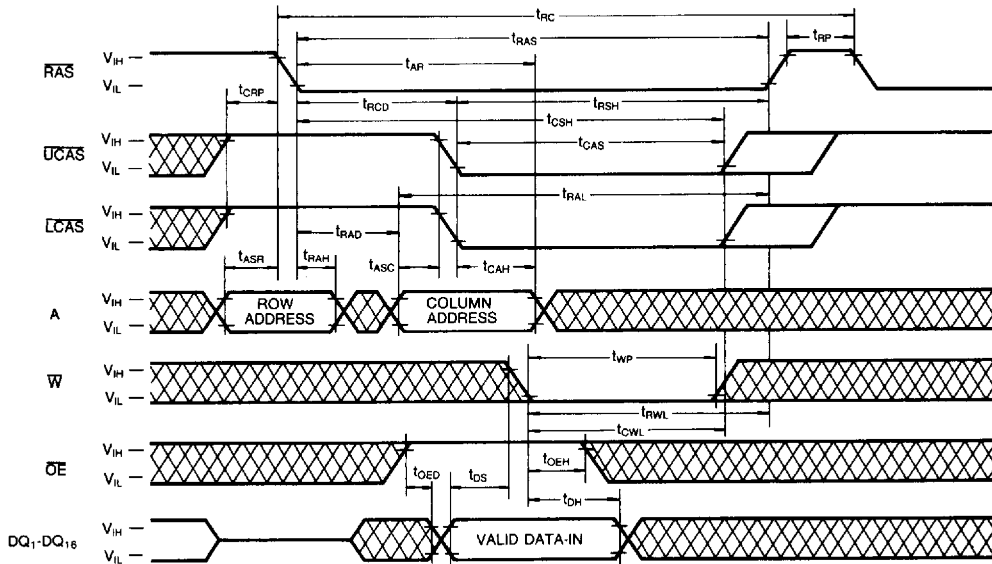


TIMING DIAGRAMS (Continued)

UPPER BYTE WRITE CYCLE (EARLY WRITE)

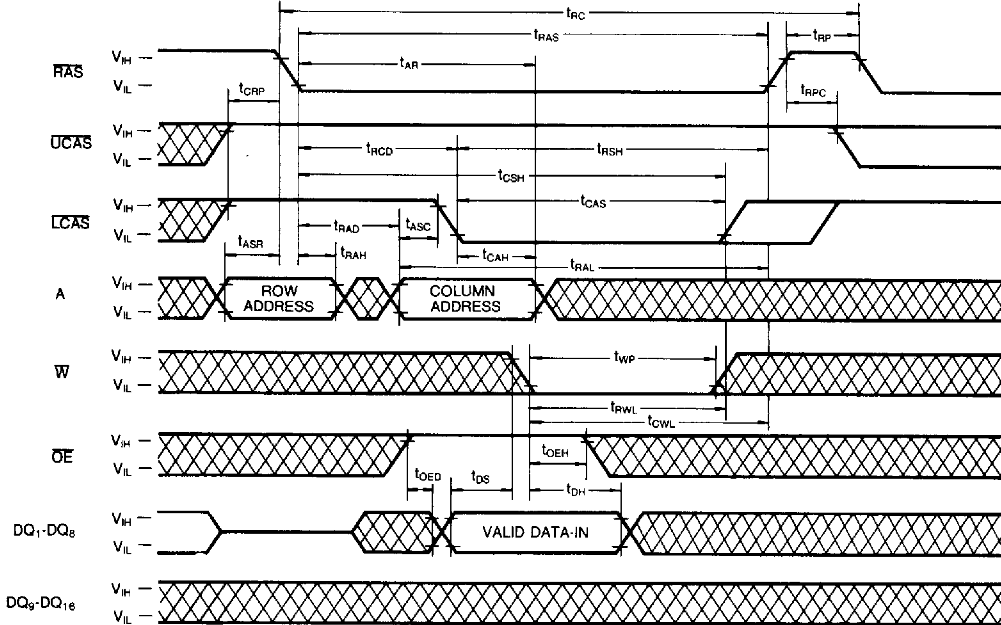


WORD WRITE CYCLE (OE CONTROLLED WRITE)

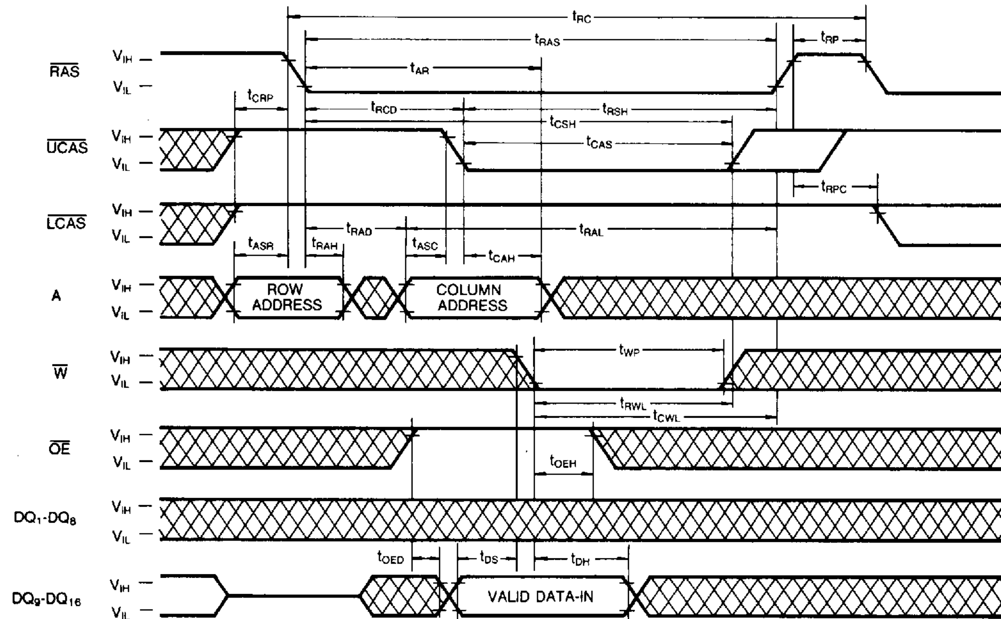


TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



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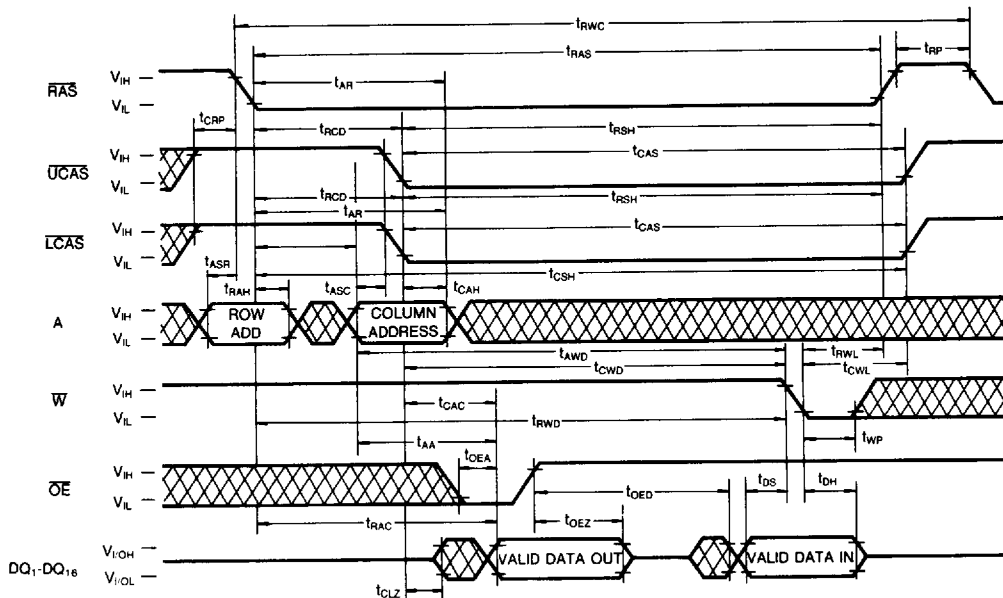
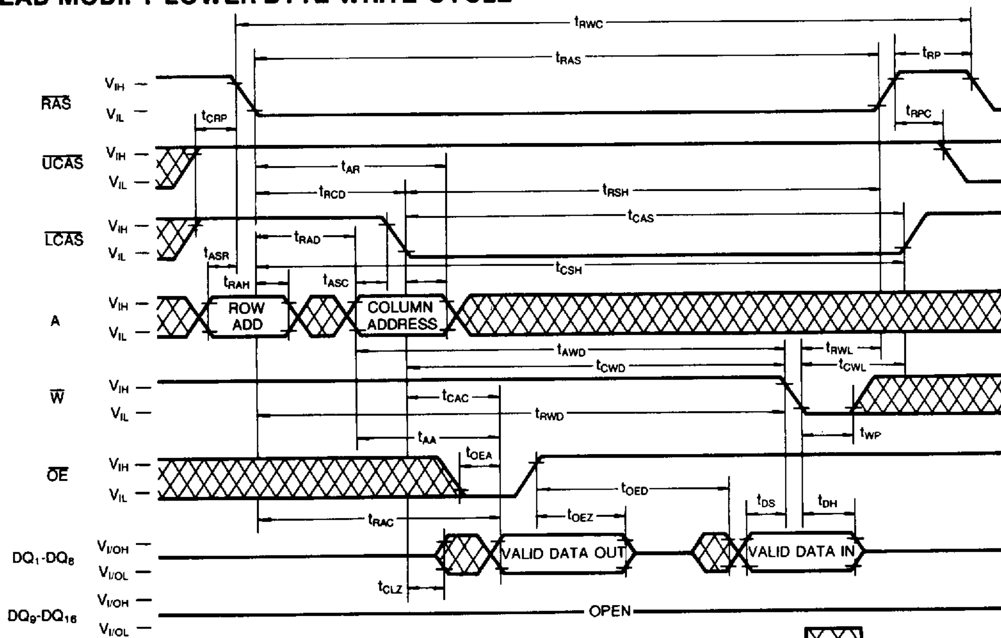
TIMING DIAGRAMS (Continued)

WORD READ-MODIFY-WRITE CYCLE

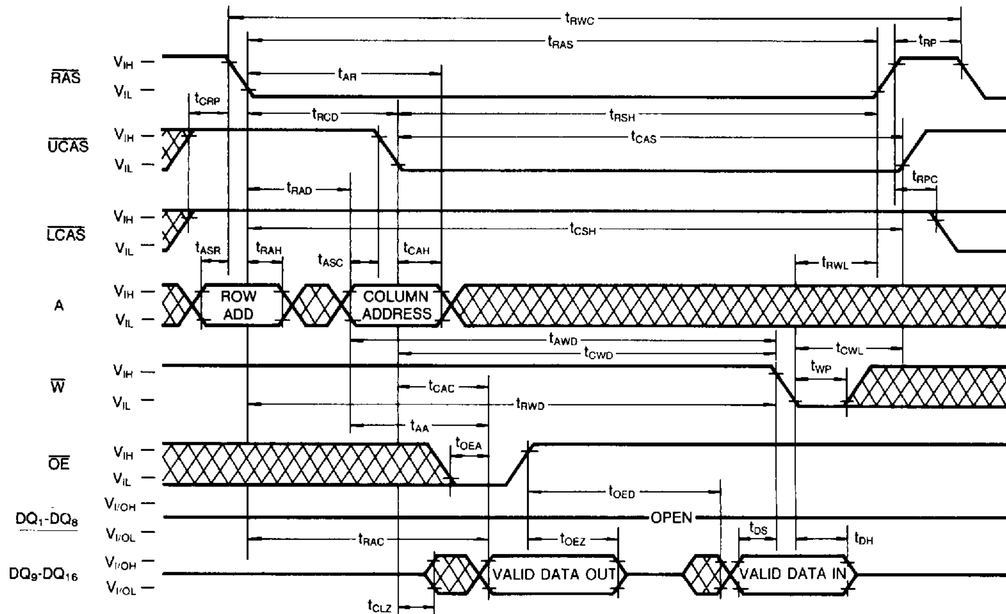


READ-MODIFY-LOWER-BYTE-WRITE CYCLE

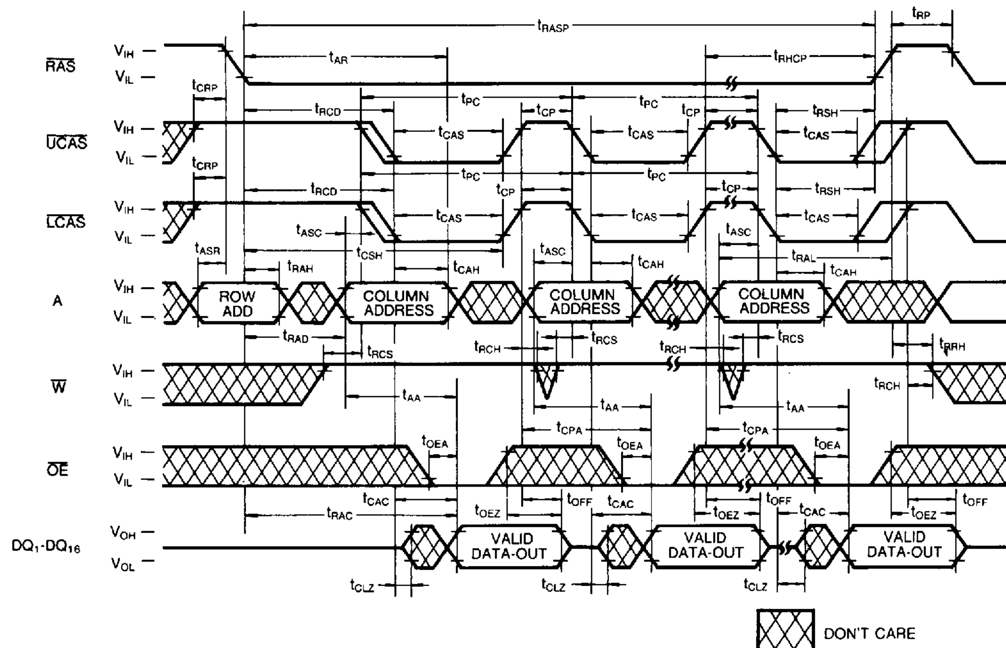


TIMING DIAGRAMS (Continued)

READ-MODIFY-UPPER-BYTE-WRITE CYCLE



FAST PAGE MODE WORD READ CYCLE



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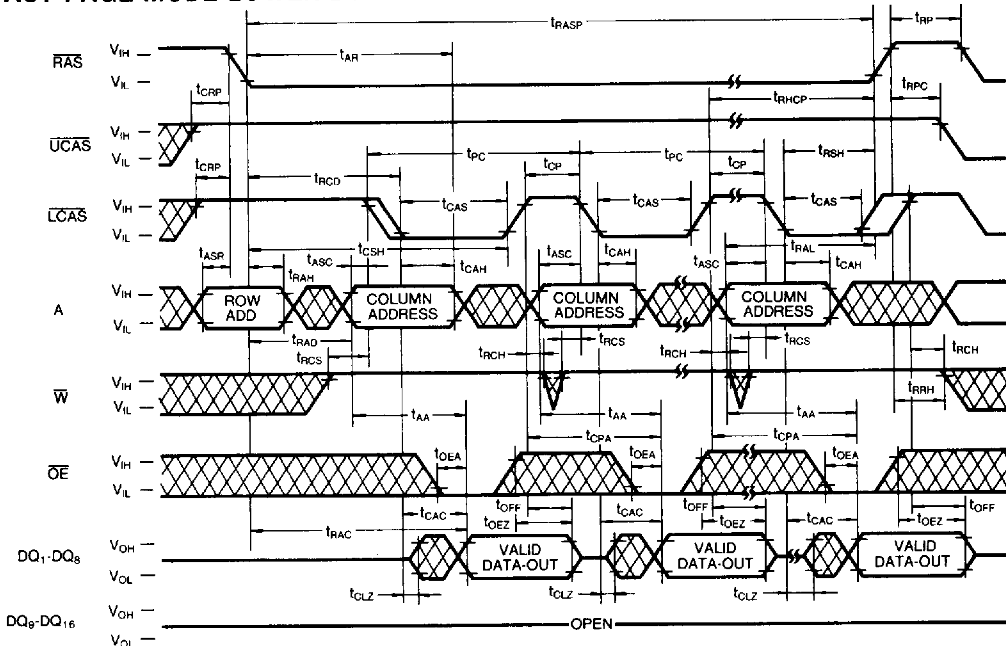
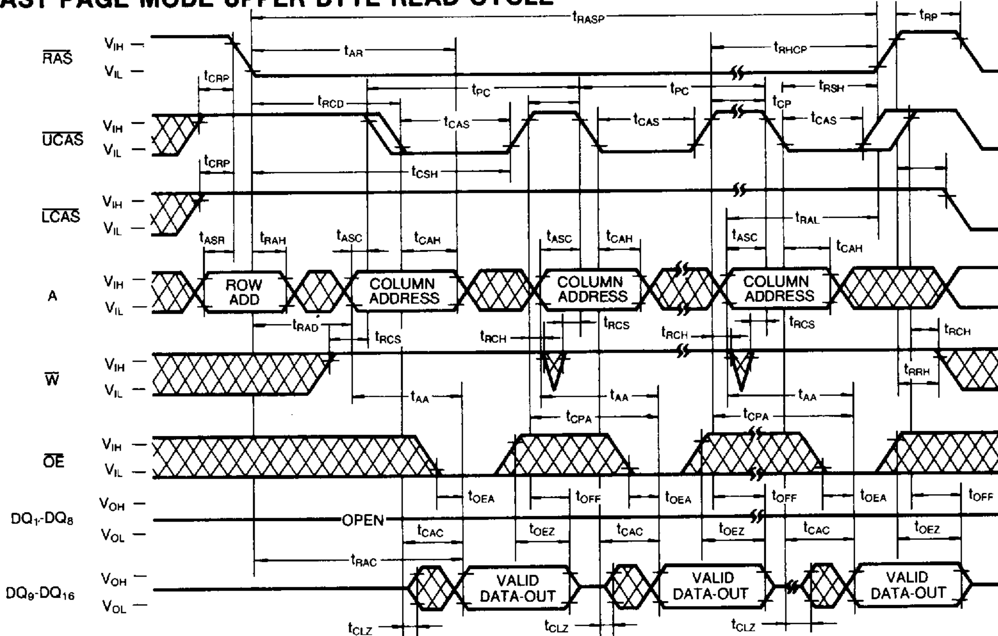
TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER BYTE READ CYCLE



FAST PAGE MODE UPPER BYTE READ CYCLE



TIMING DIAGRAMS (Continued)

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, A, $\overline{W}$, $\overline{OE}$, DQ_1-DQ_{16} (V_{IH} / V_{IL})

Timing labels: t_{RASP}, t_{RP}, t_{AR}, t_{CRP}, t_{RCD}, t_{PC}, t_{CP}, t_{RSH}, t_{CAS}, t_{CSH}, t_{ASR}, t_{ASC}, t_{RAH}, t_{CAH}, t_{RAD}, t_{WCS}, t_{WCH}, t_{WP}, t_{CWL}, t_{RWL}, t_{DS}, t_{DH}, t_{DHR}

ROW ADD / COLUMN ADDRESS / COLUMN ADDRESS / COLUMN ADDRESS

VALID DATA-IN / VALID DATA-IN / VALID DATA-IN

FAST PAGE MODE LOWER BYTE WRITE (EARLY WRITE)

$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, A, $\overline{W}$, $\overline{OE}$, DQ_1-DQ_8, DQ_9-DQ_{16} (V_{IH} / V_{IL})

Timing labels: t_{RASP}, t_{RP}, t_{AR}, t_{RPC}, t_{CRP}, t_{RCD}, t_{PC}, t_{CP}, t_{RSH}, t_{CAS}, t_{CSH}, t_{ASR}, t_{ASC}, t_{RAH}, t_{CAH}, t_{RAD}, t_{WCS}, t_{WCH}, t_{WP}, t_{CWL}, t_{RWL}, t_{DS}, t_{DH}, t_{DHR}

ROW ADD / COLUMN ADDRESS / COLUMN ADDRESS / COLUMN ADDRESS

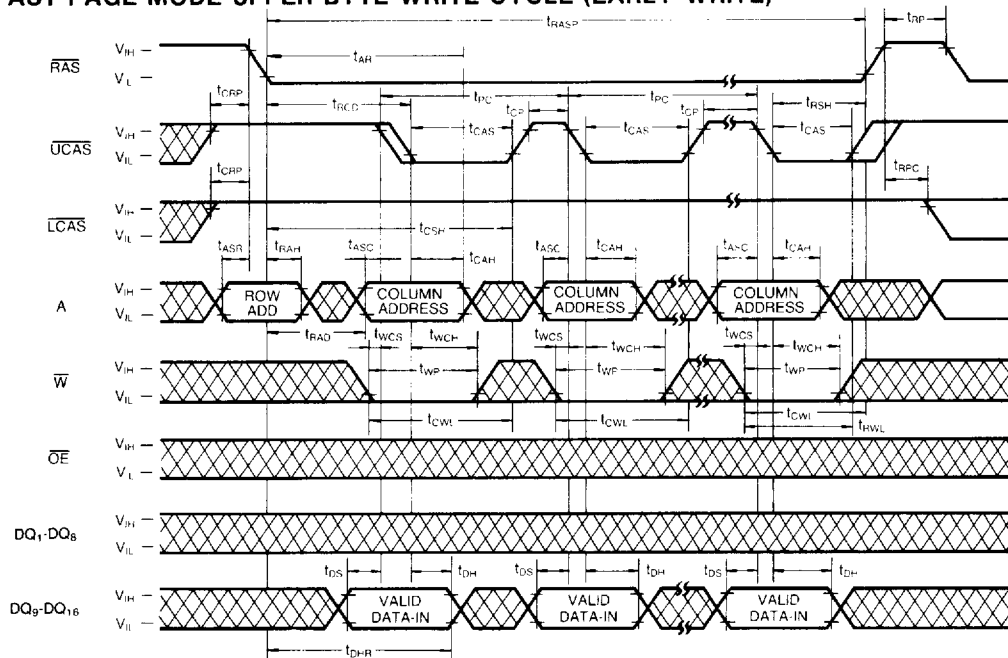
VALID DATA-IN / VALID DATA-IN / VALID DATA-IN

DON'T CARE

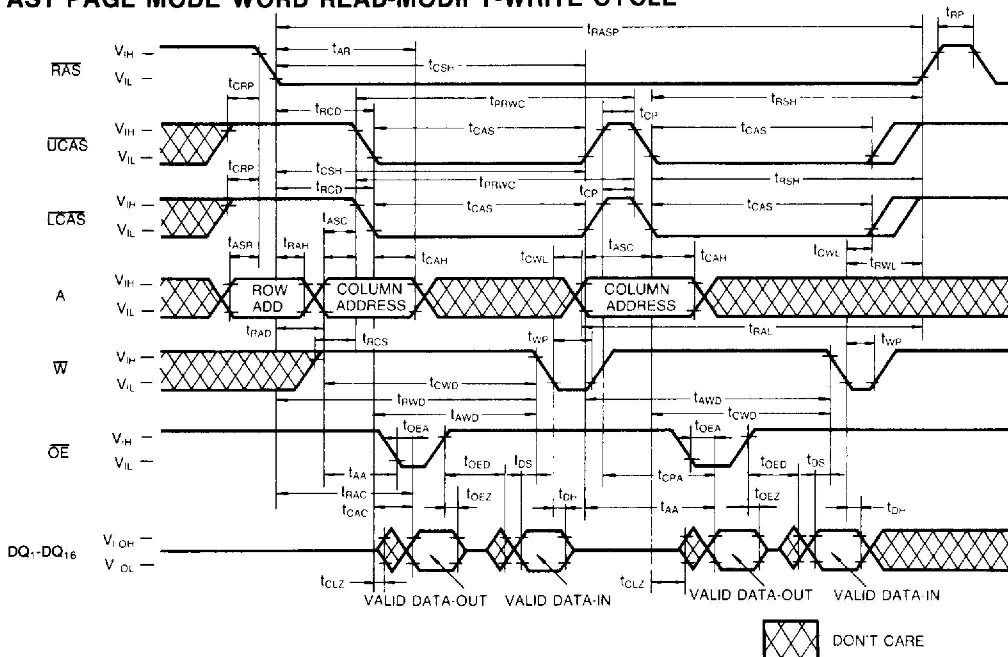
2

TIMING DIAGRAMS (Continued)

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

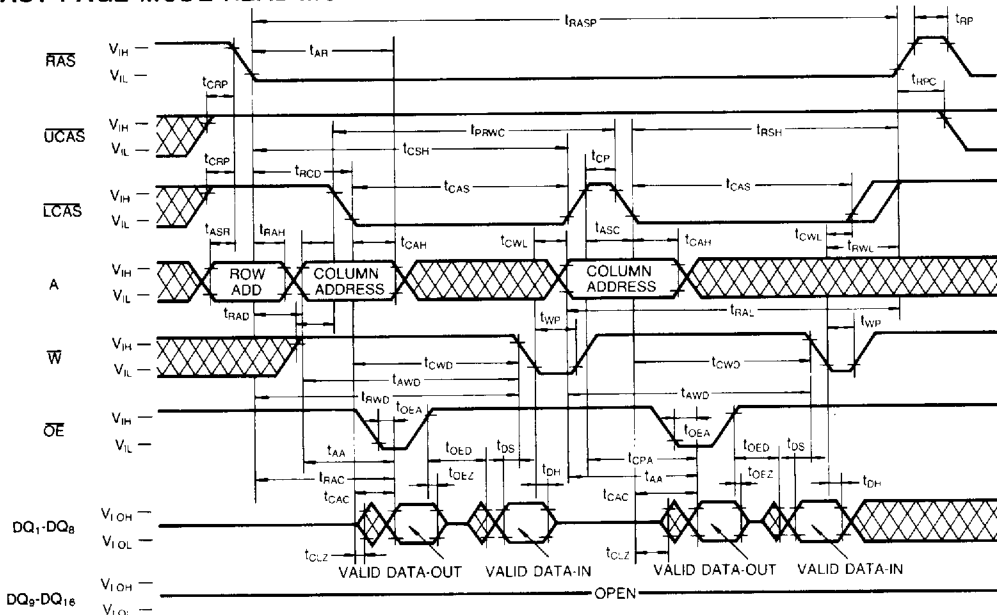


FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE

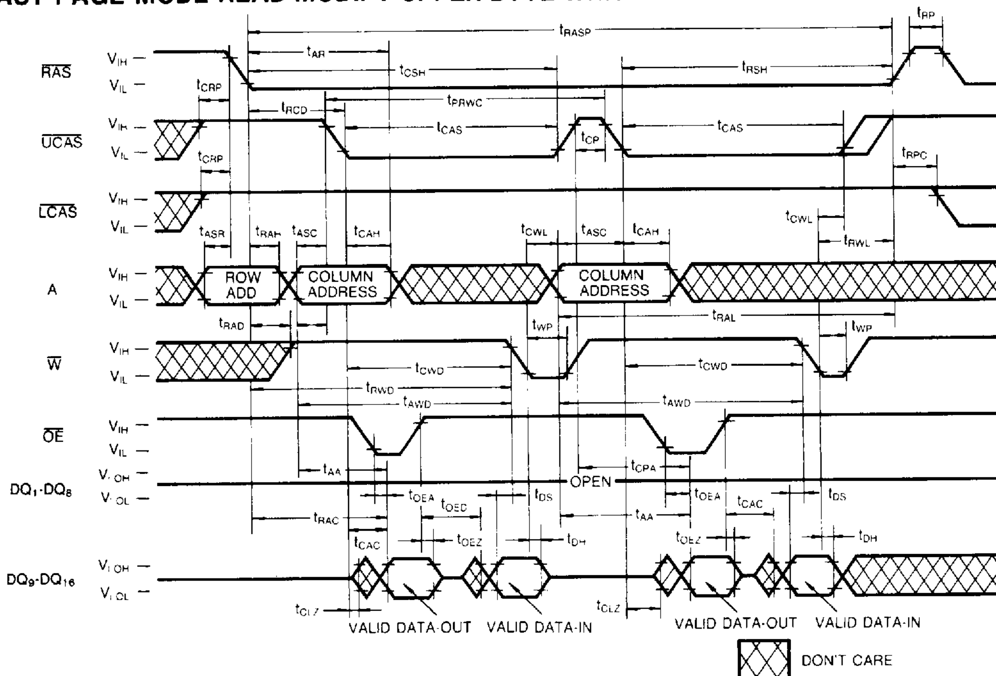


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ-MODIFY-LOWER-BYTE-WRITE CYCLE



FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE

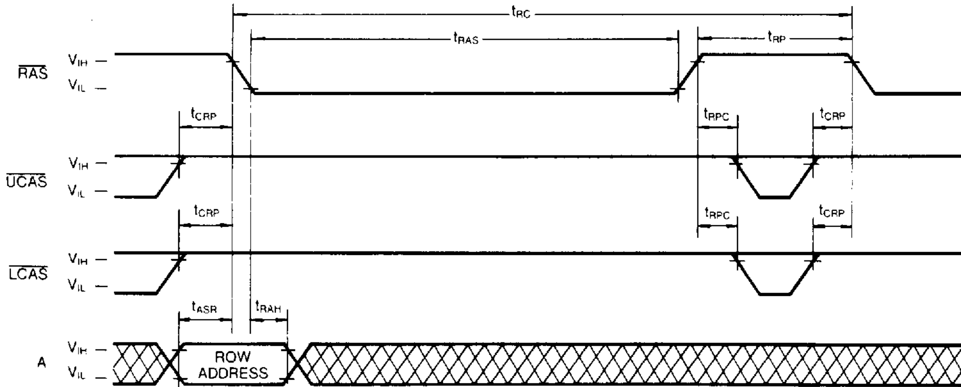


2

TIMING DIAGRAMS (Continued)

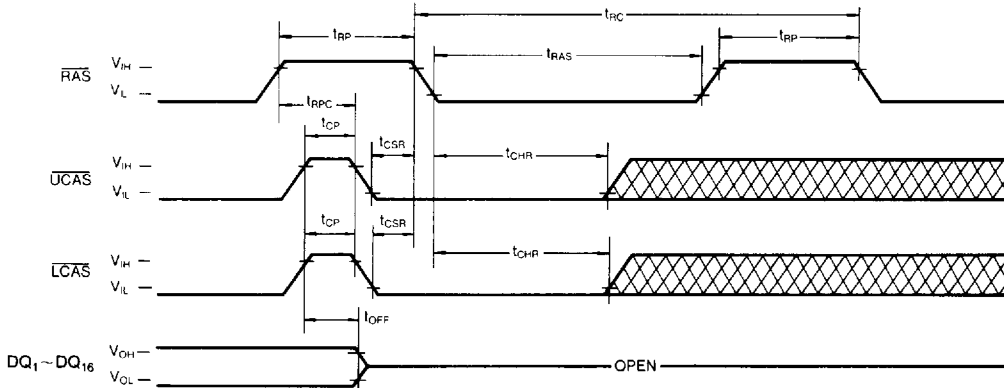
$\overline{RAS}$ ONLY REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$=Don't Care



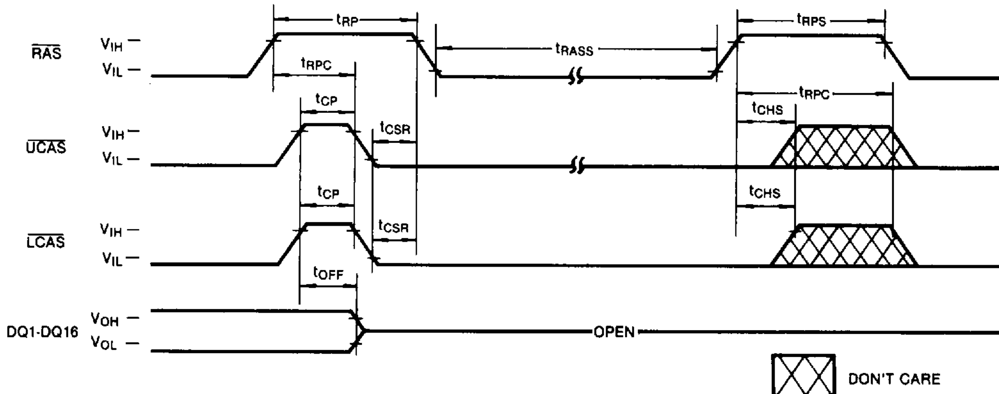
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$, A = Don't Care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$, A = Don't Care



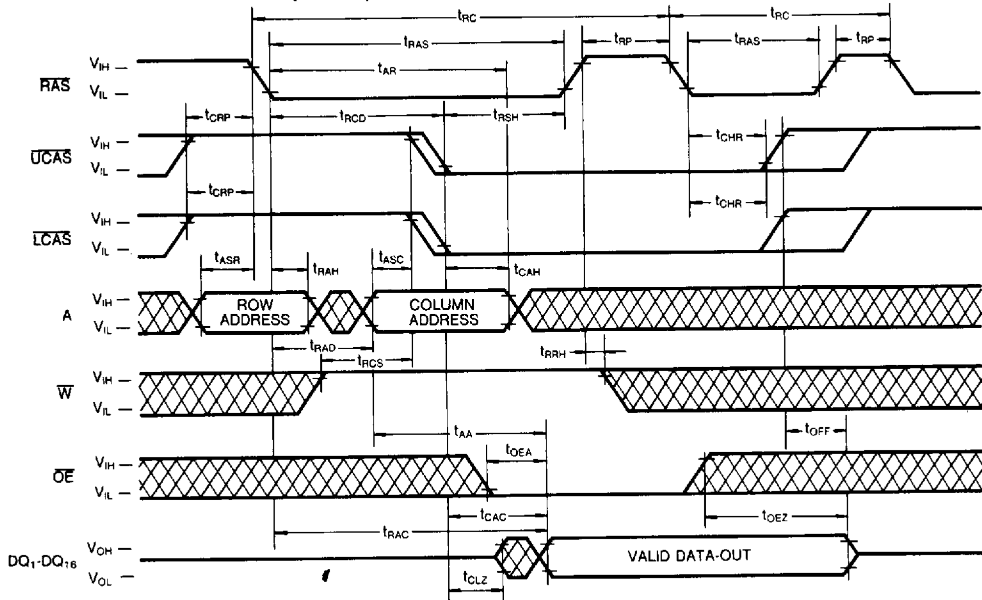
DON'T CARE

SAMSUNG ELECTRONICS

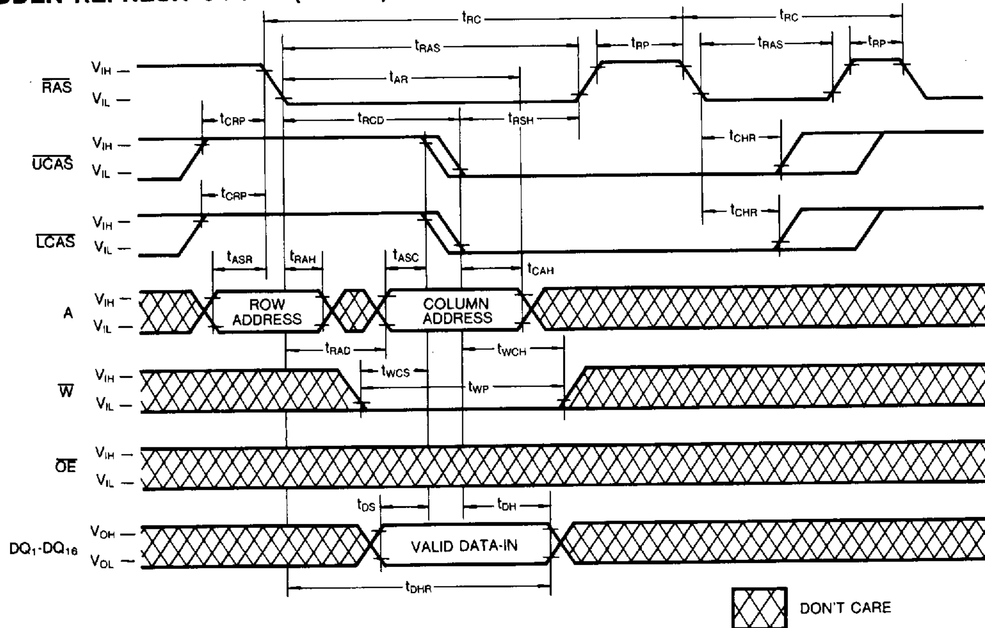
2

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

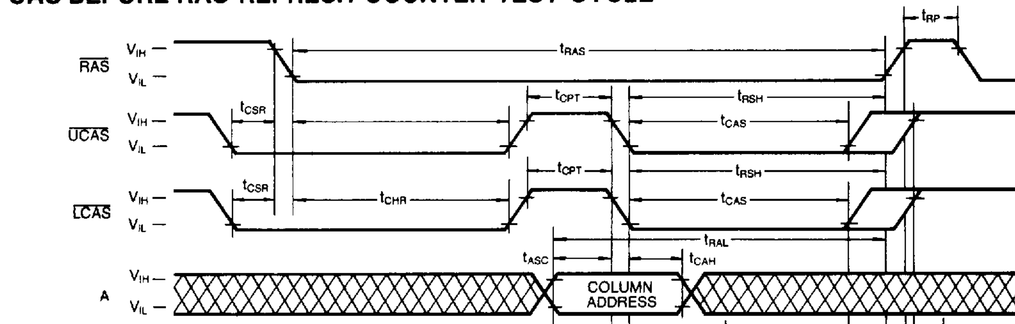


HIDDEN REFRESH CYCLE (WRITE)

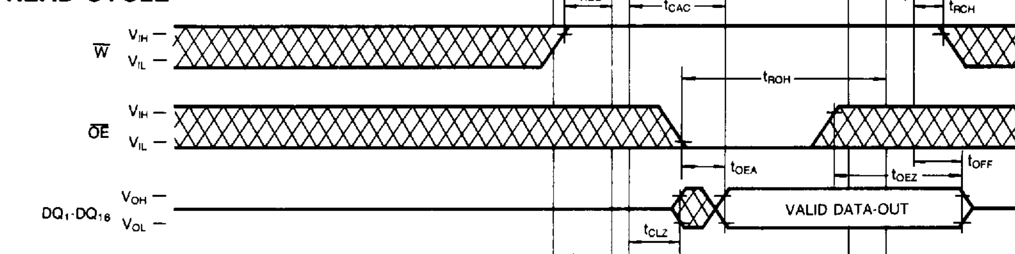


TIMING DIAGRAMS (Continued)

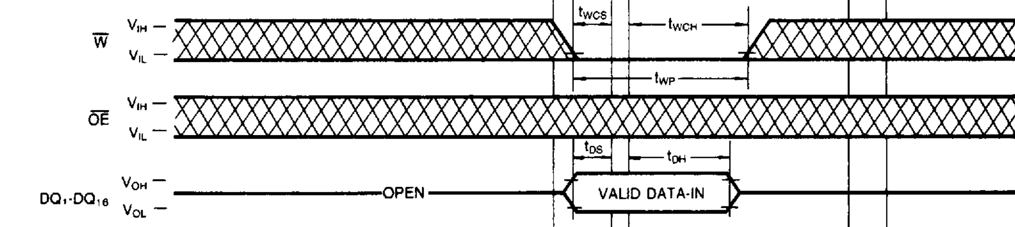
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



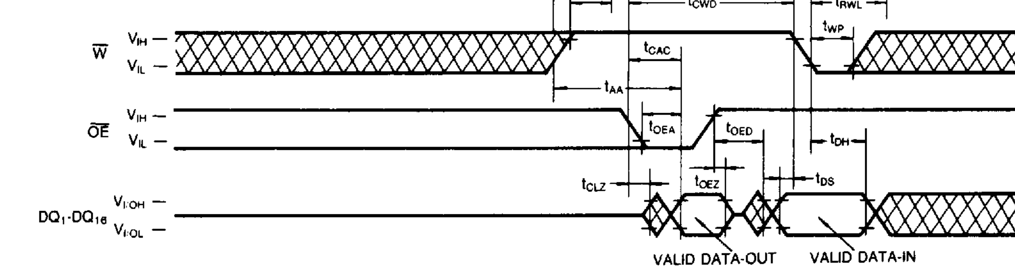
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE



DEVICE OPERATION

Device Operation

The KM416C1200L/LL contains 16,777,216 memory locations arranged in 16 groups of 1,048,576 × 1bit each. Twenty address bits are required to address a particular memory location. Since the KM416C1200L/LL has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{LCAS}$, $\overline{UCAS}$) and the valid row and column address inputs.

Operation of the KM416C1200L/LL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{LCAS}$($\overline{UCAS}$) remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{LCAS}$($\overline{UCAS}$). This is the beginning of any KM416C1200L/LL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relation ships. The cycle is terminated when both $\overline{RAS}$ and $\overline{LCAS}$ ($\overline{UCAS}$) have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time(t_{RP})requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min)and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM416C1200L/LL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{XCAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. Additionally the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If $\overline{XCAS}$ transitions to a low before t_{RCD}(max)then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{XCAS}$ transitions low after t_{RCD}(max)or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD} (max) and t_{RAD}(max).

Write

The KM416C1200L/LL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$, $\overline{LCAS}$ and $\overline{UCAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{XCAS}$, whichever is later.

Early Write : An early write cycle is performed by bringing $\overline{W}$ low before $\overline{XCAS}$. The 16-bit wide data at the data I/O pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write : In this cycle, valid data from the addressed cells appears at the output before and during the time that data is being written into the same cells. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. The $\overline{OE}$ input must be low during the time defined by t_{OEA} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM416C1200L/LL DQ pins.

Data Output

The KM416C1200L/LL has a three-state output buffers which are controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever either $\overline{CAS}$ or $\overline{OE}$ is high(V_{IH}), the outputs are in the high impedance(Hi-Z)state. In any cycle in which valid data appears at the outputs, the outputs enter into the low impedance state in the time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAS} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs(as in hidden refresh). Each of the KM416C1200L/LL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data : Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State : Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write, $\overline{CAS}$-only cycle.

Indeterminate Output State : Delayed Write(t_{CWD} or t_{RWD} times are not met)

2

DEVICE OPERATION (Continued)

Refresh

The data in the KM416C1200L/LL is stored as a charge on microscopic capacitor within each memory cell. The stored charge tends to dissipate over time and will affect data integrity if the charge is not periodically refreshed. Refresh of the individual storage cells is accomplished by accessing all rows within the refresh period(t_{REF})of within 128ms. There are several ways to accomplish this.

RAS-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with RAS while CAS remains high. This cycle must be repeated for each of the 1024 row address (A_0-A_9).

CAS -before-RAS Refresh: The KM416C1200L/LL has CAS-before-RAS on-chip refresh capability that eliminates the need for external refresh addresses. If either LCAS or UCAS in-put is held low for the specified set up time(t_{CSR}) before RAS transitions low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next CAS -before-RAS refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending either LCAS or UCAS input active time and cycling RAS. The hidden refresh cycle is actually a CAS-before-RAS refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Self Refresh: The self refresh is CAS-before-RAS refresh to be used for long periods of standby, such as a battery back-up. In normal CAS-before-RAS condition when RAS is held low above 100μs an internal timer activates an refresh operation of consecutive row addresses in DRAM. The self refresh mode is exited when either RAS or CAS goes high(V_{IH}).

Other Refresh Methods: It is also possible to refresh the KM416C1200L/LL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in the row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general RAS-only or CAS-before-RAS refresh is the preferred method.

Fast Page Mode

The KM416C1200L/LL has Fast page mode capability provides high speed read, write or read-modify-write access to all memory locations within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while RAS is held low to maintain the row address, CAS is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

CAS-before-RAS Refresh Counter Test Cycle

A special timing sequence using the CAS-before-RAS counter test cycle provides a convenient method of verifying the functionality of the CAS-before-RAS refresh activated circuitry. The cycle begins as a CAS-before-RAS refresh operation. Then, if CAS is asserted high and then low again while RAS is asserted low, the read and write operations are enabled. In this method, the row address bits A0 through A9 are supplied by on chip refresh counter.

Power-up

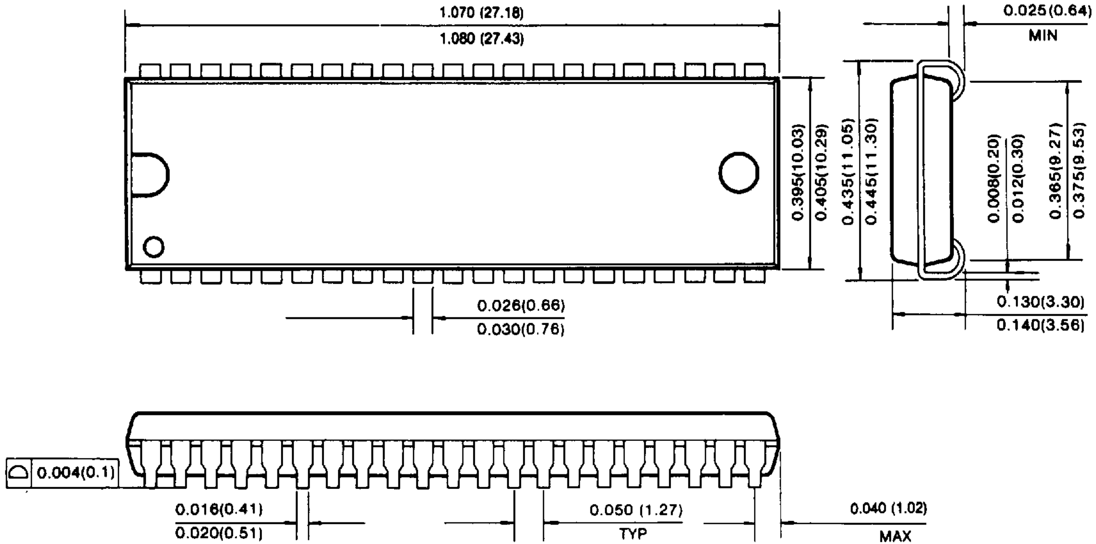
If RAS=V_{SS} during power-up, the KM416C1200L/LL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that RAS and CAS track with V_{CC} during power-up or be held a valid V_{IH} in order to minimize power-up current.

An initial pause of 200μs is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8ms period in which there are no RAS cycles. An initialization cycle is any cycle in which RAS is cycled.

PACKAGE DIMENSION

42-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



44-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)