MOTOROLA

LF355, LF356, LF357* LF355B, LF356B, LF357B*

Specifications and Applications Information

MONOLITHIC JFET INPUT OPERATIONAL AMPLIFIERS

These internally compensated operational amplifiers incorporate highly matched JFET devices on the same chip with standard bipolar transistors. The JFET devices enhance the input characteristics of these operational amplifiers by more than an order of magnitude over conventional amplifiers.

This series of op amps combines the low current characteristics typical of FET amplifiers with the low initial offset voltage and offset voltage stability of bipolar amplifiers. Also, nulling the offset voltage does not degrade the drift or common mode rejection.

- Low Input Bias Current – 30 pA
- Low Input Offset Current – 3.0 pA
- Low Input Offset Voltage – 1.0 mV
- Temperature Compensation of Input Offset Voltage – 3.0 μV/°C
- Low Input Noise Current – 0.01 pA/$\sqrt{Hz}$
- High Input Impedance – $10^{12}\Omega$
- High Common-Mode Rejection Ratio – 100 dB
- High DC Voltage Gain – 106 dB

SERIES FEATURES

- LF355/355B — Low Power Supply Current
- LF356/356B — Wide Bandwidth
- LF357/357B — Wider Bandwidth Decompensated (A_{Vmin} = 5)

	LF355/355B	LF356/356B	LF357/357B
Fast Settling Time to 0.01%	4.0 μs	1.5 μs	1.5 μs
Fast Slew Rate	5.0 V/μs	12 V/μs	50 V/μs
Wide Gain Bandwidth	2.5 MHz	5.0 MHz	20 MHz
Low Input Noise Voltage	20 nV/$\sqrt{Hz}$	12 nV/$\sqrt{Hz}$	12 nV/$\sqrt{Hz}$

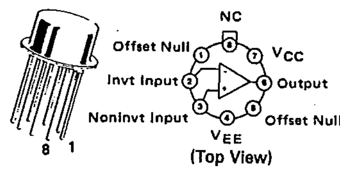
ORDERING INFORMATION

Device	Temperature Range	Package
LF355BH,H LF355BJ,J	0 to +70°C 0 to +70°C	Metal Can Ceramic DIP
LF356BH,H LF356BJ,J	0 to +70°C 0 to +70°C	Metal Can Ceramic DIP
LF357BH,H LF357BJ,J	0 to +70°C 0 to +70°C	Metal Can Ceramic DIP

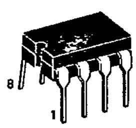
MONOLITHIC JFET OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUITS

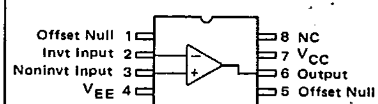
H SUFFIX
METAL PACKAGE
CASE 601-04



(Top View)



J SUFFIX
CERAMIC PACKAGE
CASE 693-02



(Top View)

APPLICATIONS

The LF series is suggested for all general purpose FET input amplifier requirements where precision and frequency response flexibility are of prime importance.

Specific applications include:

- Sample and Hold Circuits
- High Impedance Buffers
- Fast D/A and A/D Converters
- Precision High Speed Integrators
- Wideband, Low Noise, Low Drift Amplifiers

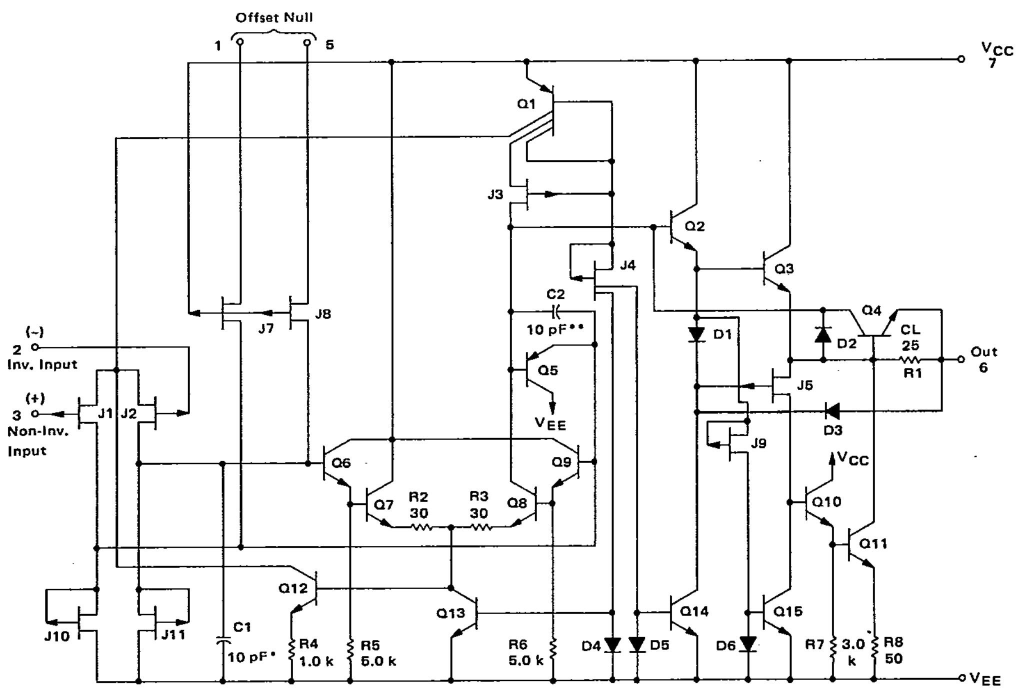
***NOTE:** The LF357/357B are designed for wider bandwidth applications. They are decompensated (A_{Vmin} = 5).

MAXIMUM RATINGS

Rating	Symbol	LF355B/ 356B/357B	LF355/356/357	Unit
Supply Voltage	V_{CC} V_{EE}	+22 −22	+18 −18	V
Differential Input Voltage	V_{ID}	±40	±30	V
Input Voltage Range (Note 1)	V_{IDR}	±20	±16	V
Output Short-Circuit Duration	T_S	Continuous		-
Operating Ambient Temperature Range	T_A	0 to +70		°C
Operating Junction Temperature	T_J	115		°C
Storage Temperature Range	T_{stg}	−65 to +150		°C

Note 1. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

CIRCUIT SCHEMATIC



*C1 = 5.0 pF on LF357.
**C2 = 2.0 pF on LF357.

2

LF355, LF356, LF357, LF355B, LF356B, LF357B

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 15 to 20 V, V_{EE} = −15 to −20 V for LF355B/356B/357B; V_{CC} = 15 V, V_{EE} = −15 V for LF355/356/357; T_A = 0°C to +70°C unless otherwise noted)

Characteristic	Symbol	LF355B/6B/7B Min	Typ	Max	LF355/6/7 Min	Typ	Max	Unit
Input Offset Voltage (R_S = 50 Ω, V_{CM} = 0)	V_{IO}							mV
(T_A = 25°C)		—	3.0	5.0	—	3.0	10	
(Over Temperature)		—	—	6.5	—	—	13	
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω)	$\Delta V_{IO}/\Delta T$	—	5.0	—	—	5.0	—	µV/°C
Change in Average TC with V_{IO} Adjust (R_S = 50 Ω) (Note 2)	$\Delta TC/\Delta V_{IO}$	—	0.5	—	—	0.5	—	µV/°C per mV
Input Offset Current (V_{CM} = 0) (Note 3)	I_{IO}							
(T_J = 25°C)		—	3.0	20	—	3.0	50	pA
(T_J ≤ 70°C)		—	—	1.0	—	—	2.0	nA
Input Bias Current (V_{CM} = 0) (Note 3)	I_{IB}							
(T_J = 25°C)		—	30	100	—	30	200	pA
(T_J ≤ 70°C)		—	—	5.0	—	—	8.0	nA
Input Resistance (T_J = 25°C)	r_i	—	10^{12}	—	—	10^{12}	—	Ω
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k, V_{CC} = 15 V, V_{EE} = −15 V)	A_{VOL}							V/mV
(T_A = 25°C)		50	200	—	25	200	—	
(0°C ≤ T_A ≤ +70°C)		25	—	—	15	—	—	
Output Voltage Swing	V_O							V
(V_{CC} = 15 V, V_{EE} = −15 V, R_L = 10 kΩ)		±12	±13	—	±12	±13	—	
(V_{CC} = 15 V, V_{EE} = −15 V, R_L = 2 kΩ)		±10	±12	—	±10	±12	—	
Input Common-Mode Voltage Range (V_{CC} = 15 V, V_{EE} = −15 V)	V_{ICR}	±11	+15.1 −12.0	—	±10	+15.1 −12.0	—	V
Common-Mode Rejection Ratio	CMRR	85	100	—	80	100	—	dB
Supply Voltage Rejection Ratio (Note 4)	PSRR	85	100	—	80	100	—	dB
Supply Current (T_A = 25°C, V_{CC} = 15 V, V_{EE} = −15 V)	I_D							mA
LF355B/355		—	2.0	4.0	—	2.0	4.0	
LF356B/357B		—	5.0	7.0	—	—	—	
LF356/357		—	—	—	—	5.0	10	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = −15 V, T_A = 25°C)

Characteristic	Symbol	LF355B/355 Min	Typ	Max	LF356B/356 Min	Typ	Max	LF357B/357 Min	Typ	Max	Unit
Slew Rate (Note 5)	SR										V/µs
(A_V = 1) LF355/356		—	5.0	—	7.5	12	—	—	—	—	
(A_V = 5) LF357		—	—	—	—	—	—	30	50	—	
Gain-Bandwidth Product	GBW	—	2.5	—	—	5.0	—	—	20	—	MHz
Settling Time to 0.01% (Note 6)	t_s	—	4.0	—	—	1.5	—	—	1.5	—	µs
Equivalent Input Noise Voltage	e_n										nV/√Hz
(R_S = 100 Ω, f = 100 Hz)		—	25	—	—	15	—	—	15	—	
(R_S = 100 Ω, f = 1000 Hz)		—	20	—	—	12	—	—	12	—	
Equivalent Input Noise Current	i_n										pA/√Hz
(f = 100 Hz)		—	0.01	—	—	0.01	—	—	0.01	—	
(f = 1000 Hz)		—	0.01	—	—	0.01	—	—	0.01	—	
Input Capacitance	C_i	—	3.0	—	—	3.0	—	—	3.0	—	pF

NOTES

(1) Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply.

(2) The temperature coefficient of the adjusted input offset voltage changes only a small amount (0.5 µV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

(3) The input bias currents approximately double for every 10°C rise in junction temperature, T_J. Due to limited test time, the input bias currents are correlated to junction temperature. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

(4) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

(5) The Min. slew rate limits apply for the LF356B and the LF357B, but do not apply for the LF356 or LF357.

(6) Settling time is defined here, for a unity gain inverter connection using 2.0 k resistors for the LF355/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10 V step input is applied to the inverter. For the LF357, A_V = −5.0, the feedback resistor from output to input is 2.0 k and the output step is 10 V (see settling time test circuit).

TYPICAL DC PERFORMANCE CHARACTERISTICS
(Curves are for LF355, LF356, and LF357 series unless otherwise specified)
INPUT BIAS CURRENT versus CASE TEMPERATURE

FIGURE 1 — (LF355 SERIES)

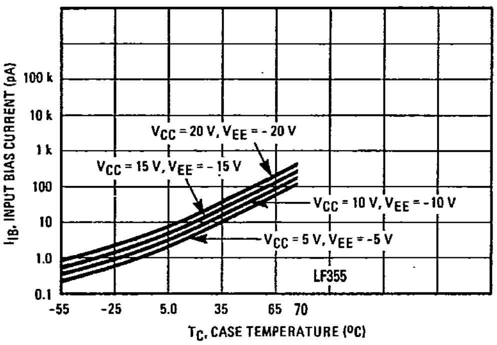


FIGURE 2 — (LF356 AND LF357 SERIES)

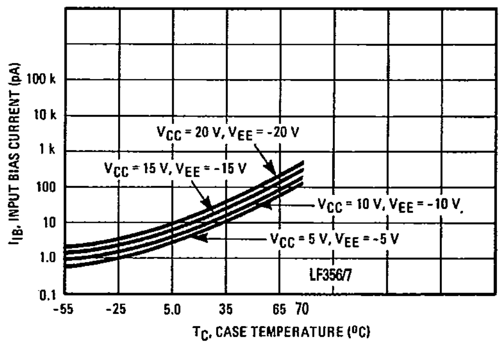


FIGURE 3 — INPUT BIAS CURRENT versus INPUT COMMON-MODE VOLTAGE

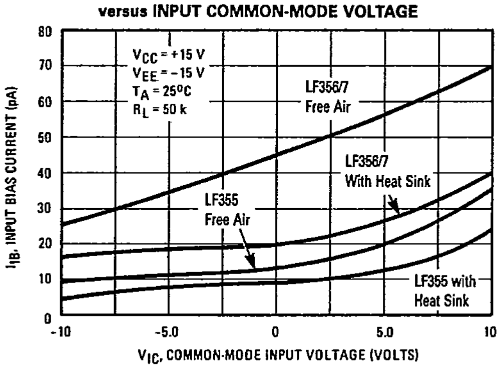
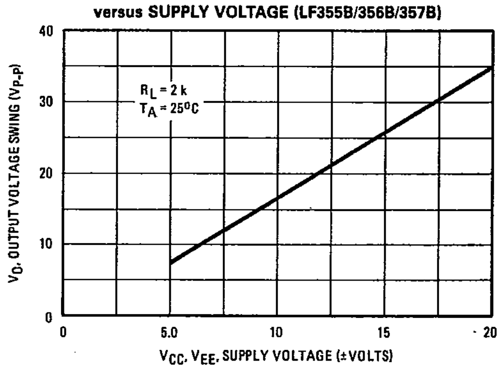


FIGURE 4 — OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE (LF355B/356B/357B)



SUPPLY CURRENT versus SUPPLY VOLTAGE

FIGURE 5 — (LF355 SERIES)

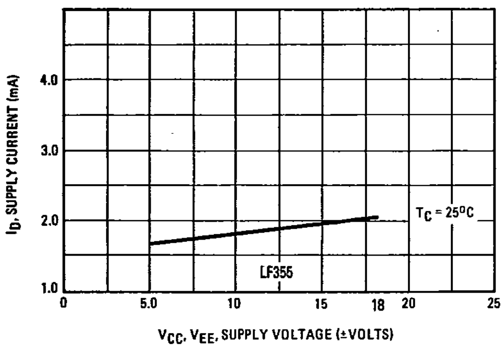
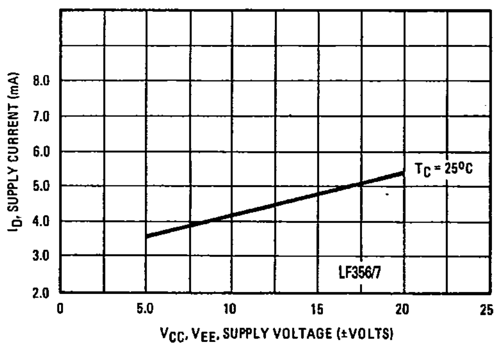


FIGURE 6 — (LF356 AND LF357 SERIES)



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TYPICAL DC PERFORMANCE CHARACTERISTICS (continued)

FIGURE 7 — NEGATIVE CURRENT LIMIT

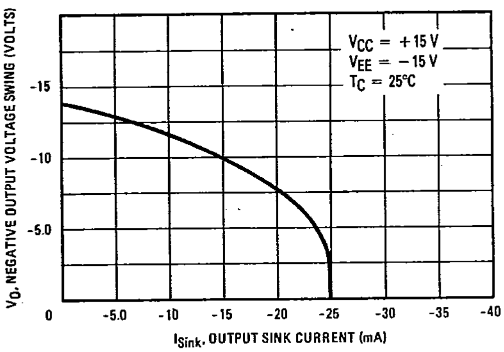


FIGURE 8 — POSITIVE CURRENT LIMIT

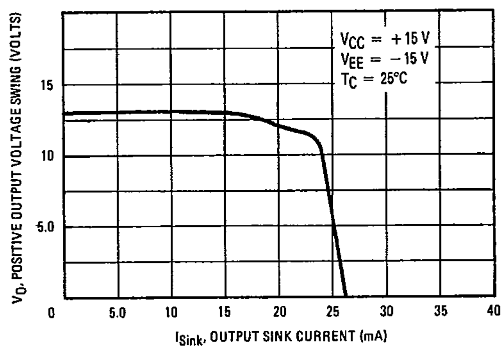


FIGURE 9 — POSITIVE COMMON-MODE INPUT VOLTAGE LIMIT

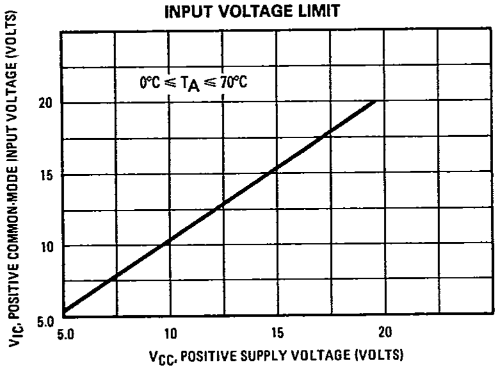


FIGURE 10 — NEGATIVE COMMON-MODE INPUT VOLTAGE LIMIT

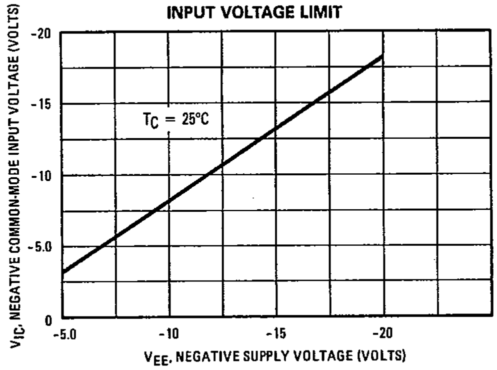


FIGURE 11 — OPEN LOOP VOLTAGE GAIN

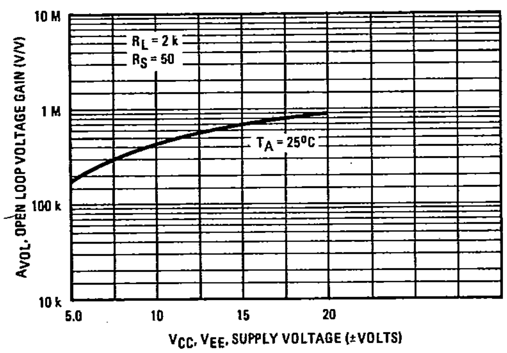
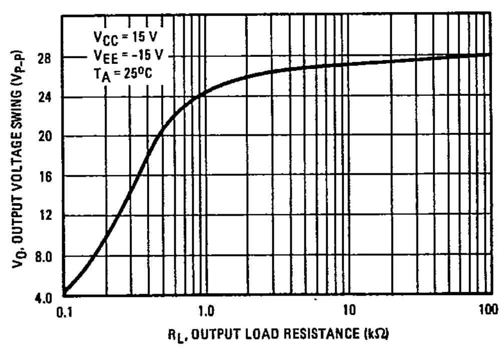


FIGURE 12 — OUTPUT VOLTAGE SWING versus LOAD RESISTANCE



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TYPICAL AC PERFORMANCE CHARACTERISTICS

GAIN BANDWIDTH PRODUCT

FIGURE 13 — (LF355 SERIES)

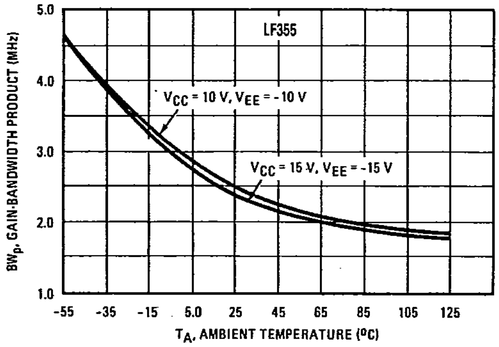
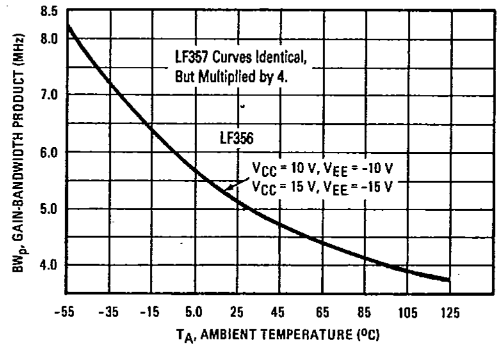


FIGURE 14 — (LF356/357 SERIES)



INVERTER SETTLING TIME

FIGURE 15 — (LF355 SERIES)

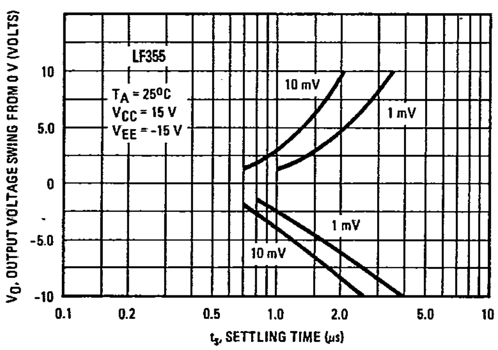


FIGURE 16 — (LF356 AND LF357 SERIES)

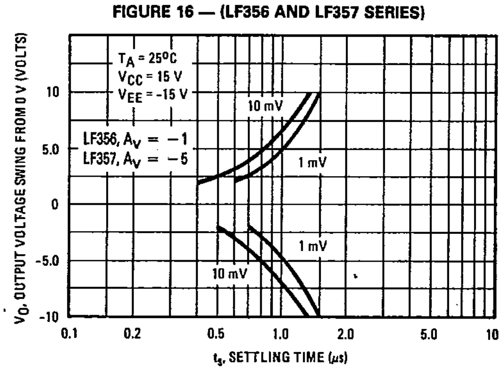


FIGURE 17 — NORMALIZED SLEW RATE

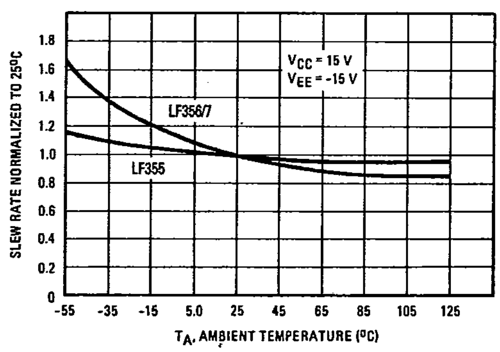
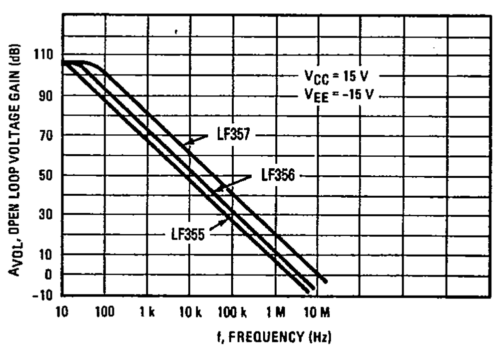


FIGURE 18 — OPEN LOOP FREQUENCY RESPONSE



LF355, LF356, LF357, LF355B, LF356B, LF357B

TYPICAL AC PERFORMANCE CHARACTERISTICS (continued)

BODE PLOT

FIGURE 19 — (LF355 SERIES)

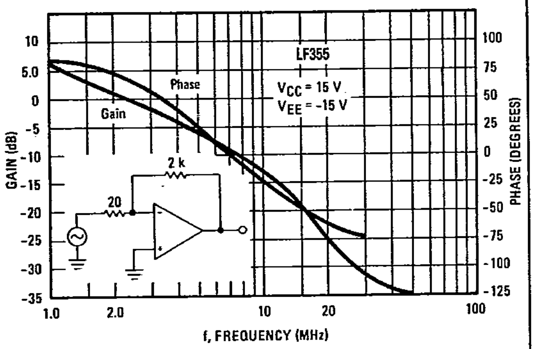


FIGURE 20 — (LF356 SERIES)

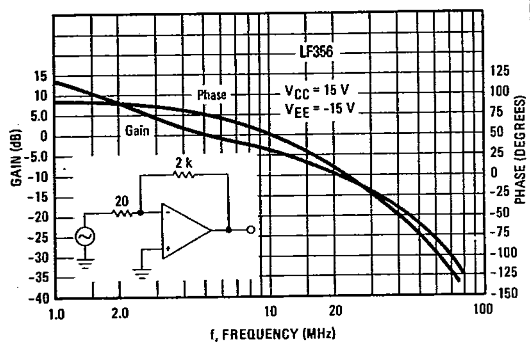
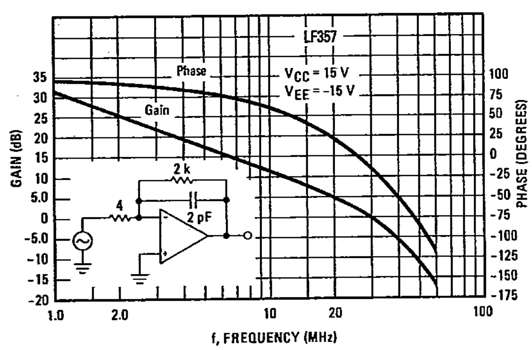


FIGURE 21 — (LF357 SERIES)



OUTPUT IMPEDANCE

FIGURE 22 — (LF355 SERIES)

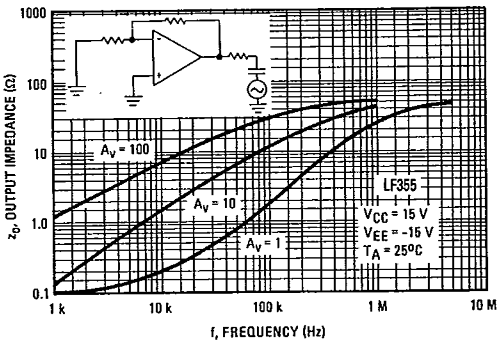


FIGURE 23 — (LF356 SERIES)

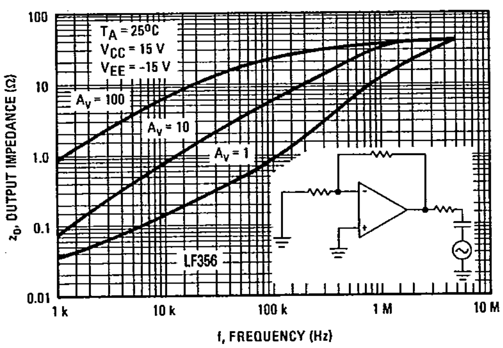
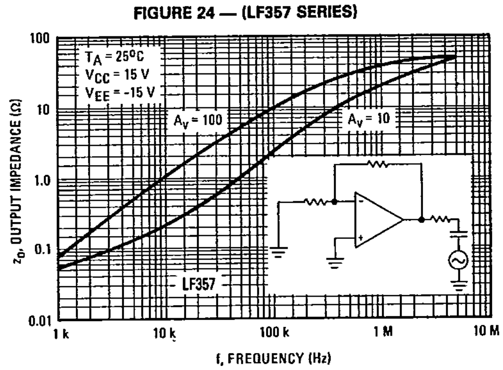


FIGURE 24 — (LF357 SERIES)



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TYPICAL AC PERFORMANCE CHARACTERISTICS (continued)

FIGURE 25 — COMMON-MODE REJECTION RATIO

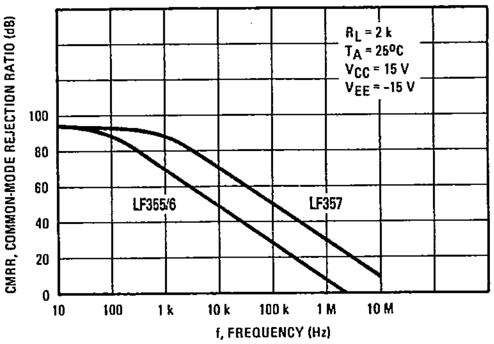
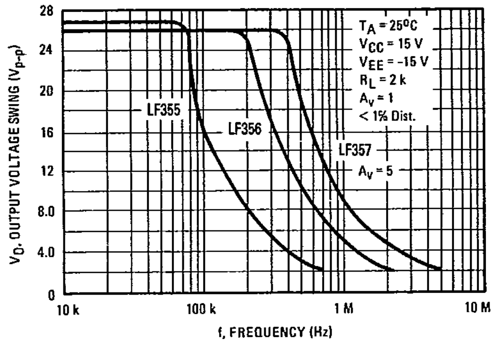


FIGURE 26 — UNDISTORTED OUTPUT VOLTAGE SWING



POWER SUPPLY VOLTAGE REJECTION RATIO

FIGURE 27 — (LF355 SERIES)

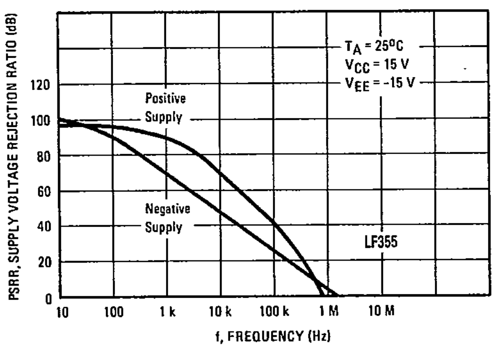
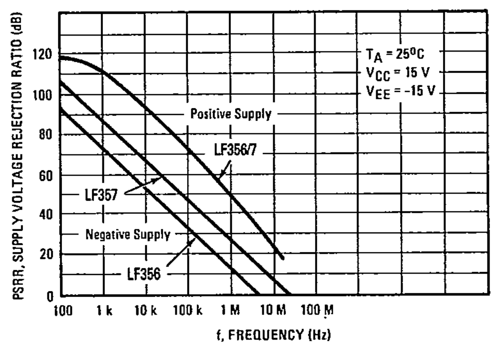


FIGURE 28 — (LF356 AND LF357 SERIES)



EQUIVALENT NOISE VOLTAGE

FIGURE 29 — (LF355/356/357 SERIES)

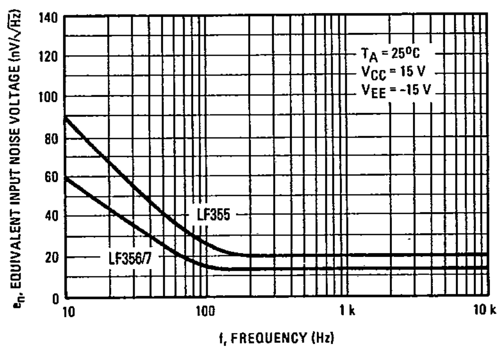
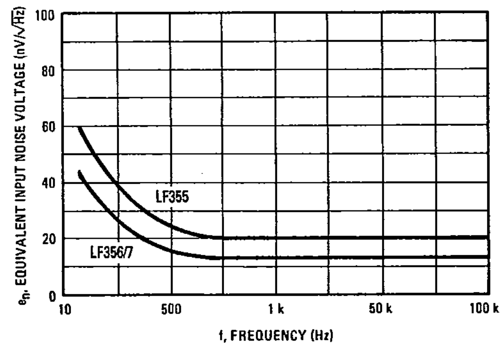
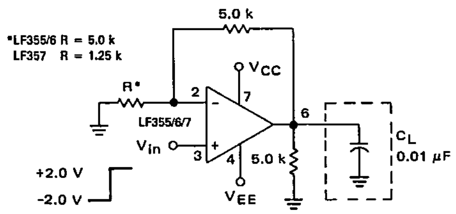


FIGURE 30 (EXPANDED SCALE)



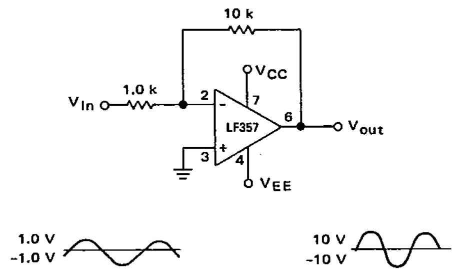
TYPICAL CIRCUIT CONNECTIONS

FIGURE 31 — DRIVING CAPACITIVE LOADS



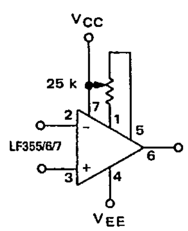
Due to a unique output stage design these amplifiers have the ability to drive large capacitive loads and still maintain stability.
$C_{L(max)} \cong 0.01\ \mu F$.
Overshoot ⩽ 20%
Settling time (t_s) ≅ 5.0 µs

FIGURE 32 — LARGE POWER BANDWIDTH AMPLIFIER



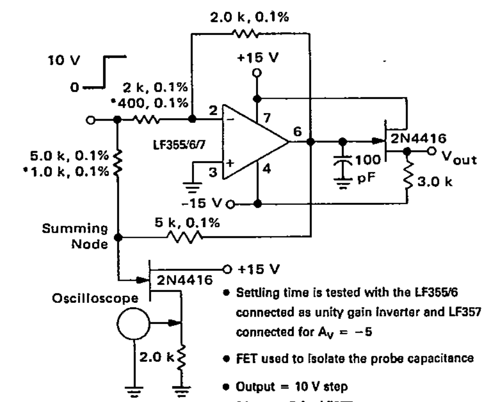
For distortion < 1% and a 20 Vp-p V_{Out} swing, power bandwidth is: 500 kHz.

FIGURE 33 — INPUT OFFSET VOLTAGE ADJUSTMENT



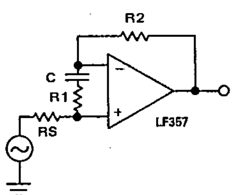
- V_{IO} is adjusted with a 25 k potentiometer
- The potentiometer wiper is connected to V_{CC}
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5 µV/°C/mV of adjustment.
- Typical overall drift: 5.0 µV/°C ±(0.5 µV/°C/mV of adjustment.)

FIGURE 34 — SETTLING TIME TEST CIRCUIT



- Settling time is tested with the LF355/6 connected as unity gain inverter and LF357 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10 V step
  *$A_V = -5$ for LF357

FIGURE 35 — NONINVERTING UNITY GAIN OPERATION FOR LF357



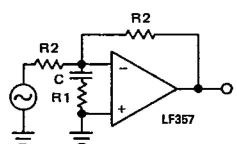
$R1C \geq \frac{1}{(2\pi)(5\ MHz)}$

$R1 = \frac{R2 + R_S}{4}$

$A_{V(DC)} = 1$

$f_{-3dB} \approx 5\ MHz$

FIGURE 36 — INVERTING UNITY GAIN FOR LF357



$R1C \geq \frac{1}{(2\pi)(5\ MHz)}$

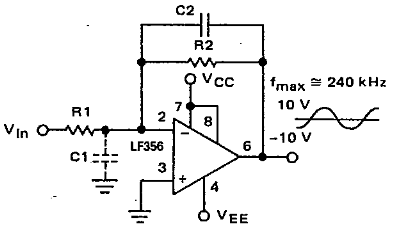
$R1 = \frac{R2}{4}$

$A_{V(DC)} = -1$

$f_{-3dB} \approx 5\ MHz$

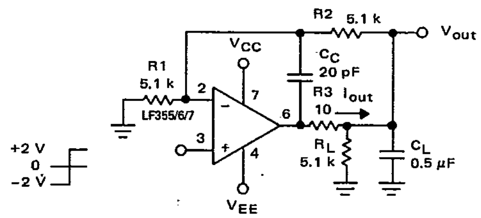
TYPICAL APPLICATIONS

FIGURE 37 — WIDE BW, LOW NOISE, LOW DRIFT AMPLIFIER



- Power BW: $f_{max} = \frac{S_r}{2\pi V_p} \cong 240\ kHz$
- Parasitic input capacitance ($C1 \approx 3$ pF for LF355, LF356, and LF357 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: $R2C2 \cong R1C1$.

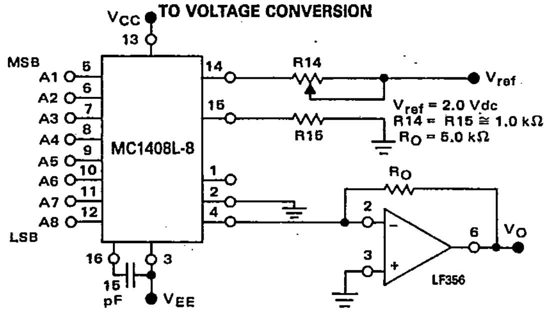
FIGURE 38 — ISOLATING LARGE CAPACITIVE LOADS



- Overshoot 6%
- $t_s = 10\ \mu s$
- When driving large C_L, the V_{out} slew rate is determined by C_L and $I_{out(max)}$:

$$\frac{\Delta V_{out}}{\Delta t} = \frac{I_{out}}{C_L} \cong \frac{0.02}{0.5}\ V/\mu s = 0.04\ V/\mu s \text{ (with } C_L \text{ shown)}$$

FIGURE 39 — 8-BIT D/A WITH OUTPUT CURRENT TO VOLTAGE CONVERSION



Theoretical V_O

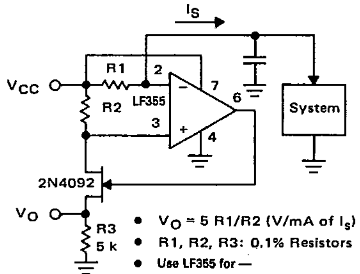
$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

Adjust V_{ref}, R14 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$$V_O = \frac{2V}{1k}(5\ k)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right]$$

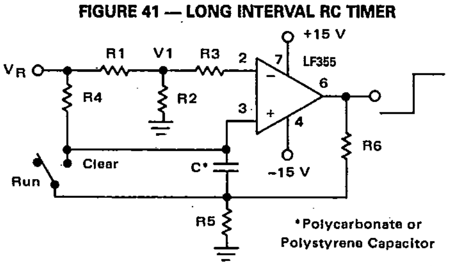
$$= 10\ V\left[\frac{255}{256}\right] = 9.961\ V$$

FIGURE 40 — PRECISION CURRENT MONITOR



- $V_O = 5\ R1/R2$ (V/mA of I_s)
- R1, R2, R3: 0.1% Resistors
- Use LF355 for —
  - ▲ Common-Mode Range to Supply Range
  - ▲ Low I_{IB}
  - ▲ Low V_{IO}
  - ▲ Low Supply Current

FIGURE 41 — LONG INTERVAL RC TIMER

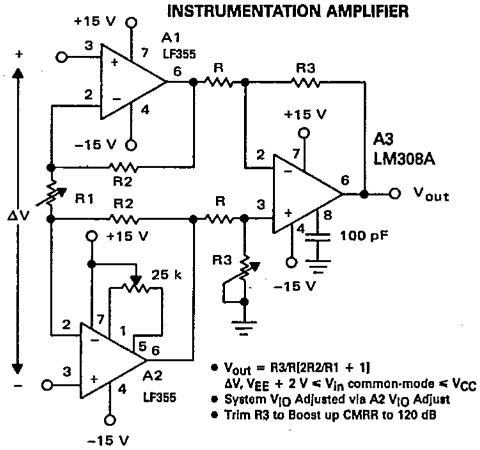


Time (t) = $R4C\ln(V_R/V_R - V_I)$, $R_3 = R_4$, $R_5 = 0.1\ R6$
If R1 = R2: t = 0.693 R4C

Design Example: 100 Second Timer

V_R = 10 V	C = 1 µF	R3 = R4 = 144 M
R6 = 20 k	R5 = 2 k	R1 = R2 = 1 k

FIGURE 42 — HIGH IMPEDANCE, LOW DRIFT INSTRUMENTATION AMPLIFIER



- $V_{out} = R3/R[2R2/R1 + 1]$
  ΔV, $V_{EE} + 2\ V \leq V_{in}$ common-mode $\leq V_{CC}$
- System V_{IO} Adjusted via A2 V_{IO} Adjust
- Trim R3 to Boost up CMRR to 120 dB