



MT5C1008 883C

# MILITARY SRAM

# 128K x 8 SRAM

T-46-23-14

## FEATURES

- High speed: 25, 30, 35, 45, and 55ns.
- Automatic chip enable power down
- All inputs and outputs are TTL compatible
- High performance, low power, CMOS process
- Single +5V ( $\pm 10\%$ ) power supply
- Low power, ICC (max.) 70mA
- MIL-STD-883 Rev. C, Class B
- RAD tolerant (consult factory)

## OPTIONS

- Timing
  - 25ns access
  - 30ns access
  - 35ns access
  - 45ns access
  - 55ns access

## MARKING

- Packages
  - Ceramic DIP
  - Ceramic LCC

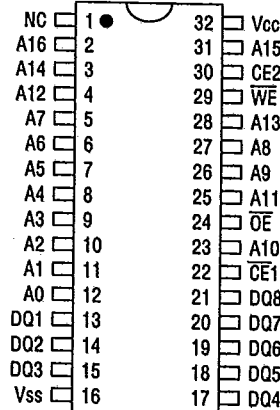
C  
EC

- Two Volt Data Retention

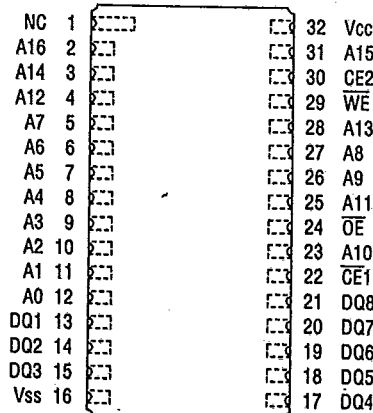
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## PIN ASSIGNMENT (Top View)

### 32L/400/600 DIP



### 32L/LCC



FAST SRAM

## GENERAL DESCRIPTION

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology. All fabrication is 100% domestic.

For flexibility in high speed memory applications, Micron offers chip enable ( $\overline{CE}$ ) on all organizations. Output enable ( $\overline{OE}$ ) is an enhancement available and can place the output in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ( $\overline{WE}$ ) and  $\overline{CE}$  inputs are both LOW. Reading is accomplished when  $\overline{WE}$  remains HIGH and  $\overline{CE}$  goes to LOW.  $\overline{OE}$  must also be LOW to read the device. The devices offer a reduced power standby mode when disabled. This allows system designs for low power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.