7-52-31

54AC16953, 54ACT16953 74AC16953, 74ACT16953

16-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0238-- D3561, JUNE 1990

- Members of Texas Instruments Widebus™ Family
- Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Centerto-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Lavout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance implanted CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'AC16953 and 'ACT16953 are inverting 16-bit registered bus transceivers composed of two 8-bit transceiver sections with separate control signals.

Data flow in the A-to-B mode is controlled by output-enable (1OEAB and 2OEAB), clock-enable (1CEAB and 2CEAB), and clock (1CLKAB and 2CLKAB) inputs. When 1CEAB (or 2CEAB) is high, data storage is inhibited and the registers retain their previous states. When 1CEAB (or 2CEAB) is low, the inverse of the data present at the corresponding A inputs is stored in the device on a low-to-high transition of 1CLKAB (or 2CLKAB). If 1OEAB (or 2OEAB) is also low, this stored data appears on the corresponding B outputs; if 10EAB (or 20EAB) is high, the corresponding B outputs are in the high-impedance state. 10EAB (or 20EAB) does not affect the operation of the Internal registers. Previously stored data can be retained or new data can be entered while the outputs are in the highimpedance state.

Data flow from B to A is controlled by 10EBA and 2OEBA, 1CEBA and 2CEBA, and 1CLKBA and 2CLKBA in a manner analogous to that described above for A-to-B data flow.

54AC16953, 54ACT16953 ... WD PACKAGE 74AC16953, 74ACT16953 ... DL PACKAGE (TOP VIEW)

10EAB	Г	U ₅₆	L	1 QEBA
1CLKAB	2	55	L	1 CLKBA
1CEAB	3	54		1 CEBA
GND [4	53		GND
1A1[5	52		1B1
1A2 [51		1B2
V _{CC} [7	50	П	Vcc
1Å3 [8	49		1B3
1A4 <u>[</u>		48	P	1B4
1A5 [1		_	1B5
GND [3	46	-	GND
1A6 [1			1B6
1A7 [1	44	_	187
1A8 [3	43		1B8
2A1	1			281
2A2 [ᆮ	2B2
2A3 [_	2B3
GND _				GND
2A4 [284
2A5 [•		Н	2B5
2A6 [•	36	Ц	286
V _{CC} [Ц	V _{CC}
2A7 [23		Ц	2B7
2A8 [H	
GND [닏	GND
2CEAB		- 1	Ш	2CEBA
2CLKAB	27	30	_	
20EAB	28	29	μ	20EBA

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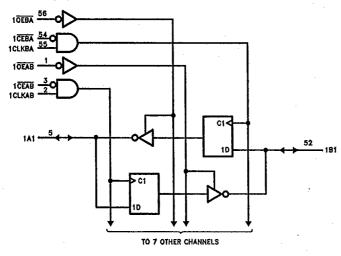
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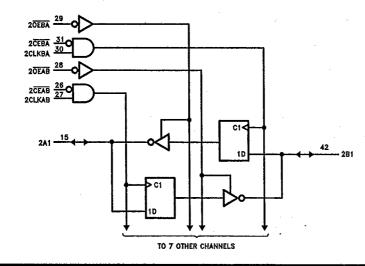
The 74AC16953 and 74ACT16953 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16953 has CMOS-compatible input thresholds. The 'ACT16953 has TTL-compatible input thresholds.

The 54AC16953 and 54ACT16953 are characterized over the full military temperature range of -55° C to 125°C. The 74AC16953 and 74ACT16953 are characterized for operation from -40° C to 85°C.

logic diagram (positive logic)





TEXAS INSTRUMENTS

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