National Semiconductor

PRELIMINARY

74VHC175
Quad D Flip-Flop

General Description

The VHC175 is an advanced high-speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The VHC175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

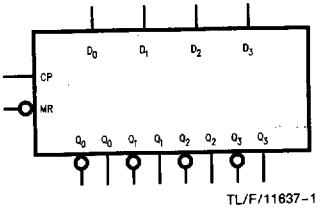
- Low power dissipation: $I_{CC} = 4\ \mu A$ (max) at $T_A = 25°C$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\%\ V_{CC}$ (min)
- All inputs are equipped with a power down protection function
- Balanced propagation delays: $t_{PLH} \cong t_{PHL}$
- Low noise: $V_{OLP} = 0.8V$ (max)
- Pin and function compatible with 74HC175

Ordering Code: See Section 6

Commercial	Package Number	Package Description
74VHC175M	M16A	16-Lead Molded JEDEC SOIC
74VHC175SJ	M16D	16-Lead Molded EIAJ SOIC
74VHC175MTC	MTC16	16-Lead Molded JEDEC Type 1 TSSOP
74VHC175N	N16E	16-Lead Molded DIP

Note: Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



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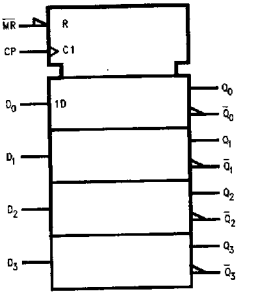
Pin Names	Description
D_0–D_3	Data Inputs
CP	Clock Pulse Input
$\overline{MR}$	Master Reset Input
Q_0–Q_3	True Outputs
$\overline{Q}_0$–$\overline{Q}_3$	Complement Outputs

IEEE/IEC



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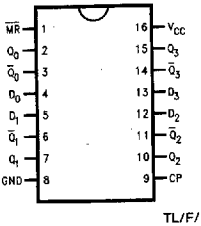
Connection Diagram

Pin Assignment for DIP, TSSOP and SOIC



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Functional Description

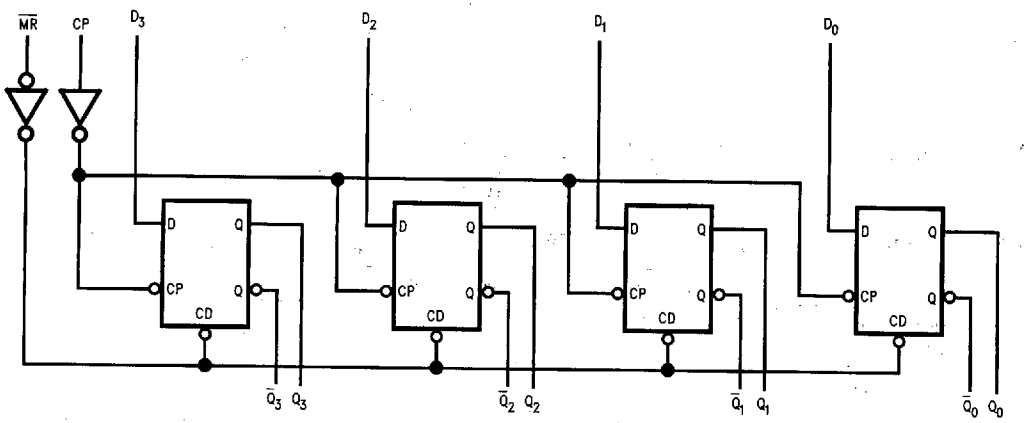
The VHC175 consists of four edge-triggered D flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs. The VHC175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

Truth Table

Inputs	Outputs	
@ t_n, $\overline{MR}$ = H	@ t_{n+1}	
D_n	Q_n	$\overline{Q}_n$
L	L	H
H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit Time before Clock Pulse
t_{n+1} = Bit Time after Clock Pulse

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Note 1: *Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation outside databook specifications.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to +5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ±0.3V	0 ~ 100 ns/V
V_{CC} = 5.0V ±0.5V	0 ~ 20 ns/V

DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V_{CC} (V)	74VHC					Units	Conditions	
			T_A = 25°C			T_A = −40°C to +85°C				
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0–5.5	1.50 0.7 V_{CC}			1.50 0.7 V_{CC}		V		
V_{IL}	Low Level Input Voltage	2.0 3.0–5.5			0.50 0.3 V_{CC}		0.50 0.3 V_{CC}	V		
V_{OH}	High Level Output Voltage	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA
		3.0 4.5	2.58 3.94			2.48 3.80		V		I_{OH} = −4 mA I_{OH} = −8 mA
V_{OL}	Low Level Output Voltage	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA
		3.0 4.5			0.36 0.36		0.44 0.44	V		I_{OL} = 4 mA I_{OL} = 8 mA
I_{IN}	Input Leakage Current	0–5.5			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

DC Characteristics for 'VHC Family Devices: See Section 2 for Waveforms (Continued)

Symbol	Parameter	V_{CC} (V)	74VHC $T_A = 25°C$ Typ	74VHC $T_A = 25°C$ Limits	Units	Conditions	Fig. No.
V_{OLP}*	Quiet Output Maximum Dynamic V_{OL}	5.0	0.4	0.8	V	C_L = 50 pF	2-11, 12
V_{OLV}*	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.4	−0.8	V	C_L = 50 pF	2-11, 12
V_{IHD}*	Minimum High Level Dynamic Input Voltage	5.0		3.5	V	C_L = 50 pF	2-11, 12
V_{ILD}*	Maximum Low Level Dynamic Input Voltage	5.0		1.5	V	C_L = 50 pF	2-11, 12

*Parameter guaranteed by design.

AC Electrical Characteristics for VHC: See Section 2 for Waveforms

Symbol	Parameter	V_{CC} (V)	74VHC $T_A = 25°C$ Min	Typ	Max	74VHC $T_A = -40°C$ to $+85°C$ Min	Max	Units	Conditions	Fig. No.
f_{MAX}	Maximum Clock Frequency	3.3 ± 0.3	90	140		75		MHz	C_L = 15 pF	
			50	75		45			C_L = 50 pF	
		5.0 ± 0.5	150	210		125		MHz	C_L = 15 pF	
			85	115		75			C_L = 50 pF	
t_{PLH}, t_{PHL}	Propagation Delay Time (CP to Q_n or $\overline{Q}_n$)	3.3 ± 0.3		7.5	11.5	1.0	13.5	ns	C_L = 15 pF	2-5, 6
				10.0	15.0	1.0	17.0		C_L = 50 pF	2-5, 6
		5.0 ± 0.5		4.8	7.3	1.0	8.5	ns	C_L = 15 pF	2-5, 6
				6.3	9.3	1.0	10.5		C_L = 50 pF	2-5, 6
t_{PLH}, t_{PHL}	Propagation Delay Time ($\overline{MR}$ to Q_n or $\overline{Q}_n$)	3.3 ± 0.3		6.3	10.1	1.0	12.0	ns	C_L = 15 pF	2-5, 6
				8.8	13.6	1.0	15.5		C_L = 50 pF	2-5, 6
		5.0 ± 0.5		4.3	6.4	1.0	7.5	ns	C_L = 15 pF	2-5, 6
				5.8	8.4	1.0	9.5		C_L = 50 pF	2-5, 6
t_{OSLH}, t_{OSHL}	Output to Output Skew	3.3 ± 0.3			1.5		1.5		C_L = 50 pF (Note 1)	
		5.0 ± 0.5			1.0		1.0		C_L = 50 pF (Note 1)	
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open	
C_{PD}	Power Dissipation Capacitance			44				pF	(Note 2)	

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLH_{max}} - t_{PLH_{min}}|$; $t_{OSHL} = |t_{PHL_{max}} - t_{PHL_{min}}|$.

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation: I_{CC} (opr.) = $C_{PD} * V_{CC} * f_{IN} + I_{CC}/4$ (per F/F), and the total C_{PD} when n pcs of the Flip Flop operate can be calculated by the following equation: C_{PD} (total) = 30 + 14 • n

AC Operating Requirements for VHC: See Section 2 for Waveforms

Symbol	Parameter	*V_{CC} (V)	74VHC $T_A = 25°C$	74VHC $T_A = -40°C$ to $+85°C$	Units	Conditions	Fig. No.
			Typ	Guaranteed Minimum			
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CP)	3.3 5.0		5.0 5.0	5.0 5.0	ns		2-6
$t_{W(L)}$	Minimum Pulse Width ($\overline{MR}$)	3.3 5.0		5.0 5.0	5.0 5.0	ns		2-6
t_S	Minimum Setup Time (Dn to CP)	3.3 5.0		5.0 4.0	5.0 4.0	ns		2-9
t_H	Minimum Hold Time (Dn to CP)	3.3 5.0		1.0 1.0	1.0 1.0	ns		2-9
t_{rem}	Minimum Removal Time ($\overline{MR}$)	3.3 5.0		5.0 5.0	5.0 5.0	ns		2-6, 9

*V_{CC} is 3.3 ±0.3V or 5.0 ±0.5V