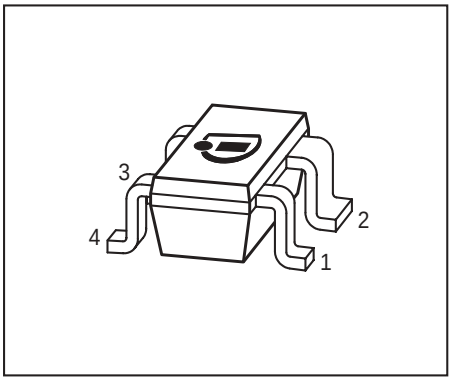
Silicon N_Channel MOSFET Tetrode



- Short-channel transistor with high S / C quality factor
- For low-noise, gain-controlled input stage up to 1 GHz
- Pb-free (RoHS compliant) package[1)]
- Qualified according AEC Q101

AEC Qualified RoHS

ESD (**E**lectro**s**tatic **d**ischarge) sensitive device, observe handling precaution!

Type	Package	Pin Configuration						Marking
ST194E6716	SOT143R	1=D	2=S	3=G1	4=G2	-	-	MRs

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	13	V
Continuous drain current	I_D	30	mA
Gate 1/ gate 2-source current	$\pm I_{G1/2SM}$	10	
Total power dissipation $T_S \leq 76°C$	P_{tot}	200	
Storage temperature	T_{stg}	-55 ... 150	°C
Channel temperature	T_{ch}	150	

Thermal Resistance

Parameter	Symbol	Value	Unit
Channel - soldering point[2)]	R_{thchs}	≤370	K/W

[1]Pb-containing package may be available upon special request

[2]For calculation of R_{thJA} please refer to Application Note Thermal Resistance

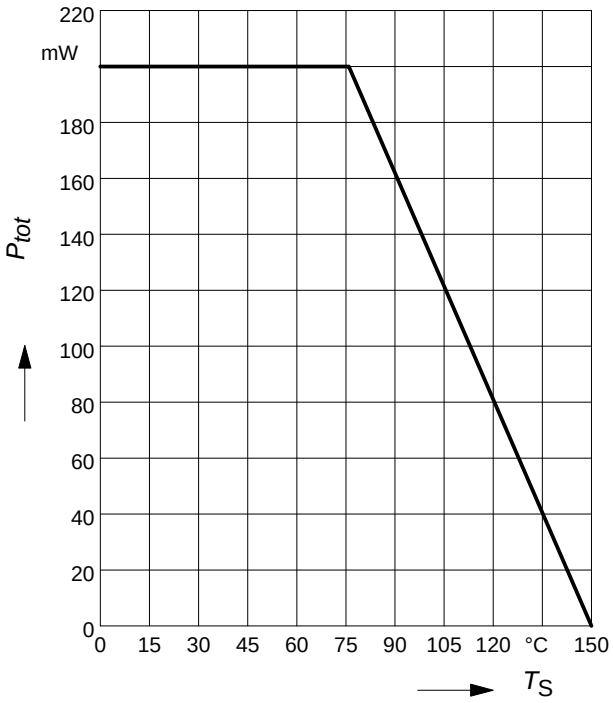
Electrical Characteristics at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Drain-source breakdown voltage I_D = 10 µA, V_{G1S} = -4 V, V_{G2S} = -4 V	$V_{(BR)DS}$	13	-	-	V
Gate 1 source breakdown voltage $\pm I_{G2S}$ = 10 mA, V_{G2S}=V_{DS}=0	$\pm V_{(BR)G1SS}$	8	-	14	
Gate2 source breakdown voltage $\pm I_{G2S}$ = 10 mA, V_{G2S}=V_{DS}=0	$\pm V_{(BR)G2SS}$	8	-	14	
Gate 1 source leakage current $\pm V_{G1S}$ = 5 V, V_{G2S}=V_{DS}=0	$\pm I_{G1SS}$	-	-	100	nA
Gate 2 source leakage current $\pm V_{G2S}$ = 5 V, V_{G2S}=V_{DS}=0	$\pm I_{G2SS}$	-	-	100	nA
Drain current V_{DS} = 8 V, V_{G1S} = 0 , V_{G2S} = 4 V	I_{DSS}	2	-	18	mA
Gate 1 source pinch-off voltage V_{DS} = 8 V, V_{G2S} = 4 V, I_D = 20 µA	$-V_{G1S(p)}$	-	0.8	2.5	V
Gate 2 source pinch-off voltage V_{DS} = 8 V, V_{G1S} = 0 , I_D = 20 µA	$-V_{G2S(p)}$	-	0.8	2	

Electrical Characteristics at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
AC Characteristics - (verified by random sampling)					
Forward transconductance V_{DS} = 8 V, I_D = 10 mA, V_{G2S} = 4 V	g_{fs}	20	24	28	-
Gate1 input capacitance V_{DS} = 8 V, I_D = 10 mA, V_{G2S} = 4 V, f = 10 MHz	C_{g1ss}	1.8	2.1	2.5	pF
Gate 2 input capacitance V_{DS} = 8 V, I_D = 10 mA, V_{G2S} = 4 V, f = 10 MHz	C_{g2ss}	-	1.2	-	pF
Feedback capacitance V_{DS} = 8 V, I_D = 10 mA, V_{G2S} = 4 V, f = 10 MHz	C_{dg1}	-	25	-	fF
Output capacitance V_{DS} = 8 V, I_D = 10 mA, V_{G2S} = 4 V, f = 10 MHz	C_{dss}	-	1.05	-	pF
Power gain (self biased) V_{DS} = 8 V, I_D = 10 mA, V_{G2S} = 4 V, f = 45 MHz V_{DS} = 8 V, I_D = 10 mA, V_{G2S} = 4 V, f = 800	G_p	 - -	 28 20	 - -	dB
Noise figure V_{DS} = 8 V, I_D = 10 mA, V_{G2S} = 4 V, f = 45 MHz V_{DS} = 8 V, I_D = 10 mA, V_{G2S} = 4 V, f = 800 MHz	F	 - -	 1.9 1.5	 - -	dB
Gain control range V_{DS} = 8 V, V_{G2S} = 4...-2 , f = 800 MHz	ΔG_p	40	50	-	

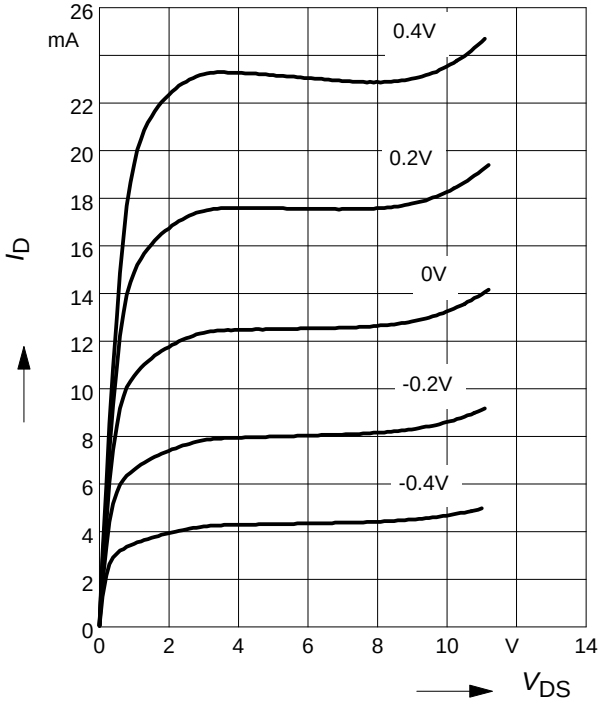
Total power dissipation $P_{tot} = f(T_S)$



Output characteristics $I_D = f(V_{DS})$

V_{G2S} = 4 V

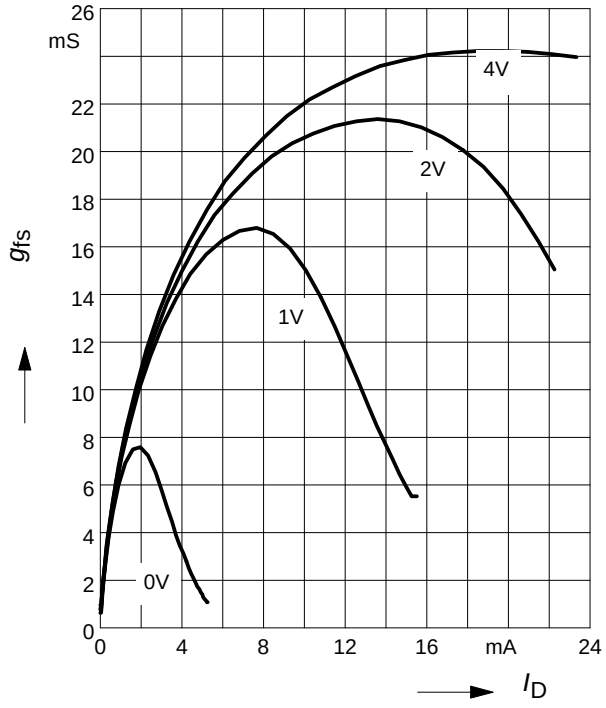
V_{G1S} = Parameter



Gate 1 forward transconductance

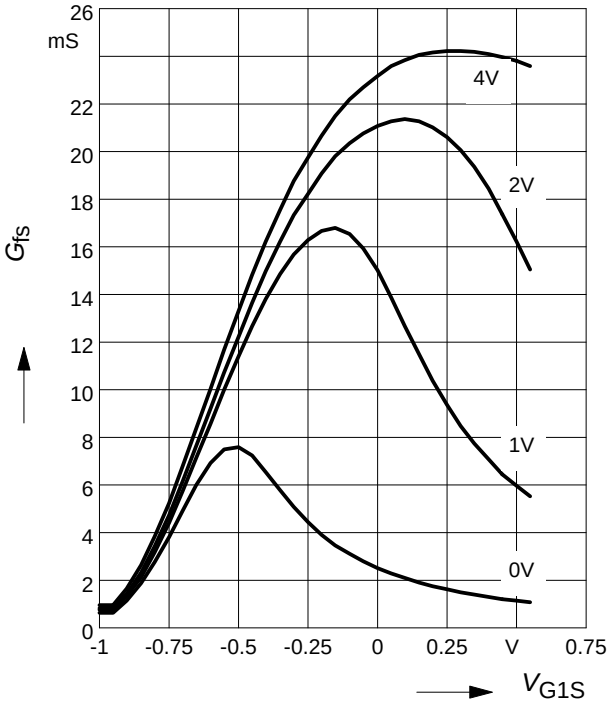
$g_{fs} = f(I_D)$

V_{DS} = 5V, V_{G2S} = Parameter



Gate 1 forward transconductance

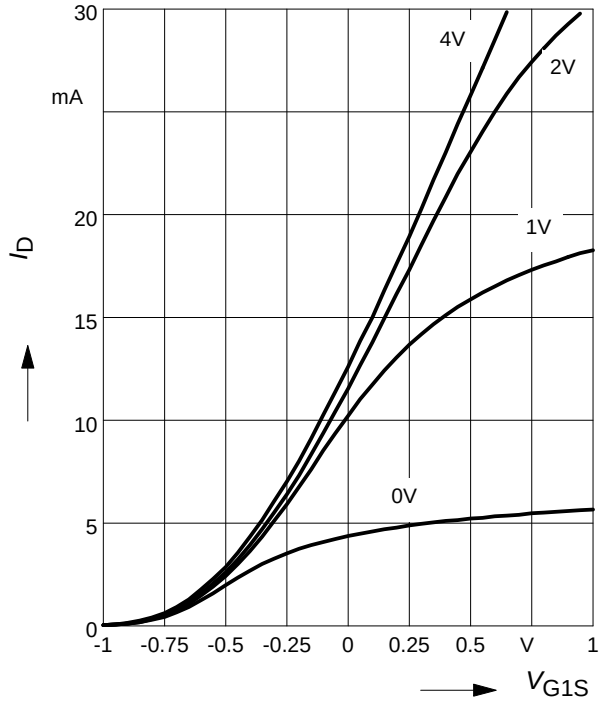
$g_{fs1} = f(V_{G1S})$



Drain current $I_D = f(V_{G1S})$

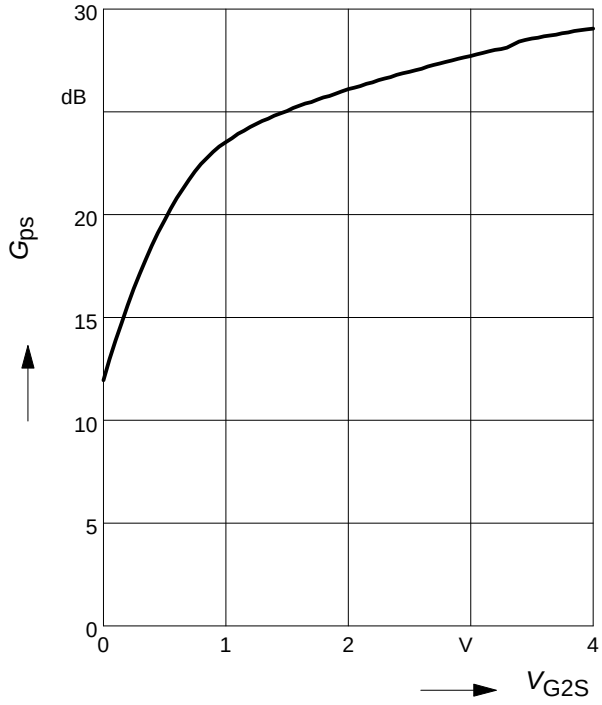
V_{DS} = 5V

V_{G2S} = Parameter



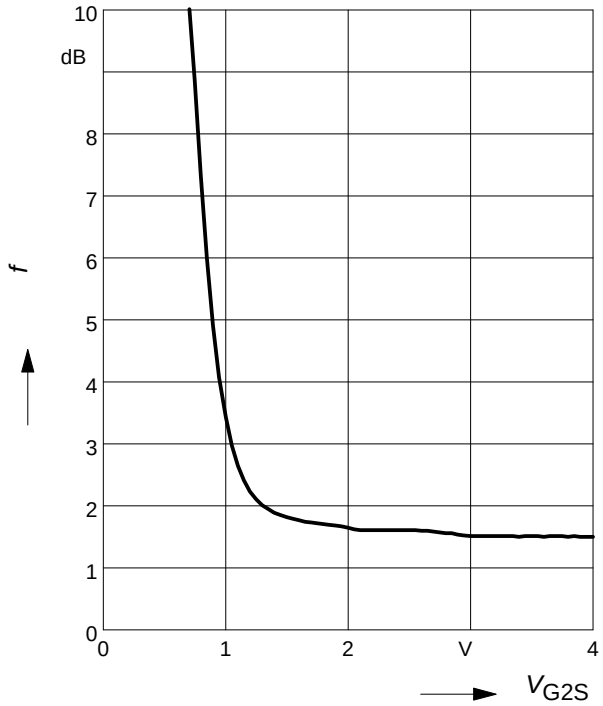
Power gain $G_{ps} = f(V_{G2S})$

f = 45 MHz



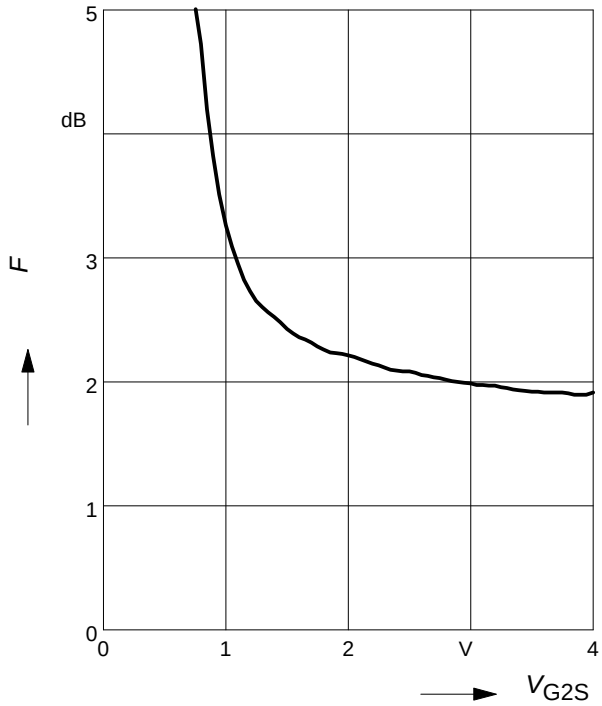
Noise figure $F = f(V_{G2S})$

f=45 MHz

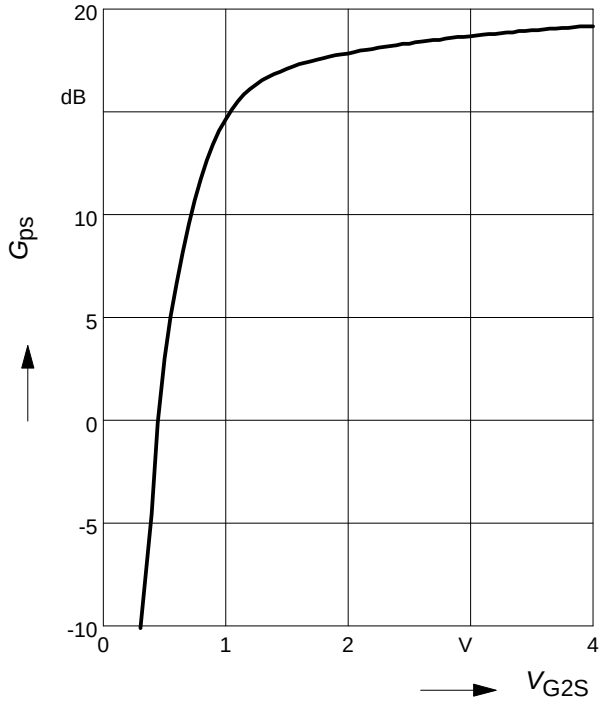


Noise figure $F = f(V_{G2S})$

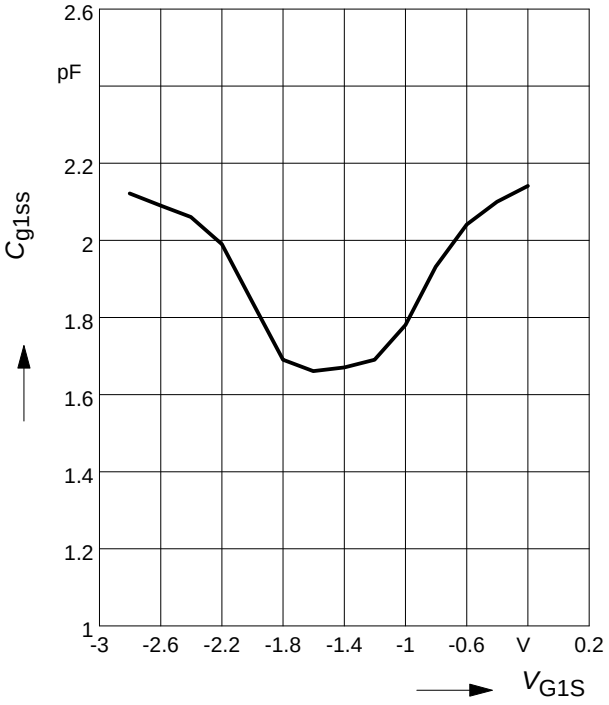
f=800 MHz



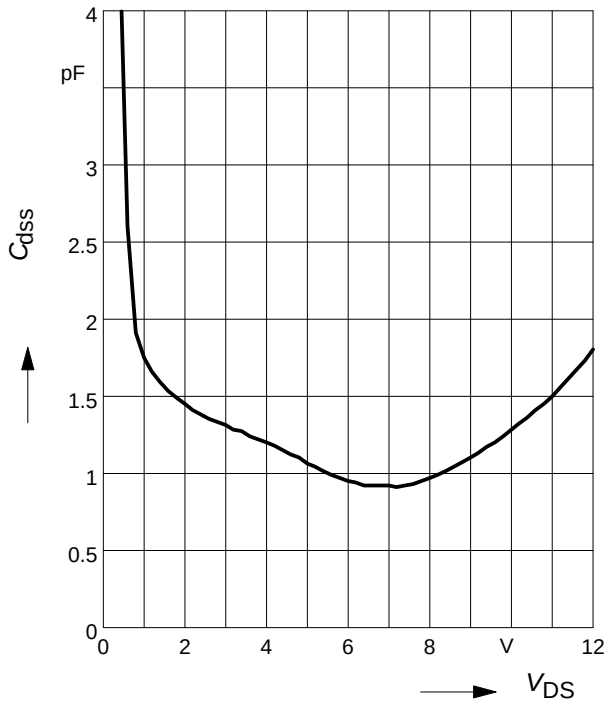
Power gain $G_{ps} = f\ (V_{G2S})$
f = 800 MHz



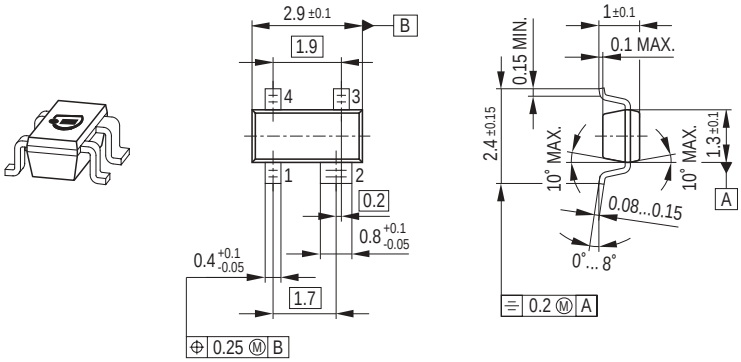
Gate 1 input capacitance $C_{g1ss} = f\ (V_{G1S})$



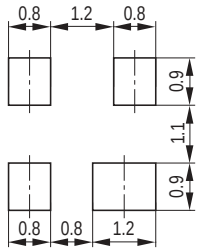
Output capacitance $C_{dss} = f(V_{DS})$



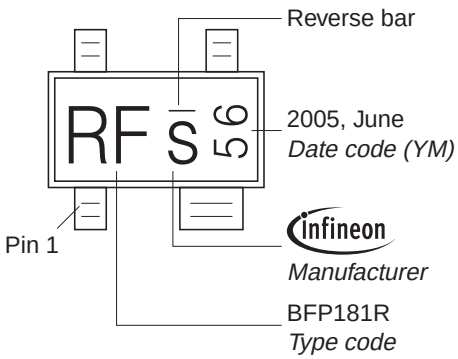
Package Outline



Foot Print

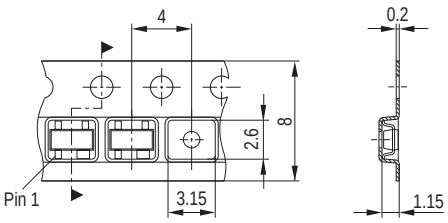


Marking Layout (Example)



Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel
Reel ø330 mm = 10.000 Pieces/Reel



Edition 2006-02-01
Published by
Infineon Technologies AG
81726 München, Germany

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