

DATA SHEET

74AC02/74ACT02 Quad 2-input NOR gate

Product specification

1997 Aug 22

Quad 2-input NOR gate

74AC02 74ACT02

FEATURES

- 74ACT02 has TTL-compatible inputs
- 74AC02 has CMOS-compatible inputs
- Meets or exceeds JEDEC standard standard for 74AC(T)XX family
- Superior ground bounce noise immunity
- Output source/sink 24mA

DESCRIPTION

The 74AC02/74ACT02 provides the 2-input NOR function.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYPICAL			UNIT
			AC		ACT	
			V _{CC} = 3.3V	V _{CC} = 5.0V	V _{CC} = 5.0V	
t _{PHL} /t _{PLH}	Propagation delay nA, nB to nY	C _L = 50pF	3.8	2.8	3.8	ns
C _I	Input capacitance		4.5			pF
C _{PD}	Power dissipation capacitance per gate	V _I = GND to V _{CC} ¹	30		30	pF

NOTE:

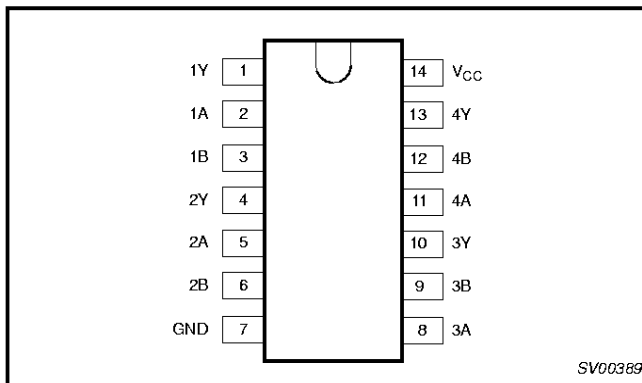
1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING AND PACKAGE INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DRAWING NUMBER
14-Pin Plastic SO	-40°C to +85°C	74AC02D 74ACT02D	74AC02D 74ACT02D	SOT108-1
14-Pin Plastic SSOP Type II	-40°C to +85°C	74AC02DB 74ACT02DB	74AC02DB 74ACT02DB	SOT337-1
14-Pin Plastic TSSOP Type I	-40°C to +85°C	74AC02PW 74ACT02PW	74AC02PW DH 74ACT02PW DH	SOT402-1

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1Y to 4Y	Data outputs
2, 5, 8, 11	1A to 4A	Data inputs
3, 6, 9, 12	1B to 4B	
7	GND	Ground (0 V)
14	V _{CC}	Positive supply voltage

Quad 2-input NOR gate

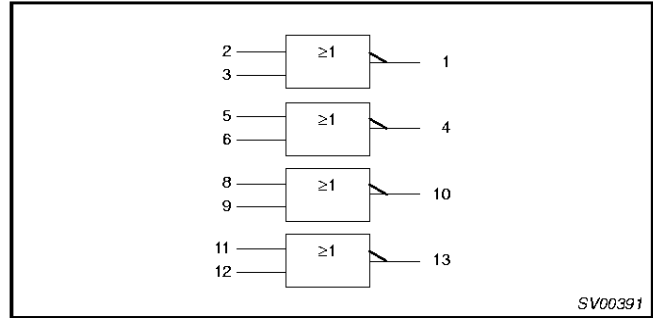
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FUNCTION TABLE

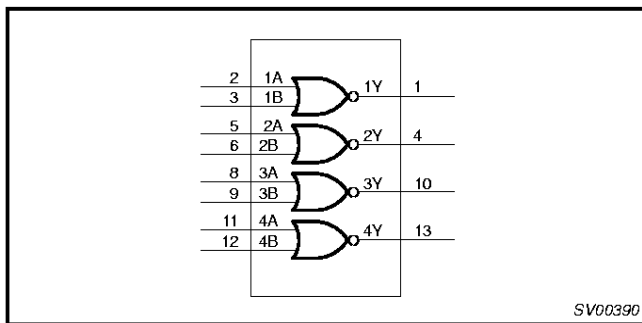
INPUTS		OUTPUT
nOE	nA	nY
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH voltage level
L = LOW voltage level

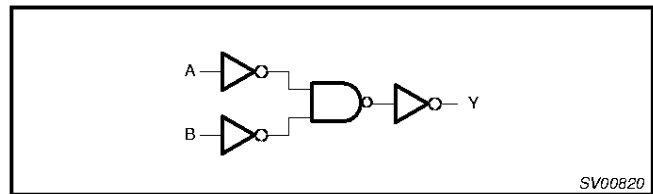
LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V _{CC}	DC supply voltage for 'AC	2.0	6.0	V
V _{CC}	DC supply voltage for 'ACT	4.5	5.5	V
V _{IN}	DC input voltage range	0	V _{CC}	V
V _O	DC output voltage range	0	V _{CC}	V
T _{amb}	Operating free-air temperature range	-40	+85	°C
ΔV/Δt	Minimum input edge rate — AC devices V _{IN} from 30% to 70% of V _{CC} V _{CC} @ 3.3V, 4.5V, 5.5V	125		mV/ns
	— ACT devices V _{IN} from 0.8V to 2.0V V _{CC} @ 4.5V, 5.5V	125		

Quad 2-input NOR gate

74AC02
74ACT02**ABSOLUTE MAXIMUM RATINGS¹**

in accordance with the Absolute Maximum Rating System (IEC134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_{IN} = -0.5V$	-20	mA
		$V_{IN} = V_{CC} + 0.5V$	+20	
V_{IN}	DC input voltage		-0.5 to $V_{CC} + 0.5$	V
I_{OK}	DC output diode current	$V_O = -0.5V$	-20	mA
		$V_O = V_{CC} + 0.5V$	+20	
V_O	DC output voltage		-0.5 to $V_{CC} + 0.5$	V
I_O	DC output source or sink current		± 50	mA
I_{CC}, I_{GND}	DC V_{CC} or GND current per output		± 50	mA
I_{CC}, I_{GND}	DC V_{CC} or GND current		± 200	mA
T_{stg}	Storage temperature range		-65 to +150	°C
P_{TOT}	Power dissipation per package - plastic mini-pack (SO) - plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K	500	mW
		above +60°C derate linearly with 5.5 mW/K	500	

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Quad 2-input NOR gate

74AC02
74ACT02**DC CHARACTERISTICS FOR THE AC FAMILY**

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	V _{CC} (V)	LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP	MAX	
V _{IH}	HIGH level Input voltage	V _{OUT} = 0.1V or (V _{CC} - 0.1V)	3.0	2.1	1.5		V
			4.5	3.15	2.25		
			5.5	3.85	2.75		
V _{IL}	LOW level Input voltage	V _{OUT} = 0.1V or (V _{CC} - 0.1V)	3.0		1.5	0.9	V
			4.5		2.25	1.35	
			5.5		2.75	1.65	
V _{OH}	HIGH level output voltage	I _{OUT} = -50 μA	3.0	2.9	2.99		V
			4.5	4.4	4.49		
			5.5	5.4	5.49		
		V _{IN} = V _{IL} or V _{IH} , I _{OH} = -12mA ¹	3.0	2.46			
		V _{IN} = V _{IL} or V _{IH} , I _{OH} = -24mA ¹	4.5	3.76			
V _{IN} = V _{IL} or V _{IH} , I _{OH} = -24mA ¹	5.5	4.76					
V _{OL}	LOW level output voltage	I _{OUT} = 50 μA	3.0		0.01	0.1	V
			4.5		0.01	0.1	
			5.5		0.01	0.1	
		V _{IN} = V _{IL} or V _{IH} , I _{OL} = 12mA ¹	3.0			0.44	
		V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA ¹	4.5			0.44	
V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA ¹	5.5			0.44			
I _{IN}	Input leakage current	V _{IN} = V _{CC} , GND	5.5			± 1.0	μA
I _{OLD}	Dynamic output current ²	V _{OLD} = 1.65V max	5.5	75			mA
I _{OHD}	Dynamic output current ²	V _{OHD} = 3.85V min	5.5			-75	mA
I _{CC}	Quiescent supply current	V _{IN} = V _{CC} or GND	5.5			40	μA

NOTES:

- All outputs loaded
- Maximum test duration 2.0 ms; one output loaded at a time

Quad 2-input NOR gate

74AC02
74ACT02

DC CHARACTERISTICS FOR THE ACT FAMILY

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	V _{CC} (V)	LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP	MAX	
V _{IH}	HIGH level Input voltage	V _{OUT} = 0.1V or (V _{CC} - 0.1V)	4.5	2.0	1.5	V	
			5.5	2.0	1.5		
V _{IL}	LOW level Input voltage	V _{OUT} = 0.1V or (V _{CC} - 0.1V)	4.5		1.5	0.8	V
			5.5		1.5	0.8	
V _{OH}	HIGH level output voltage	I _{OUT} = -50 μA	4.5	4.4	4.49	V	
			5.5	5.4	5.49		
		V _{IN} = V _{IL} or V _{IH} , I _{OH} = -24mA ¹	4.5	3.76			
			5.5	4.76			
V _{OL}	LOW level output voltage	I _{OUT} = 50 μA	4.5		0.01	0.1	V
			5.5		0.01	0.1	
		V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA ¹	4.5			0.44	
			5.5			0.44	
I _{IN}	Input leakage current	V _{IN} = V _{CC} , GND	5.5			±1.0	μA
ΔI _{CC}	Additional quiescent supply current per input pin	V _{IN} = V _{CC} - 2.1V Other inputs at V _{CC} or GND; I _{OUT} = 0	5.5			1.5	mA
I _{OLD}	Dynamic output current ²	V _{OLD} = 1.65V max	5.5	75			mA
I _{OHD}	Dynamic output current ²	V _{OHD} = 3.85V min	5.5			-75	mA
I _{CC}	Quiescent supply current	V _{IN} = V _{CC} or GND	5.5			40	μA

NOTES:

- All outputs loaded
- Maximum test duration 2.0ms, one output loaded at a time

AC CHARACTERISTICS FOR 74AC02

GND = 0V; t_r = t_f ≤ 2.5ns; C_L = 50pF; R_L = 500Ω; .

SYMBOL	PARAMETER	V _{CC} ¹	LIMITS					UNIT	WAVEFORM
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C			
			MIN	TYP	MAX	MIN	MAX		
t _{PLH}	Propagation delay nA, nB to nY	3.3	2.0	4.0	7.0	1.5	8.0	ns	1, 2
		5.0	1.5	2.9	5.0	1.0	5.5		
t _{PHL}	Propagation delay nA, nB to nY	3.3	2.0	3.6	7.0	1.5	8.0	ns	1, 2
		5.0	1.5	2.8	5.0	1.0	5.5		

NOTE:

- Voltage range 3.3V is V_{CC} = 3.3V ± 0.3V
Voltage range 5.0V is V_{CC} = 5.0V ± 0.5V

AC CHARACTERISTICS FOR 74ACT02

GND = 0V; t_r = t_f ≤ 2.5ns; C_L = 50pF; R_L = 500Ω; .

SYMBOL	PARAMETER	V _{CC} ¹	LIMITS					UNIT	WAVEFORM
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C			
			MIN	TYP	MAX	MIN	MAX		
t _{PLH}	Propagation delay nA, nB to nY	5.0	2.0	3.6	8.0	1.5	9.0	ns	1, 2
t _{PHL}	Propagation delay nA, nB to nY	5.0	2.0	4.0	8.0	1.5	9.0	ns	

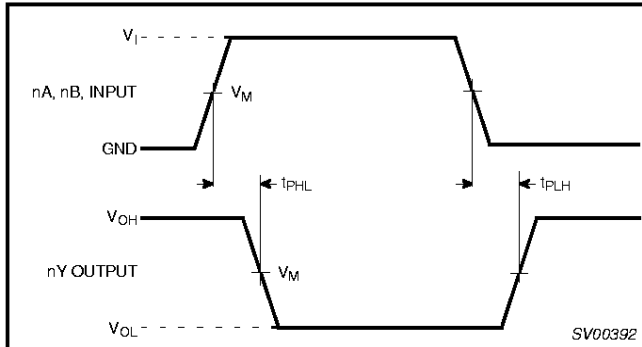
NOTE:

- Voltage range 5.0V is V_{CC} = 5.0V ± 0.5V

Quad 2-input NOR gate

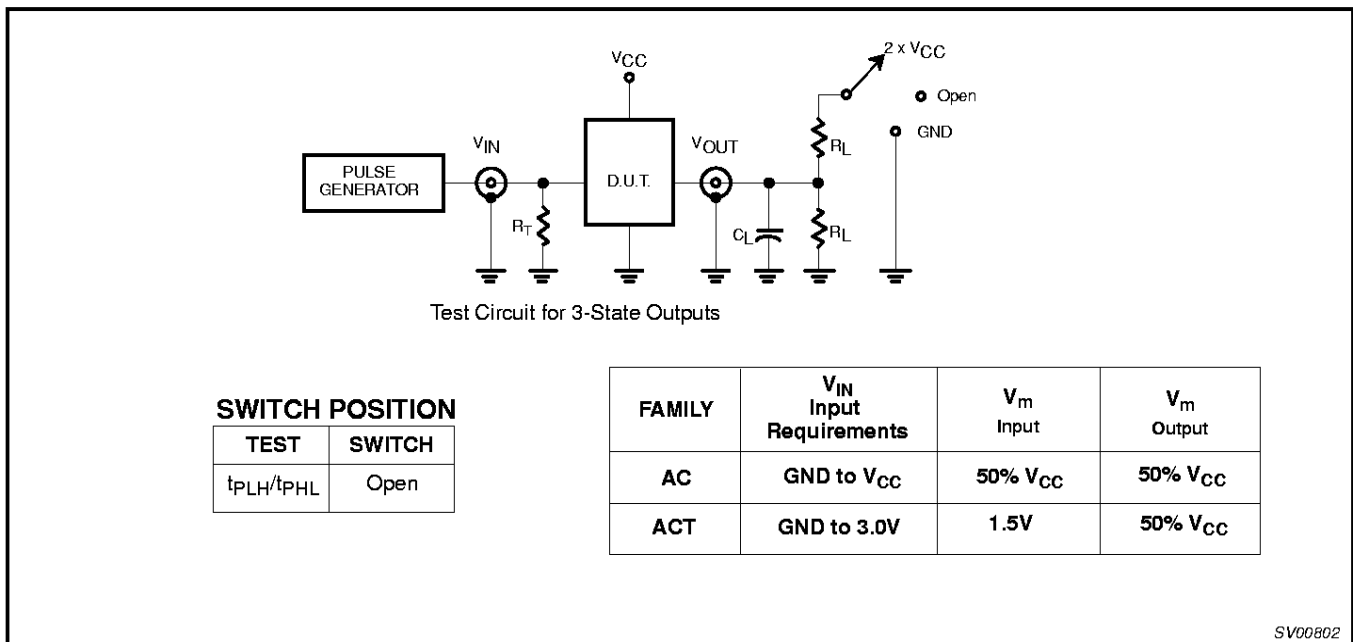
74AC02
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AC WAVEFORMS



Waveform 1. Inputs (nA, nB) to output (nY) propagation delays

TEST CIRCUIT



Waveform 2. Load circuitry for switching times.

DEFINITIONS

R_L = Load resistor; see AC Characteristics for value

C_L = Load capacitance; see AC Characteristics

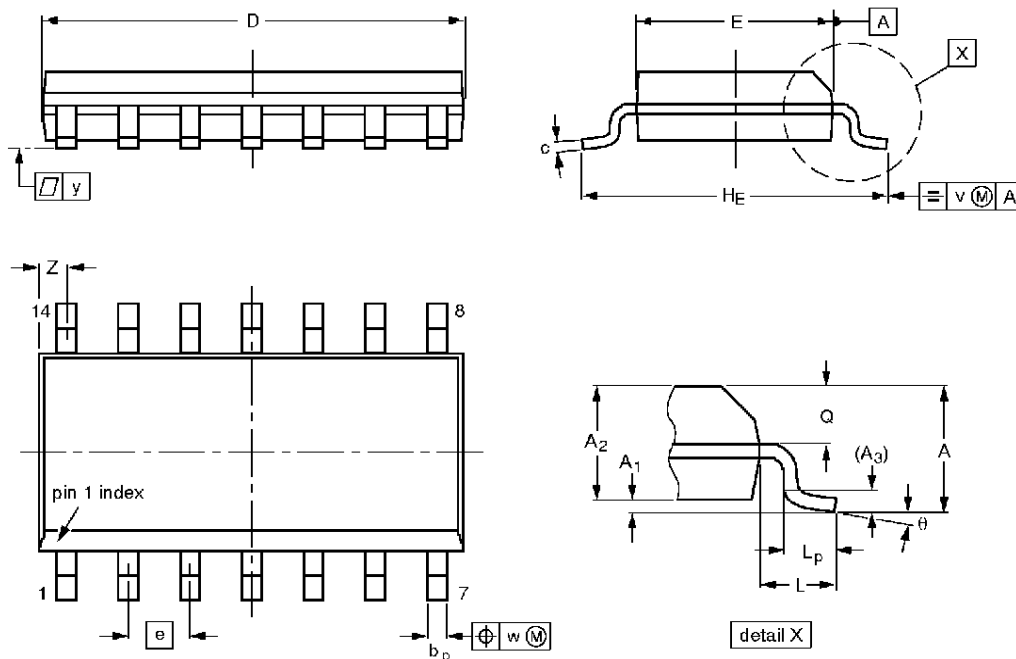
Termination resistance should be equal to Z_{OUT} of pulse generators

Quad 2-input NOR gate

74AC02
74ACT02

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	HE	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.35 0.34	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

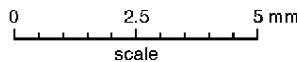
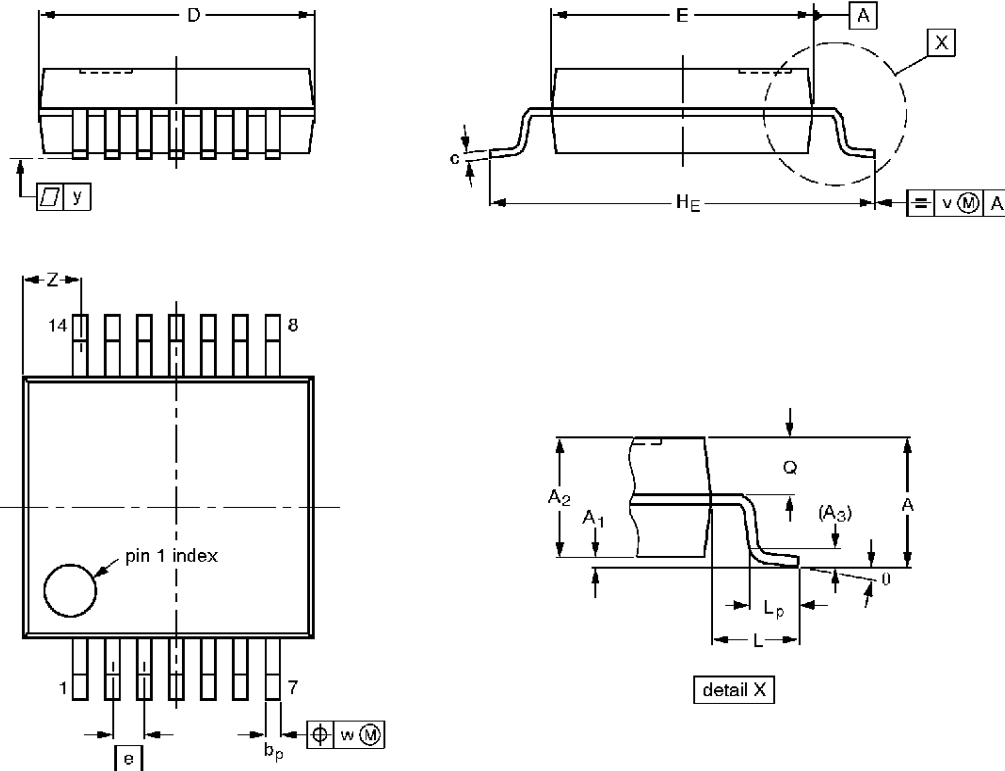
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				91-08-10 95-01-23

Quad 2-input NOR gate

74AC02
74ACT02

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

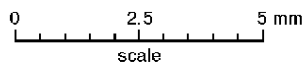
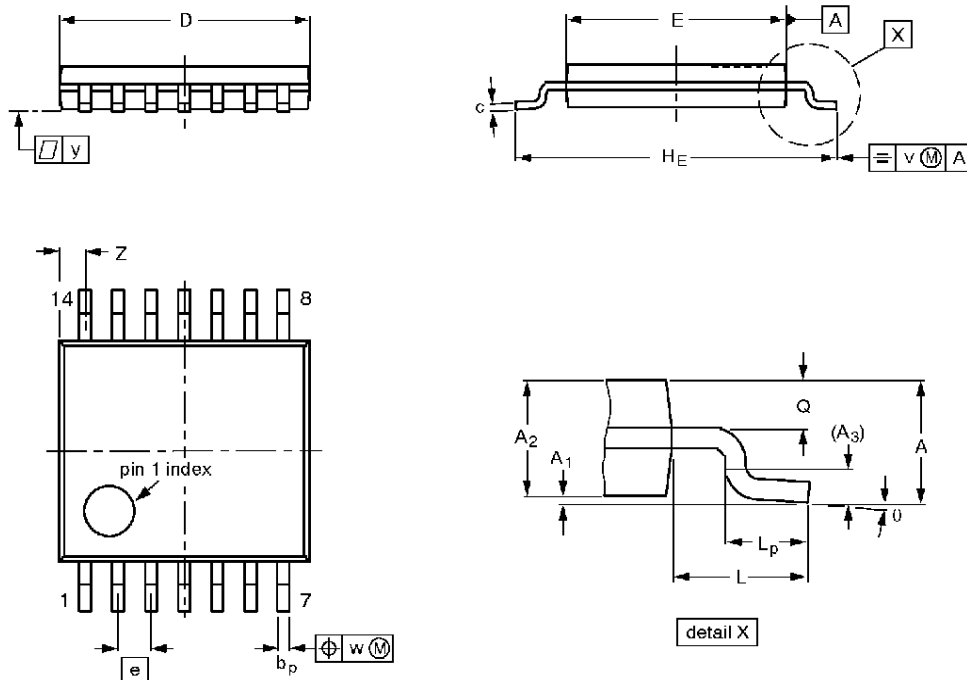
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT337-1		MO-150AB			95-02-04 96-01-18

Quad 2-input NOR gate

74AC02
74ACT02

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				94-07-12 95-04-04

Quad 2-input NOR gate

74AC02
74ACT02

NOTES

Quad 2-input NOR gate

74AC02
74ACT02

DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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