PRELIMINARY
Notice: This is not a final specification
Some parametric limits are subject to change

M5M5V1B008J-10,-12,-15

1048576-BIT (131072-WORD BY 8-BIT) BiCMOS STATIC RAM

DESCRIPTION

The M5M5V1B008 is a family of 131072-word by 8-bit static RAMs, fabricated with the high-performance BiCMOS process and designed for high-speed application. These devices operate on a single 3.3V supply, and are directly LVTTL (Low Voltage TTL) compatible. They include a power-down feature as well.

FEATURES

- Fast access time M5M5V1B008J-10 ····· 10ns(max)
  M5M5V1B008J-12 ····· 12ns(max)
  M5M5V1B008J-15 ····· 15ns(max)
- Low power dissipation Active····· 450mW(typ)
  Stand by····· 50mW(typ)
- Power down by $\overline{S}$
- Single 3.3V power supply
- Fully static operation
- Requires neither external clock nor refreshing
- All inputs and outputs are directly LVTTL compatible
- Easy memory expansion by chip-select ($\overline{S}$) input
- Output enable ($\overline{OE}$) prevents data contention in the I/O bus
- All address inputs are changeable with each other

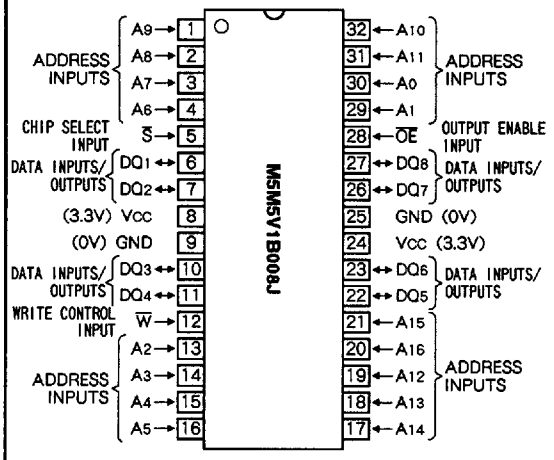
APPLICATION

High-speed memory systems

FUNCTION

A write operation is executed during the $\overline{S}$ low, and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the DQ terminal is maintained in the high impedance state.

PIN CONFIGURATION (TOP VIEW)



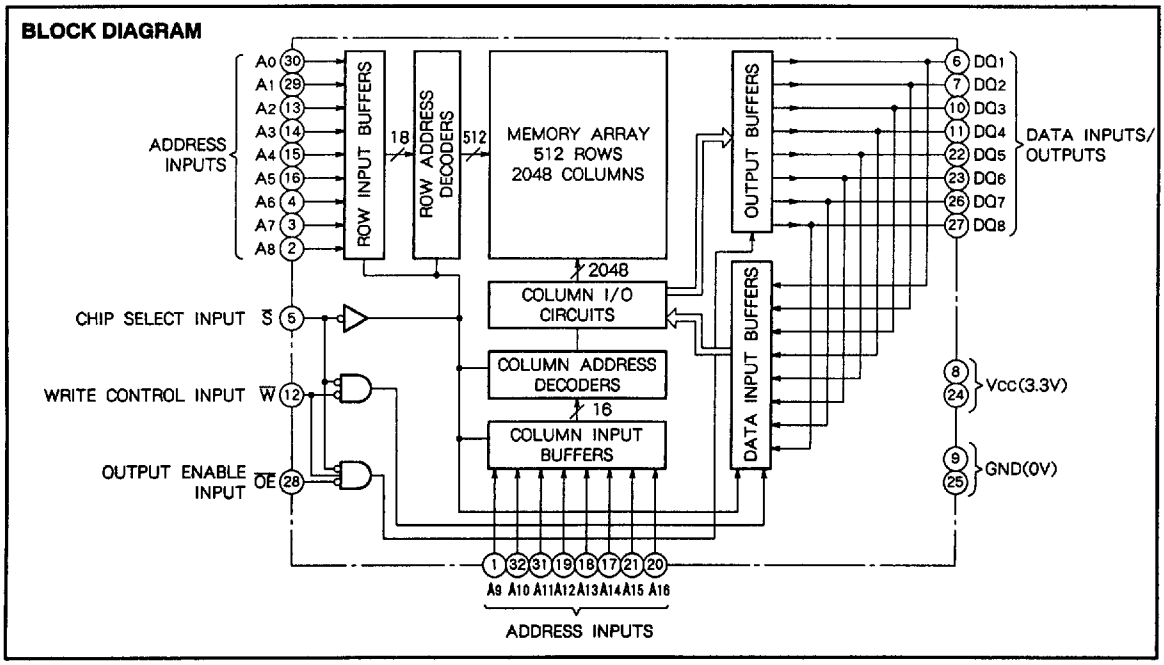
Outline 32P0K(SOJ)

In a read operation, after setting $\overline{W}$ to high, $\overline{S}$ to low and $\overline{OE}$ to low if the address signals are stable, the data is available at the DQ terminal.

When $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other devices.

Signal $\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

MODE SELECTION

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	Data input/output	Icc
H	X	X	Non selection	High-impedance	Stand by
L	X	X	Non selection	High-impedance	Active
L	L	X	Write	Din	Active
L	H	L	Read	Dout	Active
L	H	H		High-impedance	Active

H : V_{IH} L : V_{IL} X : V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	− 2.0* ~4.6	V
V_I	Input voltage		− 2.0* ~V_{CC} + 0.5 (max 4.6)	V
V_O	Output voltage		− 2.0* ~V_{CC}	V
P_d	Maximum power dissipation		1	W
T_{opr}	Operating temperature		0~70	℃
$T_{stg(bias)}$	Storage temperature (bias)		− 10~85	℃
T_{stg}	Storage temperature		− 65~150	℃

* Pulse width ≤ 10ns, In case of DC : − 0.5V

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 3.3V ± 0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			− 0.3*		0.8	V
V_{OH}	High-level output voltage	I_{OH} = − 2mA		2.4			V
		I_{OH} = − 0.1mA		V_{CC}-0.2			
V_{OL}	Low-level output voltage	I_{OL} = 2mA				0.4	V
		I_{OL} = 0.1mA				0.2	
I_I	Input current	V_I = 0~V_{CC}				2	μA
$\|I_{OZ}\|$	Off-state output current	$V_{I(\overline{S})}$ = V_{IH}, V_O = 0~V_{CC}				10	μA
I_{CC1}	Supply current from V_{CC}	$V_{I(\overline{S})}$ = V_{IL} Output open	AC(10ns cycle)			185	mA
			AC(12ns cycle)			175	
			AC(15ns cycle)			150	
			DC		90	115	
I_{CC2}	Stand by current	$V_{I(\overline{S})}$ = V_{IH}	AC(10ns cycle)			60	mA
			AC(12, 15ns cycle)			50	
			Other $V_I \geq V_{IH}$ or $\leq V_{IL}$			50	
I_{CC3}	Stand by current	$V_{I(\overline{S})}$ = V_{CC} − 0.2V Other $V_I \leq$ 0.2V or $V_I \geq V_{CC}$ − 0.2V				10	mA

Note 1. Current flow into an IC is positive, out is negative. * − 2.0V in case of AC(Pulse width ≤ 10ns)

CAPACITANCE

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I = GND, V_I = 25mVrms, f = 1MHz			6	pF
C_O	Output capacitance	V_O = GND, V_O = 25mVrms, f = 1MHz			8	pF

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 3.3V ± 0.3V, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ····· V_{IH} = 2.8V, V_{IL} = 0V

Input rise and fall time ····· 3ns

Input timing reference levels ····· V_{IH} = 1.4V, V_{IL} = 1.4V

Output timing reference levels ····· V_{OH} = 1.4V, V_{OL} = 1.4V

Output loads ····· Fig.1, Fig.2

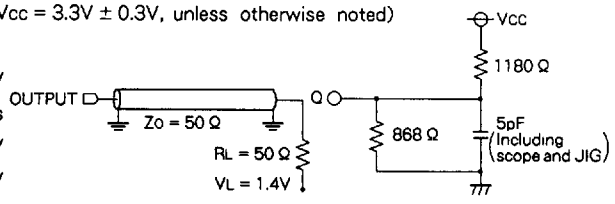


Fig.1 Output load

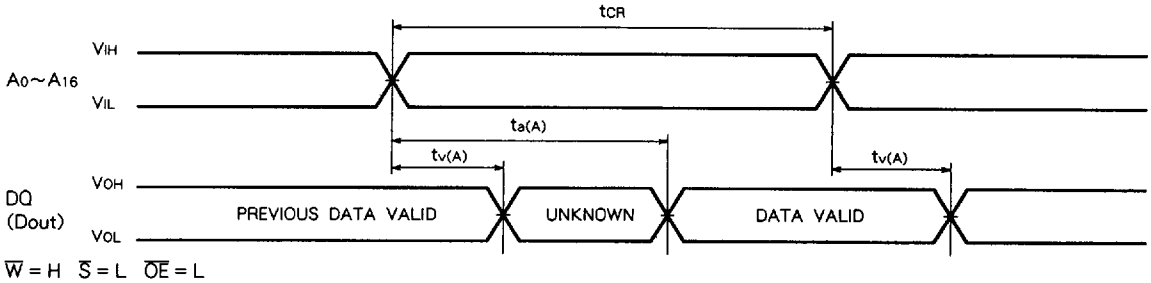
Fig. 2 Output load for t_{en}, t_{dis}

(2) READ CYCLE

Symbol	Parameter	Limits						Unit
		M5M5V1B008-10		M5M5V1B008-12		M5M5V1B008-15		
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	10		12		15		ns
$t_{a(A)}$	Address access time		10		12		15	ns
$t_{a(S)}$	Chip select access time		10		12		15	ns
$t_{a(OE)}$	Output enable access time		5		6		8	ns
$t_{v(A)}$	Data valid time after address change	4		4		4		ns
$t_{en(S)}$	Output enable time from($\overline{S}$)	4		4		4		ns
$t_{en(OE)}$	Output enable time from($\overline{OE}$)	3		3		3		ns
$t_{dis(S)}$	Output disable time from($\overline{S}$)	0	5	0	6	0	7	ns
$t_{dis(OE)}$	Output disable time from($\overline{OE}$)	0	5	0	6	0	7	ns
t_{PU}	Power-up time after chip selection	0		0		0		ns
t_{PD}	Power-down time after chip selection		10		12		15	ns

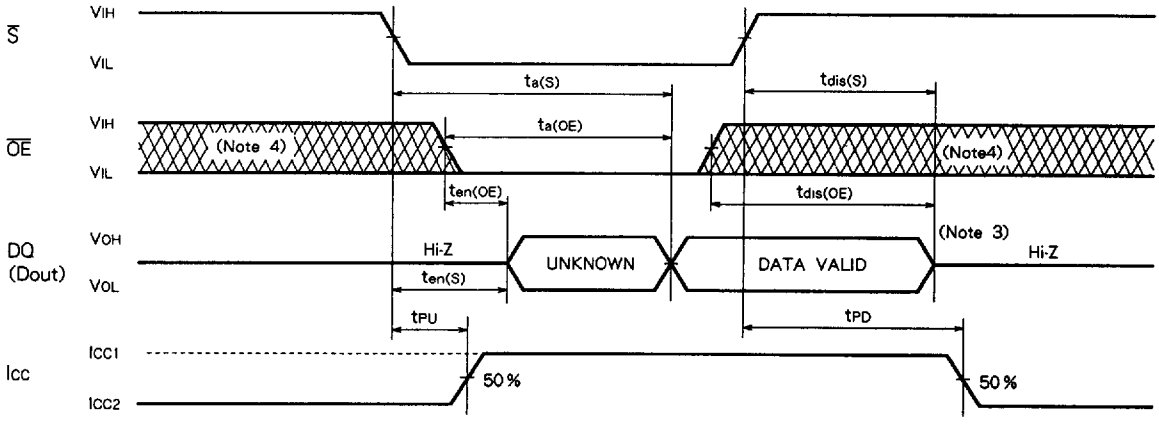
(3) TIMING DIAGRAMS FOR READ CYCLE

Read cycle 1



$\overline{W}$ = H $\overline{S}$ = L $\overline{OE}$ = L

Read cycle 2 (Note 2)



$\overline{W}$ = H

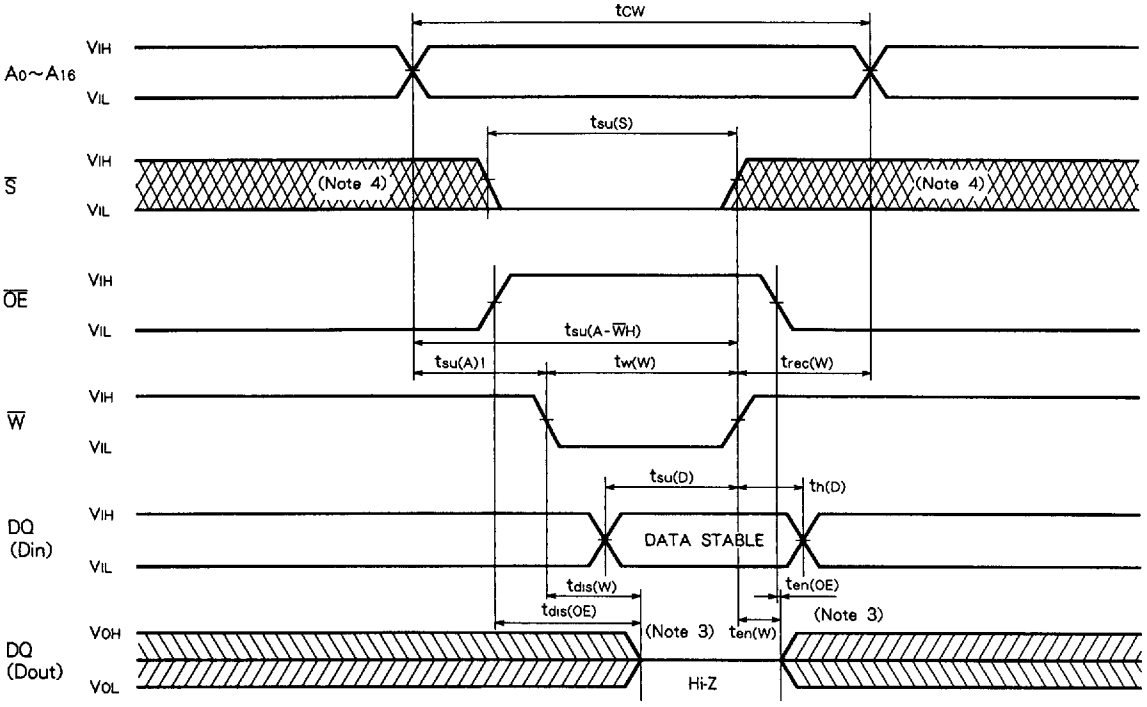
Note 2. Addresses valid prior to or coincident with $\overline{S}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.
4. Hatching indicates the state is don't care.

(4) WRITE CYCLE

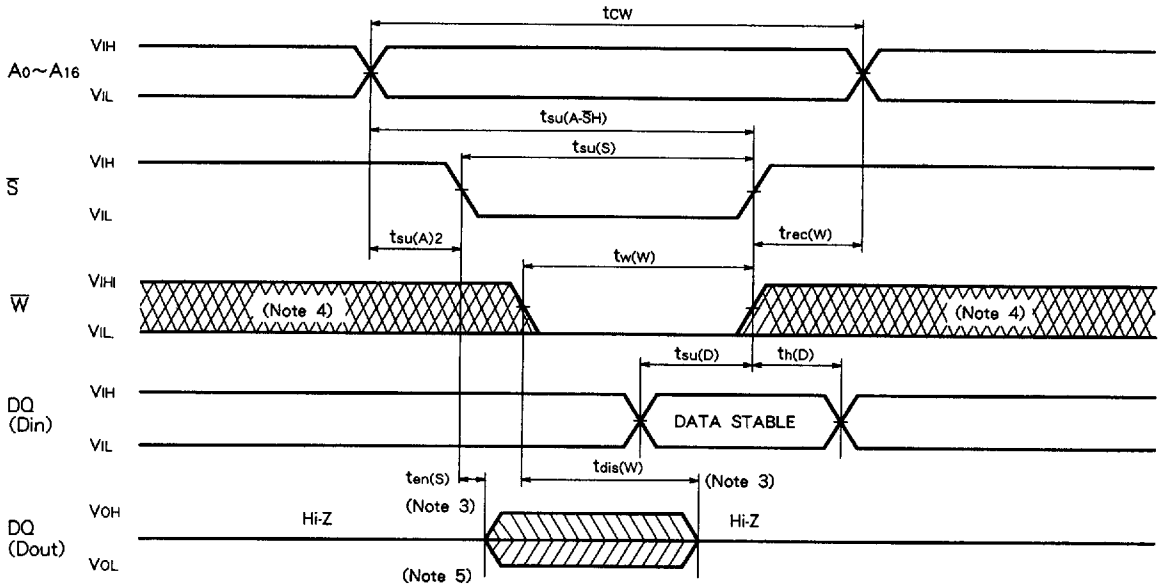
Symbol	Parameter	Limits						Unit
		M5M5V1B008-10		M5M5V1B008-12		M5M5V1B008-15		
		Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	10		12		15		ns
$t_{su(S)}$	Chip select setup time	9		10		12		ns
$t_{su(A)1}$	Address setup time($\overline{W}$)	0		0		0		ns
$t_{su(A)2}$	Address setup time($\overline{S}$)	0		0		0		ns
$t_{w(W)}$	Write pulse width	9		10		12		ns
$t_{rec(W)}$	Write recovery time	0		0		0		ns
$t_{su(D)}$	Data setup time	5		6		7		ns
$t_{h(D)}$	Data hold time	0		0		0		ns
$t_{dis(W)}$	Output disable time from($\overline{W}$)	0	5	0	6	0	7	ns
$t_{dis(OE)}$	Output disable time from($\overline{OE}$)	0	5	0	6	0	7	ns
$t_{en(W)}$	Output enable time from($\overline{W}$)	0		0		0		ns
$t_{en(OE)}$	Output enable time from($\overline{OE}$)	0		0		0		ns
$t_{su(A-\overline{W}H)}$	Address to $\overline{W}$ high	9		10		12		ns
$t_{su(A-\overline{S}H)}$	Address to $\overline{S}$ high	9		10		12		ns

(5) TIMING DIAGRAMS FOR WRITE CYCLE

Write cycle 1 ($\overline{W}$ control mode)



Write cycle 2 ($\overline{S}$ control mode)



Note 5. When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.

6. Don't apply inverted phase signal externally when DQ pin is output mode.