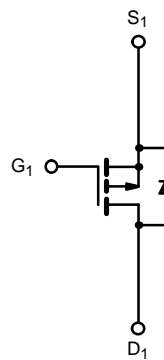
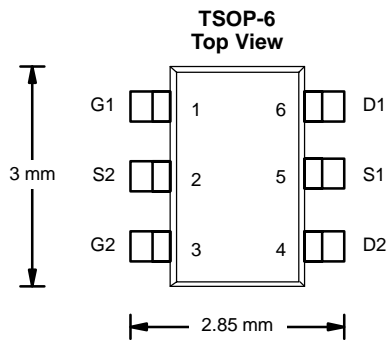




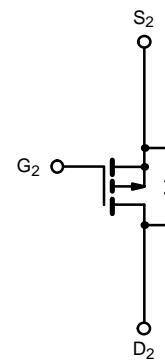
Dual P-Channel 20-V (D-S) MOSFET

TrenchFET[®]
Power MOSFETs
1.8-V Rated

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-20	0.145 @ $V_{GS} = -4.5$ V	-2.2
	0.200 @ $V_{GS} = -2.5$ V	-1.8
	0.300 @ $V_{GS} = -1.8$ V	-1.5



P-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	5 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	-20		V	
Gate-Source Voltage	V_{GS}	± 8			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	-2.2	-1.8	A
		$T_A = 70^\circ\text{C}$	-1.8	-1.5	
Pulsed Drain Current	I_{DM}	± 8			
Continuous Diode Current (Diode Conduction) ^a	I_S	-1.05	-0.75		
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	1.15	0.83	W
		$T_A = 70^\circ\text{C}$	0.73	0.53	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 5$ sec	93	110	$^\circ\text{C/W}$
		Steady State	130	150	
Maximum Junction-to-Foot (Drain)	R_{thJF}	90	90		

Notes

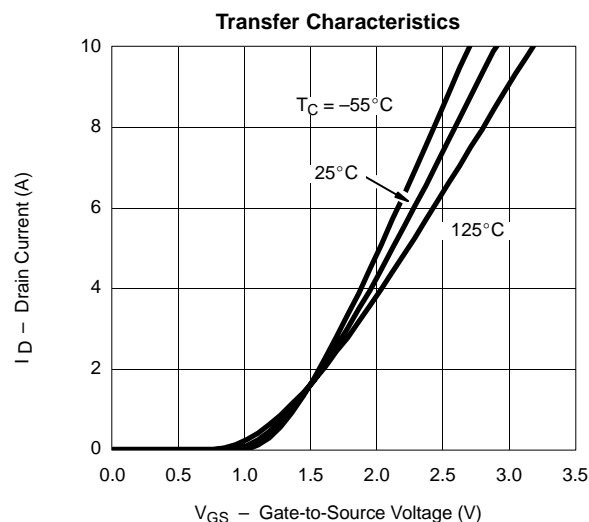
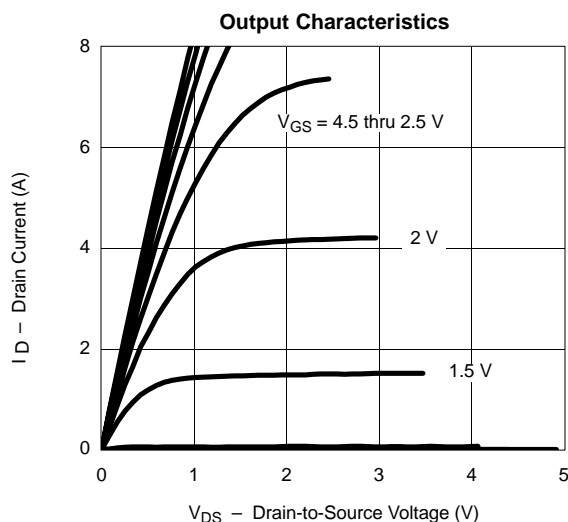
a. Surface Mounted on 1" x 1" FR4 Board.

SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-0.45			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -16 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -16 V, V _{GS} = 0 V, T _J = 85 °C			-10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} = -5 V, V _{GS} = -4.5 V	-5			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = -4.5 V, I _D = -2.2 A		0.115	0.145	Ω
		V _{GS} = -2.5 V, I _D = -1.8 A		0.163	0.200	
		V _{GS} = -1.8 V, I _D = -1.0 A		0.240	0.300	
Forward Transconductance ^a	g _{fs}	V _{DS} = -5 V, I _D = -2.2 A		5		S
Diode Forward Voltage ^a	V _{SD}	I _S = -1.05 A, V _{GS} = 0 V		-0.8	-1.1	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -2.2 A		5	7.5	nC
Gate-Source Charge	Q _{gs}			1		
Gate-Drain Charge	Q _{gd}			0.9		
Turn-On Delay Time	t _{d(on)}	V _{DD} = -4 V, R _L = 8 Ω I _D ≅ -1 A, V _{GEN} = -4.5 V, R _G = 6 Ω		12	20	ns
Rise Time	t _r			29	50	
Turn-Off Delay Time	t _{d(off)}			24	45	
Fall Time	t _f			30	50	
Source-Drain Reverse Recovery Time	t _{rr}		I _F = -1.05 A, di/dt = 100 A/μs		20	

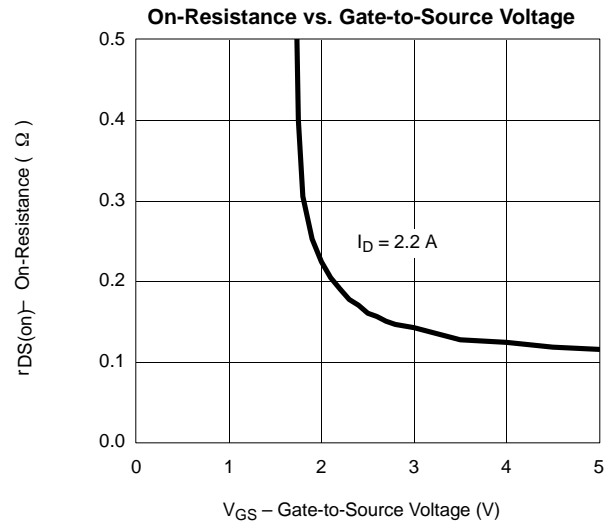
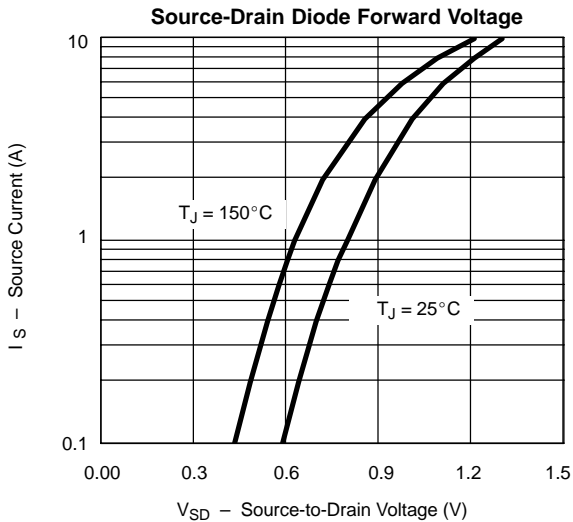
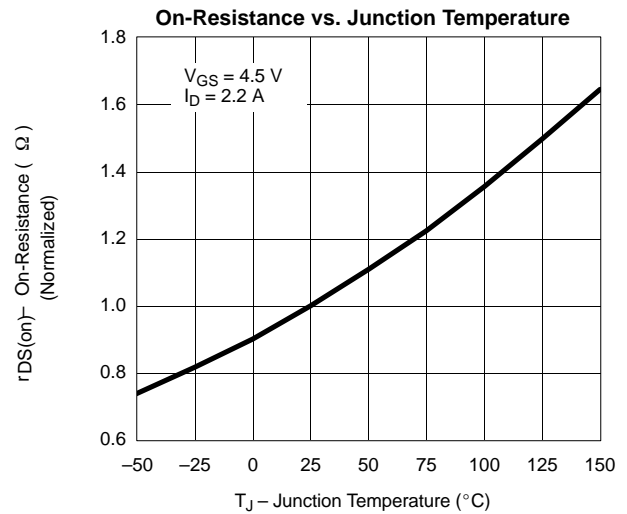
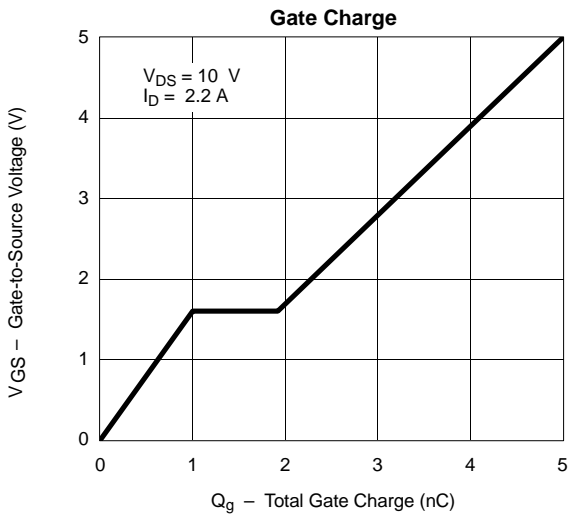
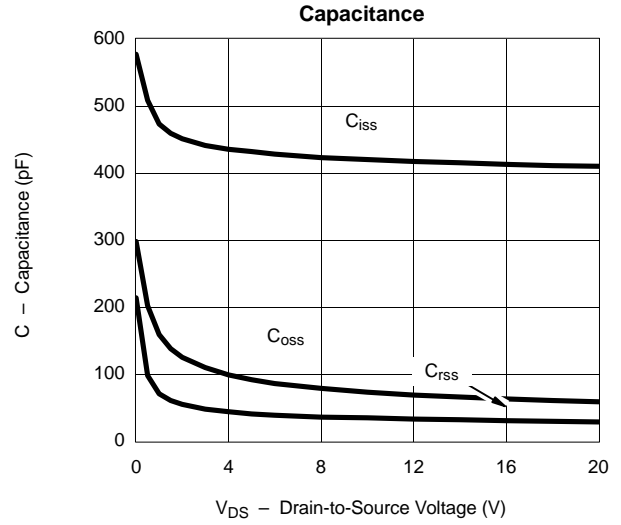
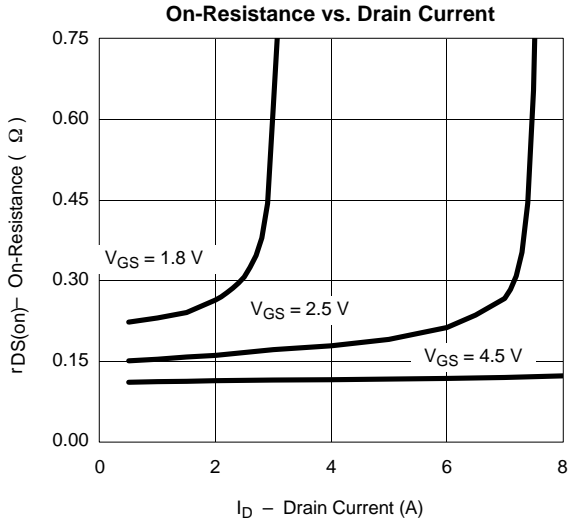
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

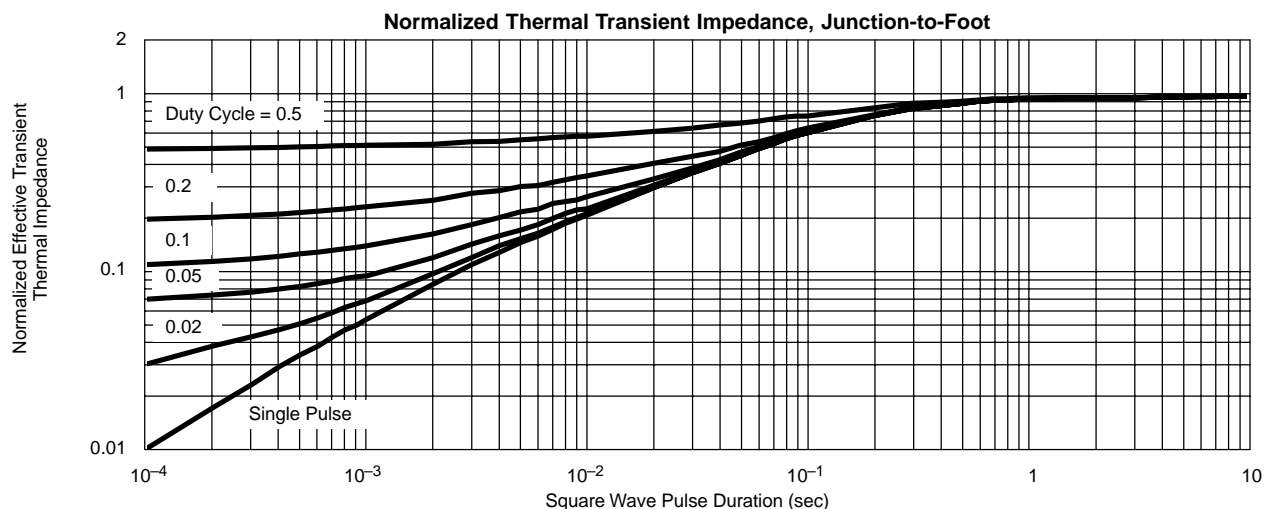
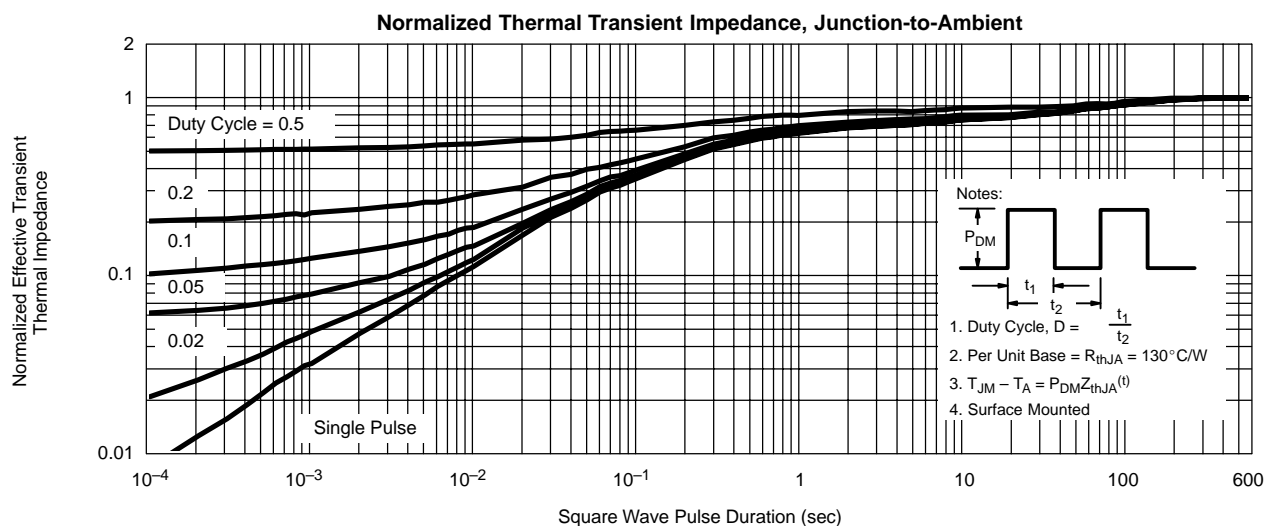
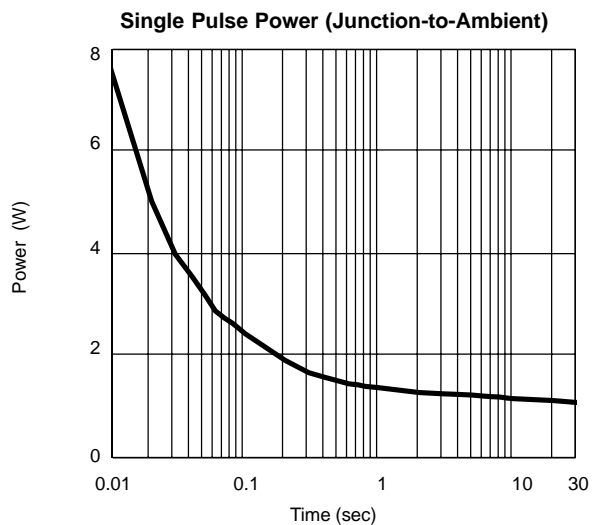
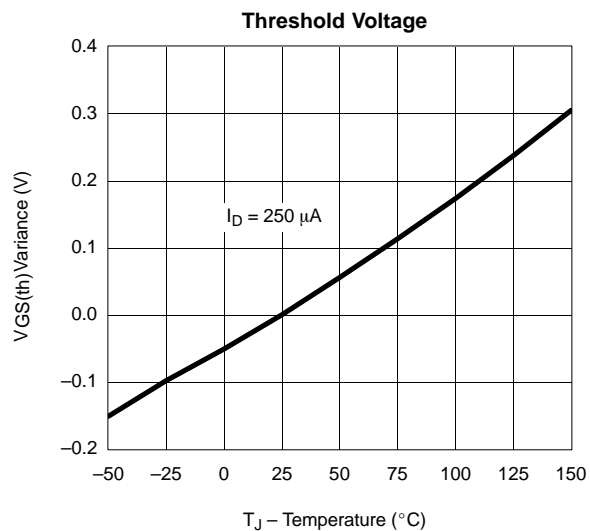
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





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