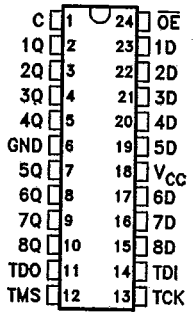
SN54BCT8373, SN74BCT8373
SCAN TEST DEVICES WITH OCTAL D-TYPE LATCHES

T-46-07-27

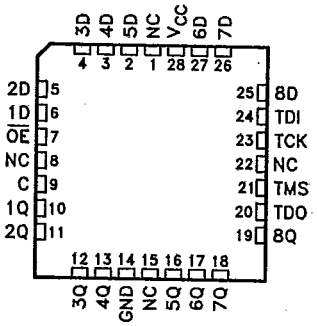
TI0222—D8373 JUNE 1990

- Members of Texas Instruments SCOPE™ Family of Testability Products
- Octal Test Integrated Circuits
- Compatible With the IEEE Standard 1149.1 (JTAG) Serial Test Bus
- Functionally Equivalent to SN54/74F373 and SN54/74BCT373 in the Normal Function Mode
- Test Operation Synchronous to Test Access Port (TAP)
- Implement Optional "Test Reset" Signal on TAP by Recognizing a Double-High on TMS Pin
- SCOPE™ Instruction Set
  - Conform to the IEEE 1149.1 Boundary Scan
  - Provide Data Compression of Inputs
  - Provide Pseudo-Random Pattern Generation From Outputs
  - Sample Input/Toggle Output Mode
  - Output to High-Impedance State Mode
- Fabricated Using TI's State-of-the-Art BICMOS Technology
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

SN54BCT8373 ... JT PACKAGE
SN74BCT8373 ... DW OR NT PACKAGE
(TOP VIEW)



SN54BCT8373 ... FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The SN54BCT8373 and SN74BCT8373 are members of Texas Instruments SCOPE™ testability IC family. This family of components blends test circuitry with standard logic functions to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode these devices are functionally equivalent to the SN54/74F373 and SN54/74BCT373 octal D-type latches. In the test mode, the test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self-test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ octal latches.

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SCAN TEST DEVICES WITH OCTAL D-TYPE LATCHES

description (continued)

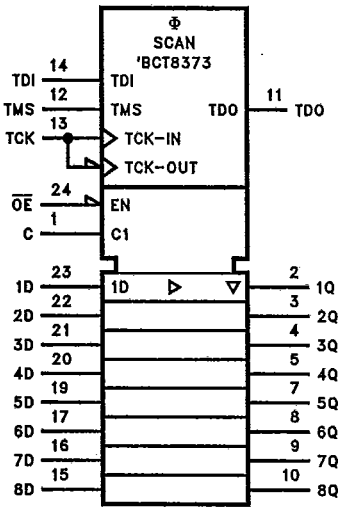
In the test mode the normal operation of the SCOPE™ octal latch is inhibited and the test circuitry is enabled to observe and control the device's I/O boundary. When enabled, the test circuitry can perform boundary scan test operations as described in the IEEE Standard 1149.1 specification. Four dedicated test pins are used to control the operation of the test circuitry: TDI (test data in), TDO (test data out), TMS (test mode select), and TCK (test clock). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54BCT8373 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT8373 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
$\overline{OE}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

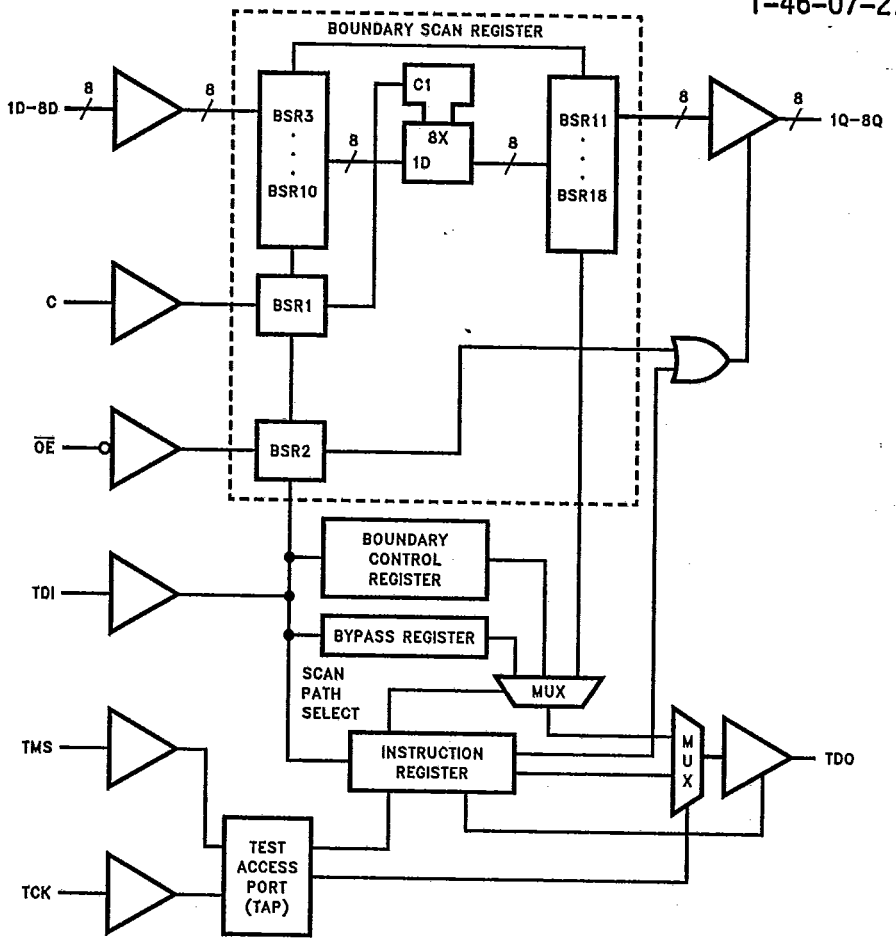
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

functional block diagram

T-46-07-27



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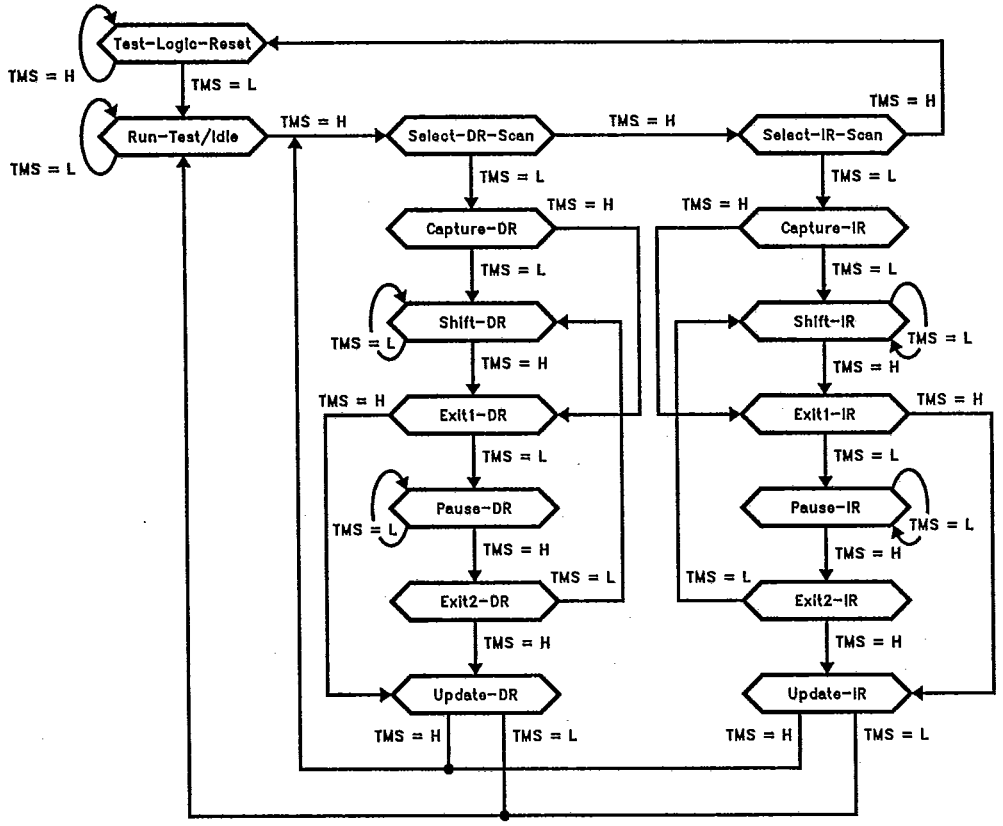

FIGURE 1. TAP STATE DIAGRAM

state diagram description

The TAP proceeds through the states shown in Figure 1 according to the IEEE Standard 1149.1. There are six stable states (indicated by a looping arrow in Figure 1) and ten unstable states in the diagram. A stable state is defined as a state the TAP can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram, one to manipulate a data register and one to manipulate the instruction register. It is necessary to finish manipulating one register before accessing another.

Test-Logic-Reset
In this state, the test logic is not active and the device operates in its normal function mode. The state diagram is constructed such that the TAP will return to this state in no more than five TCK cycles if TMS is high. The TMS pin has an internal pullup resistor that will force it high if left unconnected, or if a board defect causes it to be open-circuited. The device powers up in the Test-Logic-Reset state.

Run-Test/Idle
The TAP must pass through this state before executing any test operations. The test operations controlled by the boundary control register (see Table 2) are performed while in the Run-Test/Idle state.

Select-DR-Scan, Select-IR-Scan
No specific function is performed in these states, and the TAP will exit either of them on the next TCK cycle.

Capture-DR
The selected data register is placed in the scan path. Depending on the current instruction, data may or may not be loaded or captured by that register on the rising edge of TCK causing the TAP state to change. On the falling edge of TCK in Capture-DR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to the level present when it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to a low level.

Shift-DR
While in this state, data is serially shifted through the selected data register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR).

Exit1-DR, Exit2-DR
These are temporary states used to end the shifting process. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. The last shift occurs on the TCK cycle in which the TAP state changes from Shift-DR to Exit1-DR.

Pause-DR
The TAP can remain in this state indefinitely. The Pause-DR state provides the capability of suspending and resuming shift operations without loss of data.

Update-DR
If the current instruction calls for the latches in the selected data register to be updated with current data, the latches are updated during this, and only this, state. TDO goes to the high-impedance state on the falling edge of TCK in Update-DR.

state diagram description (continued)

Capture-IR
The instruction register is preloaded with a 10000001 pattern and placed in the scan path. On the falling edge of TCK in Capture-IR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to the level present when it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to a low level.

Shift-IR
While in this state, data is serially shifted through the instruction register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR).

Exit1-IR, Exit2-IR
These are temporary states used to end the shifting process. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. The last shift occurs on the TCK cycle in which the TAP state changes from Shift-IR to Exit1-IR.

Pause-IR
The TAP can remain in this state indefinitely. The Pause-IR state provides the capability of suspending and resuming shift operations without loss of data.

Update-IR
The latches shadowing the instruction register are updated with the new instruction. TDO goes to the high-impedance state on the falling edge of TCK in Update-IR.

instruction register description

Serial test information is conveyed by means of a 4-wire test bus. Commands, data, and control signals are all passed along the 4-wire bus. The function of the TAP is to extract the state control information and synchronous control signals for the bus and generate the appropriate on-chip control signals for the test structures in the device. The TAP monitors two signals from the bus, TCK and TMS. Figure 1 shows the TAP state diagram. The functional block diagram illustrates the IEEE Standard 1149.1 4-wire test bus and boundary scan architecture, and the relationship between the TAP, the test bus, and the boundary scan test elements.

Data is captured on the rising edge of TCK, and outputs change after the falling edge of TCK.

As shown in the functional block diagram, the 'BCT8373 contains an eight-bit instruction register and three data registers: the 18-bit boundary scan register, the two-bit boundary control register, and the one-bit bypass register. Any register can be thought of as a serial shift register with a shadow latch on each bit. Latches may be loaded during the Update-DR and Update-IR TAP states.

The instruction register (IR) is eight bits long and is used to tell the device what instruction is to be executed. Information contained in the instruction includes the test operation to be performed, the state of the functional inputs and outputs (whether or not the device will perform its normal function during the test operation), which of the three data registers is to be selected for inclusion in the scan path during the next data register scan operation, and the source of the data preloaded in the data register during the Capture-DR state. Table 1 lists the instructions supported by the 'BCT8373. Any SCOPE™ instructions not supported default to BYPASS.

The IR is loaded during the Capture-IR state with the value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path.

The instruction register order of scan is shown in Figure 2.

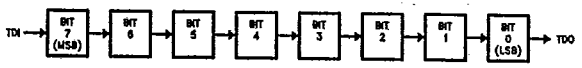

FIGURE 2. INSTRUCTION REGISTER ORDER OF SCAN

data register descriptions

boundary scan register

The boundary scan register (BSR) contains 18 bits, one for each functional input and output on the device. The BSR is used to store test data that is to be applied internally and/or externally to the device, and to capture and store data that is applied to the functional inputs and outputs of the device. The origination of the value loaded in the BSR during the Capture-DR state is determined by the current instruction.

The boundary scan register order of scan is shown in Figure 3.

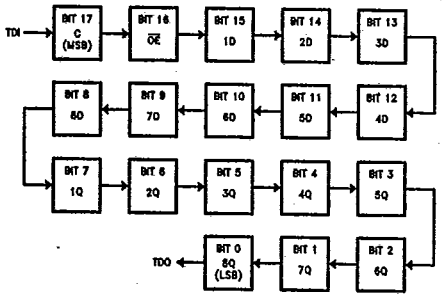

FIGURE 3. BOUNDARY SCAN REGISTER ORDER OF SCAN

boundary control register

The boundary control register (BCR) contains two bits and is used to implement additional test operations not included in the SCOPE™ instruction set, including pseudo-random pattern generation (PRPG) and parallel signature analysis (PSA) operations. The BCR retains its current value during the Capture-DR state. The BCR resets to the PSA operation.

The boundary control register order of scan is shown in Figure 4.

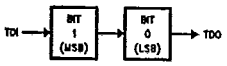

FIGURE 4. BOUNDARY CONTROL REGISTER ORDER OF SCAN

bypass register

The bypass register is a one-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation. The bypass register is loaded with a logic 0 during the Capture-DR state.

The bypass register order of scan is shown in Figure 5.

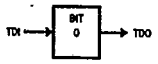

FIGURE 5. BYPASS REGISTER ORDER OF SCAN

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TABLE 1. INSTRUCTION REGISTER OPCODES

BINARY CODE†‡ BIT 7 → BIT 0 MSB → LSB	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER	MODE
X0000000	EXTEST	Boundary Scan	Boundary Scan	Test
X0000001	BYPASS§	Bypass Scan	Bypass	Normal
X0000010	SAMPLE	Sample Boundary	Boundary Scan	Normal
X0000011	INTEST	Boundary Scan	Boundary Scan	Test
X0000100	BYPASS§	Bypass Scan	Bypass	Normal
X0000101	BYPASS§	Bypass Scan	Bypass	Normal
X0000110	TRIBYP	Control Boundary to High-Impedance	Bypass	Modified Test
X0000111	SETBYP	Control Boundary to 1/0	Bypass	Test
X0001000	BYPASS§	Bypass Scan	Bypass	Normal
X0001001	RUNT	Boundary Run Test	Bypass	Test
X0001010	READBN	Boundary Read	Boundary Scan	Normal
X0001011	READBT	Boundary Read	Boundary Scan	Test
X0001100	CELLTST	Boundary Self-test	Boundary Scan	Normal
X0001101	TOPHIP	Boundary Toggle Outputs	Bypass	Test
X0001110	SCANCN	Boundary Control Register Scan	Boundary Control	Normal
X0001111	SCANCT	Boundary Control Register Scan	Boundary Control	Test
ALL OTHER	BYPASS	Bypass Scan	Bypass	Normal

† The SCOPE instruction set specifies even parity in the eight-bit instruction. This feature is not implemented in the 'BCT8373.
‡ X = Don't care.
§ A SCOPE opcode exists but is not supported in the 'BCT8373.

Instruction register opcode descriptions

The 'BCT8373 runs test instructions based on the value scanned into the instruction register. The test functions are defined as follows:

boundary scan
This instruction simultaneously executes the IEEE Standard 1149.1 EXTEST and INTEST instructions. The boundary scan register is selected in the scan path. Data appearing at the device inputs and outputs is captured. Data previously loaded into the boundary scan register is applied to the device inputs and through the device outputs.

bypass scan
Conforms to the IEEE Standard 1149.1 BYPASS instruction. The one-bit bypass register is selected in the scan path. A logic 0 is loaded in the bypass register. The device operates in the normal mode.

sample boundary
Conforms to the IEEE Standard 1149.1 SAMPLE instruction. Data appearing at the device inputs and outputs is sampled without affecting normal device operation. The boundary scan register is selected in the scan path.

control boundary to high-impedance
The device outputs are placed in the high-impedance state. The bypass register is selected in the scan path. Device inputs remain operational, and the internal logic function will be performed.

control boundary to 1/0
The data in the boundary scan register is applied to the functional inputs and through the device outputs. The bypass register is selected in the scan path.

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instruction register opcode descriptions (continued)

boundary run test
A test operation is run as decoded by the boundary control register. The desired test must be preloaded in the boundary control register, and the TAP placed in the Run-Test/Idle state. The four test operations decoded by the boundary control register are:

– parallel signature analysis (PSA)
Data appearing on the functional data inputs is compressed into sixteen bits. An initial seed value should be scanned into the boundary scan register prior to performing this operation. Figure 6 shows the algorithm through which the signature is generated.

– pseudo-random pattern generation (PRPG)
A pseudo-random pattern is generated at the functional outputs. An initial seed value should be scanned into the boundary scan register prior to performing this operation. Figure 7 shows the algorithm through which the patterns are generated. Note that a seed value of all zeroes will not produce additional patterns.

– simultaneous PSA and PRPG
Both PSA and PRPG operations are performed as shown in Figure 8.

– sample inputs/toggle outputs
Data appearing at the functional inputs is sampled on each TCK rising edge, and the functional outputs are toggled on each TCK falling edge.

boundary read
The boundary scan register is selected in the scan path. No load operation is performed prior to shifting. This instruction is useful for inspecting data after a PSA operation.

boundary control register scan
The two-bit boundary control register is placed in the scan path. This register must be loaded prior to executing a boundary run test operation.

boundary self-test
The boundary scan register is selected in the scan path. This operation tests the logic in the boundary scan cells by loading the inverse of the current value of the cells. By loading a known value in the boundary scan register, executing CELLTST, and inspecting the resulting data through a scan operation, the integrity of the boundary scan register can be verified.

boundary toggle outputs
Functional outputs are toggled on each TCK falling edge. Data appearing on the device's functional inputs is not captured.

tap bits for PSA and PRPG

The BCR opcodes are shown in Table 2. The use of these TAP bits and the algorithms used for 8- and 16-bit PSA and PRPG operations are shown in Figures 6 through 8. The two control inputs, C and $\overline{OE}$, are ignored during these operations.

TABLE 2. BOUNDARY CONTROL REGISTER OPCODES

BINARY CODE BIT 1 → BIT 0 MSB → LSB	DESCRIPTION
00	Sample inputs/toggle outputs
01	PRPG/16-bit mode
10	PSA/16-bit mode
11	Simultaneous PRPG and PSA/8-bit mode

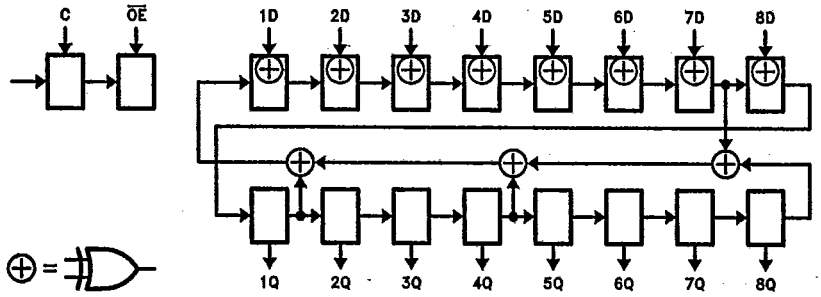

FIGURE 6. 16-BIT PSA CONFIGURATION

A PSA operation on the 8 data inputs proceeds as the 8 data outputs are held static.

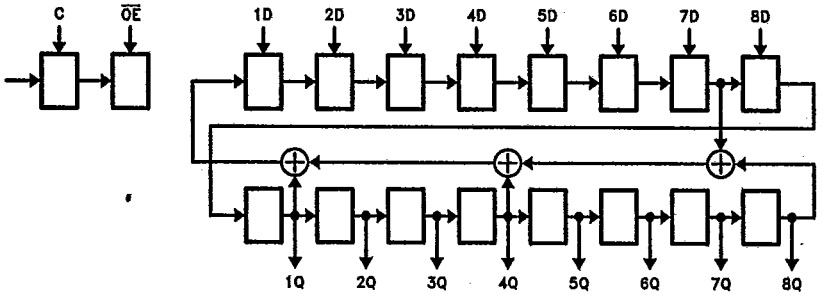

FIGURE 7. 16-BIT PRPG CONFIGURATION

A PRPG operation from the eight data outputs proceeds while the inputs are ignored.

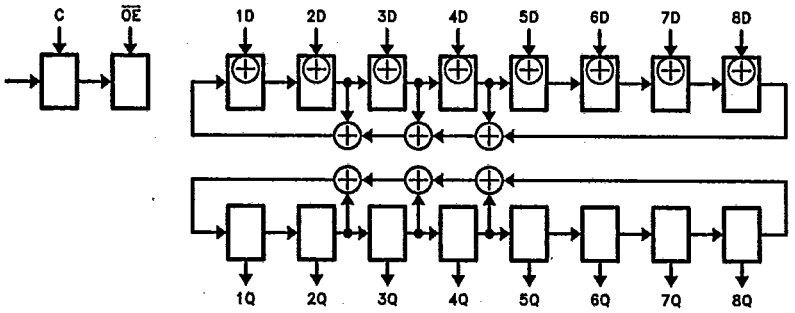

FIGURE 8. 8-BIT PSA AND PRPG CONFIGURATION

Simultaneously, an 8-bit PSA operation proceeds on the 8 data inputs, while an 8-bit PRPG operation proceeds from the 8 data outputs.

timing description

All test operations of the 'BCT8373 are synchronous to TCK. Data on the TDI, TMS, and functional inputs is captured on the rising edge of TCK. Data appears on the TDO and functional output pins on the falling edge of TCK.

The 'BCT8373 is advanced through its state diagram (see Figure 1) by changing the value of TMS and applying a clock pulse to TCK. A simple timing example is shown in Figure 9. In this example, the device begins in the Test-Logic-Reset state and is loaded with an instruction to select the bypass register in the scan path. The binary logic value 101 is shifted through the bypass register from TDI to TDO, and the device is returned to the Test-Logic-Reset state. Table 3 explains the function of the test circuitry during each TCK cycle.

TABLE 3. EXPLANATION OF TIMING EXAMPLE

TCK CYCLE(S)	TAP STATE AFTER TCK	DESCRIPTION/COMMENT
1	Test-Logic-Reset	Recycle on reset state.
2	Run-Test/Idle	Begin advancing towards desired state.
3	Select-DR-Scan	
4	Select-IR-Scan	
5	Capture-IR	IR loads with 10000001; TDO becomes active after falling edge of TCK.
6	Shift-IR	Ready to shift in instruction; TDI must be active before next clock.
7–13	Shift-IR	A BYPASS instruction (11111111) is serially loaded into the IR.
14	Exit1-IR	Note that TMS goes high prior to TCK #14. The last bit of the instruction is shifted in as the TAP advances from Shift-IR to Exit1-IR.
15	Update-IR	The IR is updated with the new instruction. TDO goes inactive (high-impedance) on the falling edge of TCK #15.
16	Select-DR-Scan	
17	Capture-DR	The bypass register loads with a logic 0; TDO becomes active.
18	Shift-DR	The bypass register is now in the scan path. Data will shift from TDI to TDO.
19–20	Shift-DR	The binary value '101' is shifted from TDI to TDO through the bypass register. Note that the last value shifted in (a logic 1) remains in the bypass register and is not shifted to the next test element.
21	Exit1-DR	
22	Update-DR	
23	Select-DR-Scan	
24	Select-IR-Scan	
25	Test-Logic-Reset	Test operation completed.

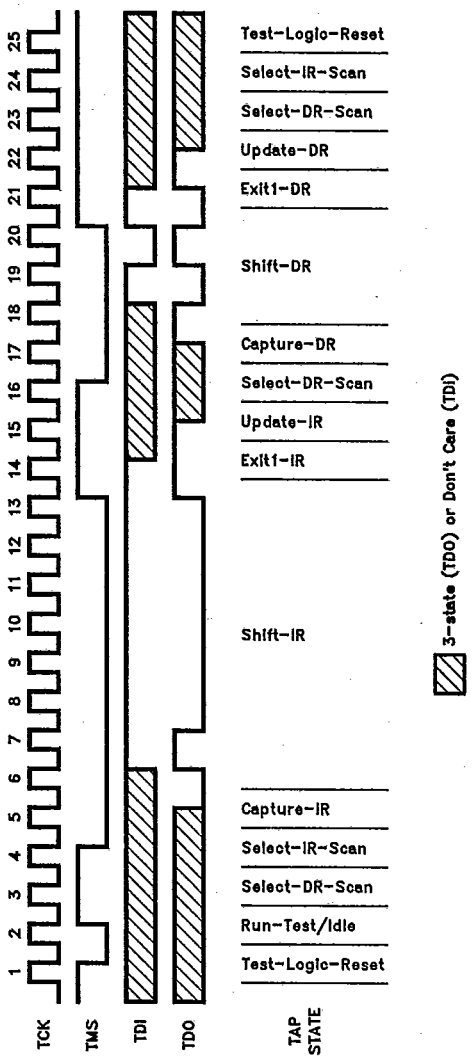

FIGURE 9. TIMING EXAMPLE

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except TMS) ..... −0.5 V to 7 V
Input voltage range, V_I (TMS) ..... −0.5 V to 12 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Current into any output in the low state: SN54BCT8373 (TDO) ..... 40 mA
SN54BCT8373 (Any Q) ..... 96 mA
SN74BCT8373 (TDO) ..... 48 mA
SN74BCT8373 (Any Q) ..... 128 mA
Operating free-air temperature range: SN54BCT8373 ..... −55°C to 125°C
SN74BCT8373 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54BCT8373			SN74BCT8373			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IHH}	Double high-level input voltage	TMS	10	8.6	12	10	8.6	12	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	TDO			−3			−3	mA
		Any Q			−12			−15	
I_{OL}	Low-level output current	TDO			20			24	mA
		Any Y			48			64	
T_A	Operating free-air temperature		−55		125	0		70	°C

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

SN54BCT8373, SN74BCT8373
SCAN TEST DEVICES WITH OCTAL D-TYPE LATCHES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54BCT8373			SN74BCT8373			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	Any Q	V_{CC} = 4.75 V	I_{OH} = −3 mA	2.7	3.4		2.7	3.4		V
		V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		
			I_{OH} = −12 mA	2	3.2					
			I_{OH} = −15 mA				2	3.1		
	TDO		I_{OH} = −1 mA	2.5	3.4		2.5	3.4		
			I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
V_{OL}	Any Q	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				V
			I_{OL} = 64 mA					0.42	0.55	
	TDO		I_{OL} = 20 mA		0.3	0.5				
			I_{OL} = 24 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V, V_I = 5.5 V				0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V, V_I = 2.7 V		−1	35	−100	−1	−35	−100	µA
I_{IHH}	TMS	V_{CC} = 5.5 V, V_I = 10 V			0.3	1		0.3	1	mA
I_{IL}		V_{CC} = 5.5 V, V_I = 0.5 V			−70	−200		−70	−200	µA
I_{OZH}	Any Q	V_{CC} = 5.5 V, V_O = 2.7 V				50			50	µA
	TDO	V_{CC} = 5.5 V, V_O = 2.7 V		−1	−35	−100	−1	−35	−100	
I_{OZL}	Any Q	V_{CC} = 5.5 V, V_O = 0.5 V				−50			−50	µA
	TDO	V_{CC} = 5.5 V, V_O = 0.5 V			−70	−200		−70	−200	
I_{OS}‡		V_{CC} = 5.5 V, V_O = 0		−100		−225	−100		−225	mA
I_{CC}		V_{CC} = 5.5 V, Outputs open	Outputs high		3.5	7		3.5	7	mA
			Outputs low		35	52		35	52	
			Outputs disabled		1.5	3.5		1.5	3.5	
C_i		V_{CC} = 5 V, V_I = 2.5 V or 0.5 V			10			10		pF
C_i	$\overline{OE}$	V_{CC} = 5 V, V_I = 0.5 V			8			8		pF
C_o		V_{CC} = 5 V, V_O = 2.5 V or 0.5 V			14			14		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

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timing requirements

			V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
			'BCT8373			'54BCT8373		'74BCT8373		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0		20	0	20	0	20	MHz
t_w	Pulse duration	TCK high or low	25			25		25		ns
		TMS reset high	50			50		50		
t_{su}	Setup time	TMS before TCK ↑	15			15		15		ns
		TDI before TCK ↑	6			6		6		
		Any D before TCK ↑	6			6		6		
		$\overline{OE}$ before TCK ↑	6			6		6		
t_h	Hold time	TMS after TCK ↑	0			0		0		ns
		TDI after TCK ↑	4.5			4.5		4.5		
		Any D after TCK ↑	4.5			4.5		4.5		
		$\overline{OE}$ after TCK ↑	4.5			4.5		4.5		
t_{pu}		Wait time, power up to TCK ↑	100			100		100		ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN54BCT8373, SN74BCT8373
SCAN TEST DEVICES WITH OCTAL D-TYPE LATCHES

switching characteristics (see Figure 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'BCT8373			'54BCT8373		'74BCT8373		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK		20			20		20		MHz
t_{PLH}	D	Any Q	2	5.6	9	2	11.5	2	10	ns
t_{PHL}			2	5.5	9	2	10.6	2	10	
t_{PLH}	C	Q	3	6.7	10.5	3	12.9	3	11.4	ns
t_{PHL}			3	6.7	10.5	3	12.8	3	11.6	
t_{PLH}	TCK↓	Any Q	3.9	10.9	15.7	3.9	21.5	3.9	19.8	ns
t_{PHL}			3.9	10.8	15.3	3.9	21.5	3.9	19.5	
t_{PLH}	TCK↓	TDO	3.2	8.5	12.3	3.2	16.8	3.2	15.4	ns
t_{PHL}			3.2	8.3	12	3.2	16.2	3.2	15	
t_{PLH}	TCK↑	Any Q	6.2	13.7	21	6.2	29	6.6	25	ns
t_{PHL}			6.6	15	22	6.6	29.6	6.6	26	
t_{PZH}	$\overline{OE}$	Any Q	2.4	5.6	9	2.4	11.1	2.4	10.6	ns
t_{PZL}			3	6.8	10.9	3	12.9	3	12	
t_{PHZ}	$\overline{OE}$	Any Q	2.5	5.7	9.5	2.5	10.9	2.5	10	ns
t_{PLZ}			2.4	5.5	9	2.4	10.5	2.4	9.6	
t_{PZH}	TCK↓	Any Q	4.7	11.7	16.7	4.7	23.1	4.7	21.1	ns
t_{PZL}			5.5	13.6	19.7	5.5	24.4	5.5	22.9	
t_{PHZ}	TCK↓	Any Q	3.4	9	13.2	3.4	18.7	3.4	17.3	ns
t_{PLZ}			3.6	10	14.6	3.6	19.5	3.6	17.8	
t_{PZH}	TCK↑	Any Q	6.9	15.5	21.7	6.9	30	6.9	27	ns
t_{PZL}			7.8	17.6	24.9	7.8	32	7.8	29	
t_{PHZ}	TCK↑	Any Q	5	12.7	18.3	5	25.5	5	22.8	ns
t_{PLZ}			4.6	12.2	17.5	4.6	24.7	4.6	22	
t_{PZH}	TCK↓	TDO	2.4	6.2	9	2.4	11.3	2.4	10.8	ns
t_{PZL}			3.2	7.6	10.6	3.2	13.2	3.2	12.6	
t_{PHZ}	TCK↓	TDO	2.6	7.1	10.2	2.6	13	2.6	12.8	ns
t_{PLZ}			2.2	5.9	8.7	2.2	12.7	2.2	11.6	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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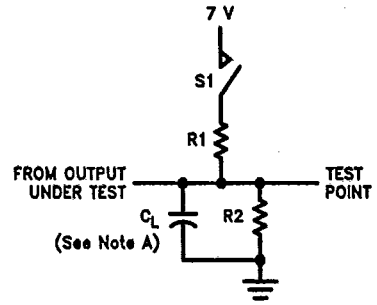
PARAMETER MEASUREMENT INFORMATION

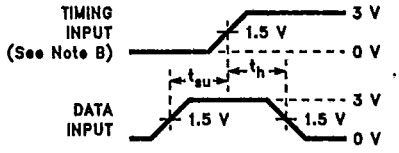
T-46-07-27



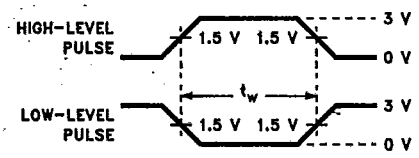
LOAD CIRCUIT

SWITCH POSITION TABLE

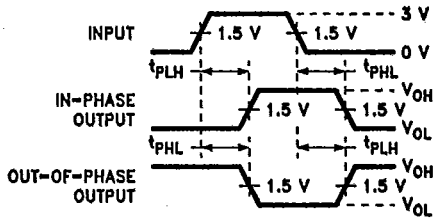
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



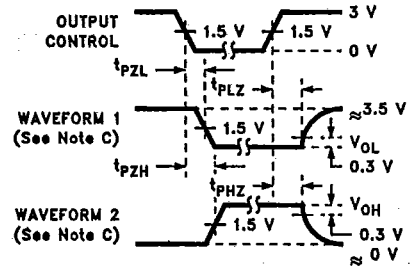
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 10. LOAD CIRCUIT AND VOLTAGE WAVEFORMS