

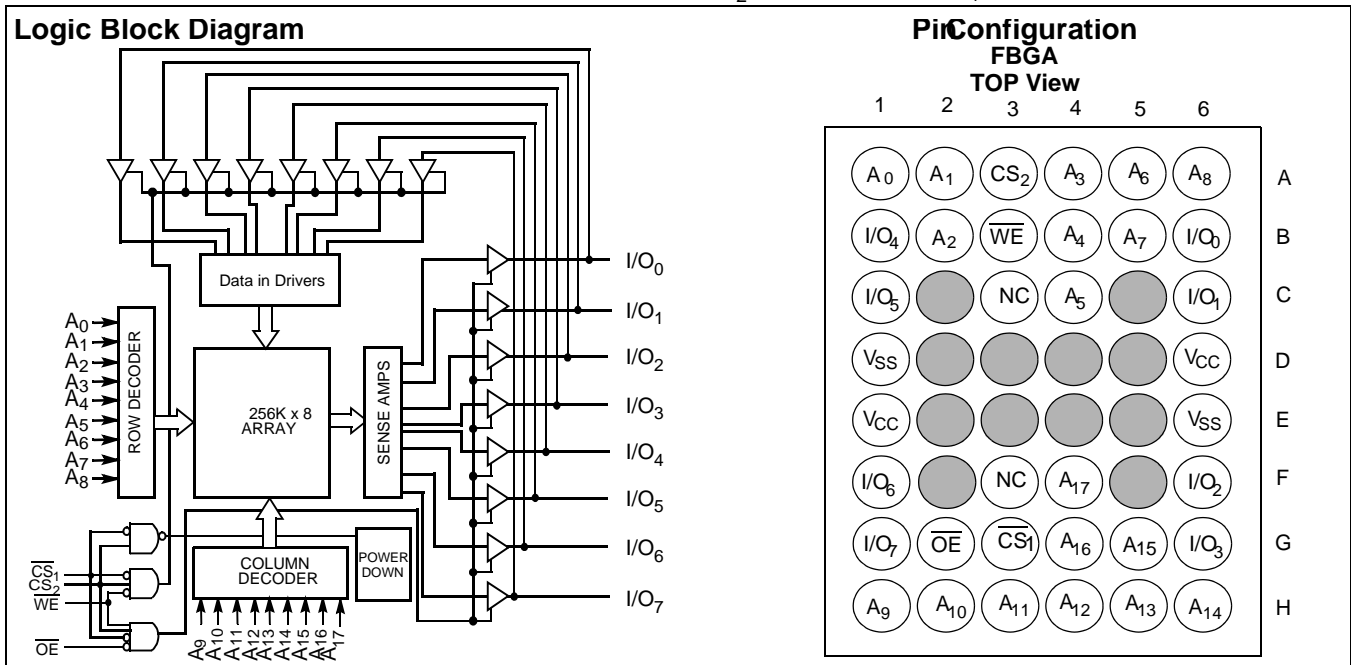
# 256K x 8 Static RAM

## Features

- **Temperature Ranges**
  - Industrial: -40°C to 85°C
- **Low voltage range:**
  - 2.7–3.6V
- **Ultra-low active power**
- **Low standby power**
- **Easy memory expansion with  $\overline{CS}_1/\overline{CS}_2$  and  $\overline{OE}$  features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Offered in standard non-lead-free 36-ball FBGA package**

## Functional Description

The CY62138VN is a high-performance CMOS static RAM organized as 256K words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that reduces power consumption by 99% when addresses are not toggling. The device can be put into standby mode when deselected ( $\overline{CS}_1$  HIGH or  $\overline{CS}_2$  LOW). Writing to the device is accomplished by taking Chip Enable One ( $\overline{CS}_1$ ) and Write Enable (WE) inputs LOW and Chip Enable Two ( $\overline{CS}_2$ ) HIGH. Data on the eight I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is then written into the location specified on the address pins (A<sub>0</sub> through A<sub>17</sub>). Reading from the device is accomplished by taking Chip Enable One ( $\overline{CS}_1$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable (WE) and Chip Enable Two ( $\overline{CS}_2$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins. The eight input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{CS}_1$  HIGH or  $\overline{CS}_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CS}_1$  LOW,  $\overline{CS}_2$  HIGH, and WE LOW).



## Product Portfolio

Product	V <sub>CC</sub> Range			Speed	Power Dissipation (Industrial)			
	V <sub>CC(min)</sub>	V <sub>CC(typ)</sub> <sup>[1]</sup>	V <sub>CC(max)</sub>		Operating (I <sub>CC</sub> )		Standby (I <sub>SB2</sub> )	
					Typ. <sup>[1]</sup>	Maximum	Typ. <sup>[1]</sup>	Maximum
CY62138VN	2.7V	3.0V	3.6V	70 ns	7 mA	15 mA	1 μA	15 μA

**Note:**

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC Typ</sub>, T<sub>A</sub> = 25°C.

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied..... -55°C to +125°C  
 Supply Voltage to Ground Potential ..... -0.5V to +4.6V  
 DC Voltage Applied to Outputs in High-Z State<sup>[2]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

DC Input Voltage<sup>[2]</sup> ..... -0.5V to  $V_{CC} + 0.5V$   
 Output Current into Outputs (LOW)..... 20 mA  
 Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)  
 Latch-up Current..... > 200 mA

### Operating Range

Device	Range	Ambient Temperature	$V_{CC}$
CY62138VN	Industrial	-40°C to +85°C	2.7V to 3.6V

### Electrical Characteristics Over the Operating Range

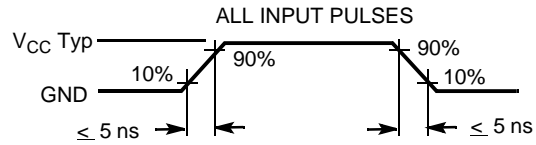
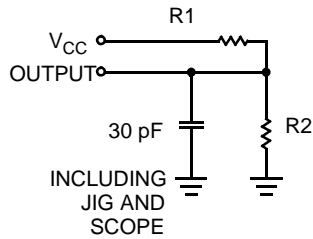
Parameter	Description	Test Conditions		CY62138VN			Unit
				Min.	Typ. <sup>[1]</sup>	Max.	
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -1.0 \text{ mA}$	$V_{CC} = 2.7V$	2.4			V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 2.1 \text{ mA}$	$V_{CC} = 2.7V$			0.4	V
$V_{IH}$	Input HIGH Voltage		$V_{CC} = 3.6V$	2.2		$V_{CC} + 0.5V$	V
$V_{IL}$	Input LOW Voltage		$V_{CC} = 2.7V$	-0.5		0.8	V
$I_{IX}$	Input Leakage Current	$GND \leq V_I \leq V_{CC}$		-1	$\pm 1$	+1	$\mu A$
$I_{OZ}$	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ , Output Disabled		-1	+1	+1	$\mu A$
$I_{CC}$	$V_{CC}$ Operating Supply Current	$I_{OUT} = 0 \text{ mA}$ , $f = f_{MAX} = 1/t_{RC}$ , CMOS Levels	$V_{CC} = 3.6V$		7	15	mA
		$I_{OUT} = 0 \text{ mA}$ , $f = 1 \text{ MHz}$ , CMOS Levels			1	2	mA
$I_{SB1}$	Automatic CE Power-down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , $f = f_{MAX}$		$V_{CC} = 3.6V$		100	$\mu A$
$I_{SB2}$	Automatic CE Power-down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , $f = 0$		$V_{CC} = 3.6V$	1	15	$\mu A$

### Capacitance<sup>[3]</sup>

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ C$ , $f = 1 \text{ MHz}$ , $V_{CC} = V_{CC(typ)}$	6	pF
$C_{OUT}$	Output Capacitance		8	pF

**Notes:**

2.  $V_{IL}(\text{min}) = -2.0V$  for pulse durations less than 20 ns.
3. Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**


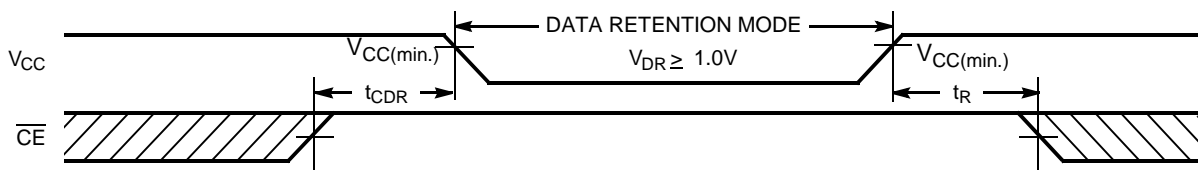
Equivalent to: THÉVENIN EQUIVALENT



Parameters	Value	Unit
R1	1105	Ohms
R2	1550	Ohms
R <sub>TH</sub>	645	Ohms
V <sub>TH</sub>	1.75	Volts

**Data Retention Characteristics (Over the Operating Range)**

Parameter	Description	Conditions <sup>[4]</sup>	Min.	Typ. <sup>[1]</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		1.0		3.6	V
I <sub>CCDR</sub>	Data Retention Current	V <sub>CC</sub> = 1.0V CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V No input may exceed V <sub>CC</sub> +0.3V		0.1	5	μA
t <sub>CDR</sub> <sup>[3]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub>	Operation Recovery Time		100			ms

**Data Retention Waveform<sup>[5]</sup>**

**Notes:**

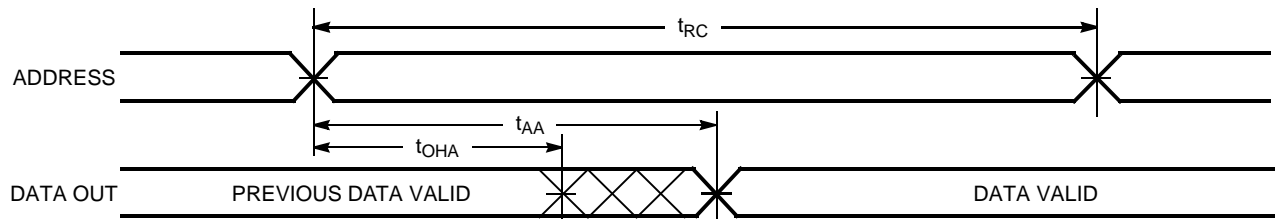
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to V<sub>CC</sub> typ., and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- CE is the combination of both CS<sub>1</sub> and CS<sub>2</sub>.

**Switching Characteristics** Over the Operating Range<sup>[4]</sup>

Parameter	Description	CY62138VN		Unit
		Min.	Max.	
<b>Read Cycle</b>				
$t_{RC}$	Read Cycle Time	70		ns
$t_{AA}$	Address to Data Valid		70	ns
$t_{OHA}$	Data Hold from Address Change	10		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		70	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		35	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low-Z <sup>[6]</sup>	5		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High-Z <sup>[6, 7]</sup>		25	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low-Z <sup>[6]</sup>	10		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High-Z <sup>[6, 7]</sup>		25	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-up	0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-down		70	ns
<b>Write Cycle<sup>[8, 9]</sup></b>				
$t_{WC}$	Write Cycle Time	70		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	60		ns
$t_{AW}$	Address Set-up to Write End	60		ns
$t_{HA}$	Address Hold from Write End	0		ns
$t_{SA}$	Address Set-up to Write Start	0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	50		ns
$t_{SD}$	Data Set-up to Write End	30		ns
$t_{HD}$	Data Hold from Write End	0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High-Z <sup>[6, 7]</sup>		25	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low-Z <sup>[6]</sup>	10		ns

**Switching Waveforms**

**Read Cycle No. 1<sup>[10, 11]</sup>**

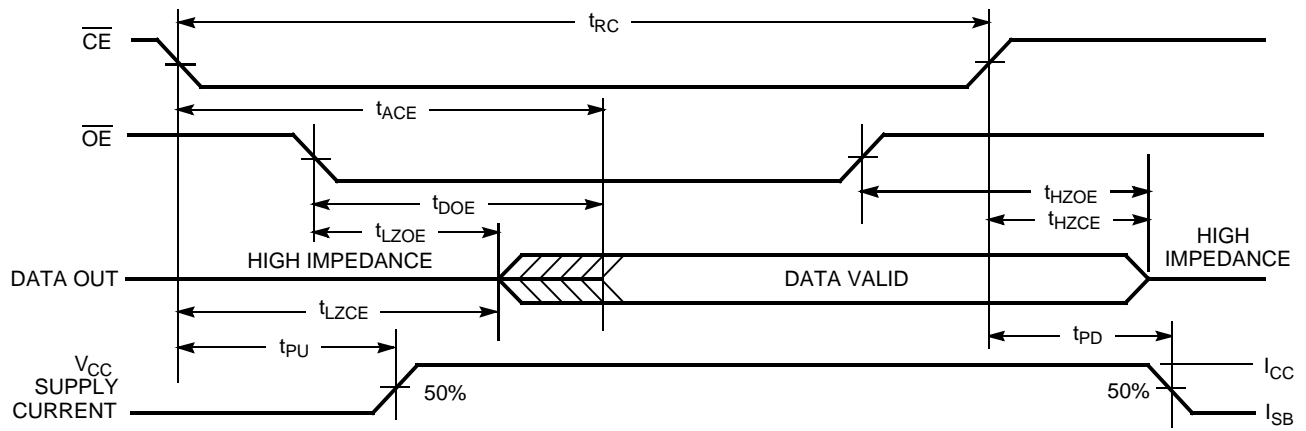


**Notes:**

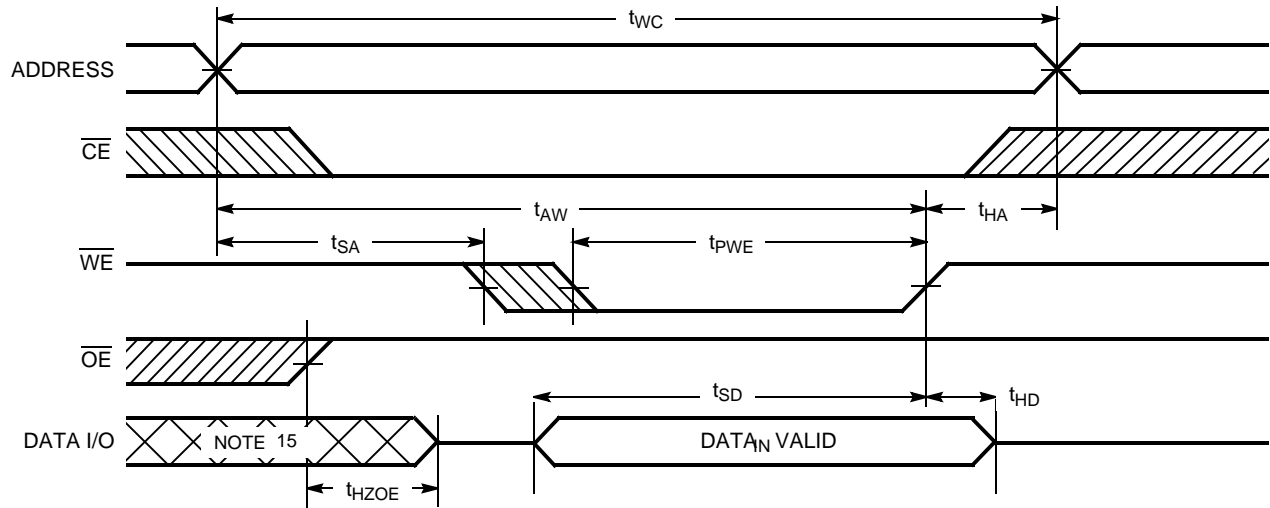
6. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
7.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. The minimum write cycle time for write cycle #3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .
10. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
11.  $\overline{WE}$  is HIGH for read cycle.

Switching Waveforms (continued)

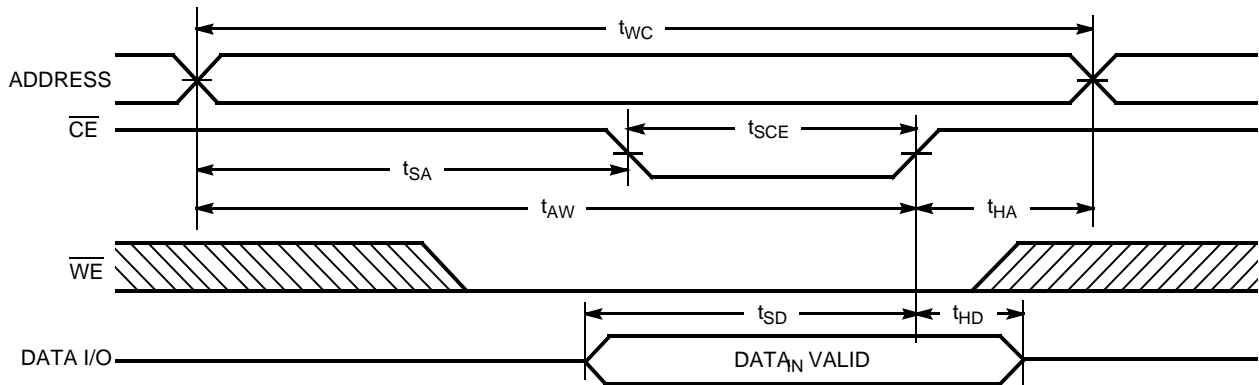
Read Cycle No. 2<sup>[5., 11, 12]</sup>



Write Cycle No. 1 (WE Controlled)<sup>[5, 8, 13, 14]</sup>



Write Cycle No. 2 (CE Controlled)<sup>[5, 8, 13, 14]</sup>

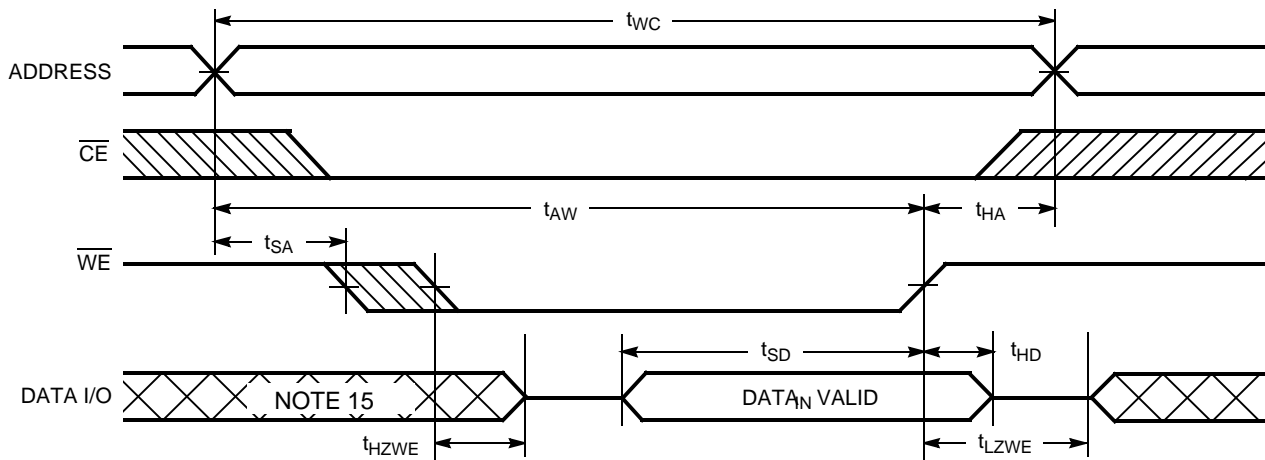


Notes:

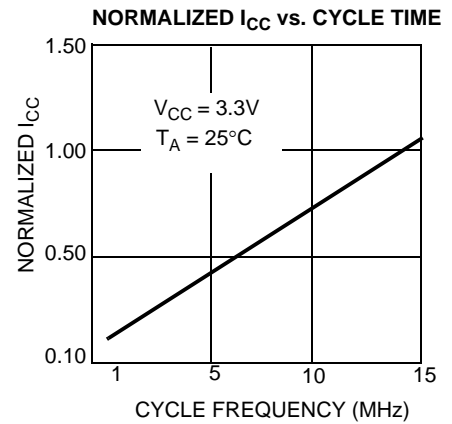
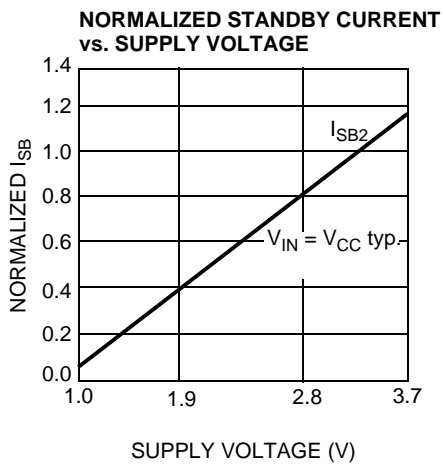
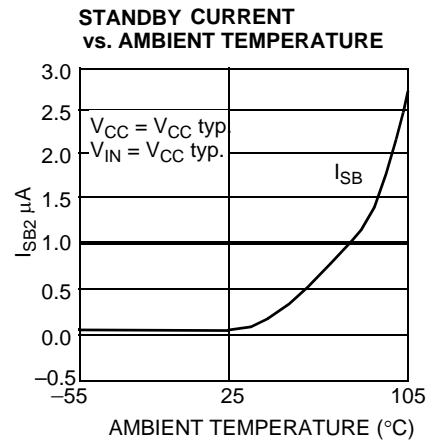
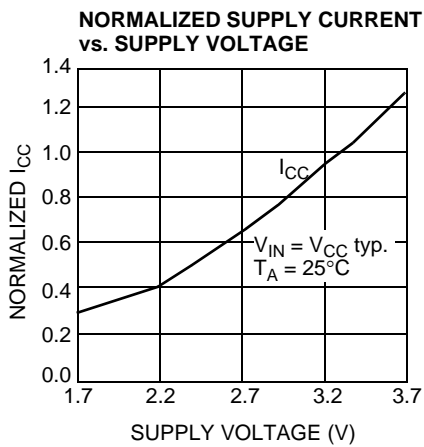
- 12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
- 13. Data I/O is high impedance if  $OE = V_{IH}$ .
- 14. If  $\overline{CE}$  goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.
- 15. During this period, the I/Os are in output state and input signals should not be applied.

**Switching Waveforms** (continued)

Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[5, 9, 14]</sup>



**Typical DC and AC Characteristics**



**Truth Table**

$\overline{CS}_1$	$CS_2$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	X	High-Z	Deselect/Power-down	Standby ( $I_{SB}$ )
X	L	X	X	High-Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	H	H	L	Data Out	Read	Active ( $I_{CC}$ )
L	H	L	X	Data In	Write	Active ( $I_{CC}$ )
L	H	H	H	High-Z	Deselect, Output Disabled	Active ( $I_{CC}$ )

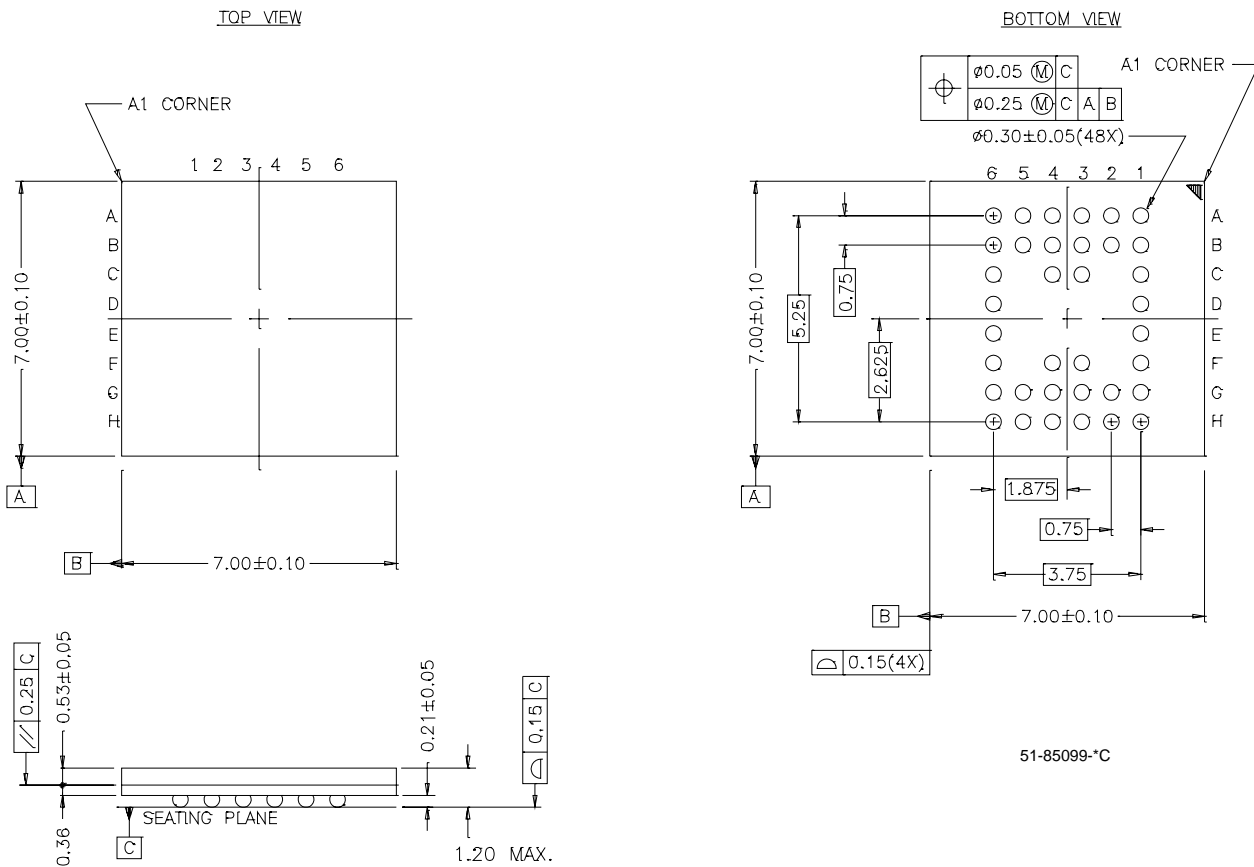
**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
70	CY62138VNLL-70BAI	51-85099	36-ball (7.0 mm x 7.0 mm x 1.2 mm) FBGA	Industrial

Please contact your local Cypress sales representative for availability of other parts

**Package Diagram**

**36-Ball FBGA (7 x 7 x 1.2 mm) (51-85099)**



More Battery Life is a trademark, and MoBL is a registered trademark, of Cypress Semiconductor. All products and company names mentioned in this document may be the trademarks of their respective holders.

**Document History Page**

<b>Document Title: CY62138VN MoBL<sup>®</sup> 256K x 8 Static RAM</b> <b>Document Number: 001-06513</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	426504	See ECN	NXR	New Data Sheet