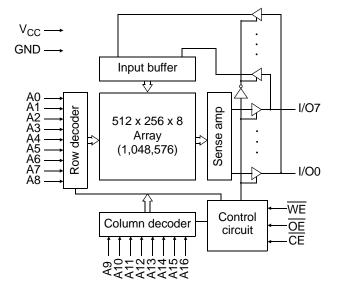


### 5V 128K X 8 CMOS SRAM (Center power and ground)

#### **Features**

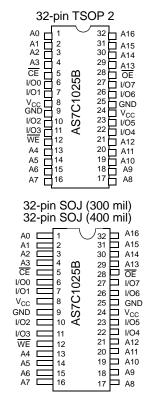
- Product AS7C1025B
- Industrial and commercial temperatures
- Organization: 131,072 x 8 bits
- · High speed
  - 10/12/15/20 ns address access time
  - 5/6/7/8 ns output enable access time
- Low power consumption: ACTIVE
  - 605mW / max @ 10 ns
- Low power consumption: STANDBY
  - 28 mW / max CMOS
- 6 T 0.18 u CMOS technology
- $\bullet$  Easy memory expansion with  $\overline{\text{CE}}, \overline{\text{OE}}$  inputs
- Center power and ground

#### Logic block diagram



- TTL/LVTTL-compatible, three-state I/O
- JEDEC-standard packages
  - 32-pin, 300 mil SOJ
- 32-pin, 400 mil SOJ
- 32-pin, TSOP 2
- ESD protection  $\geq$  2000 volts
- Latch-up current ≥ 200 mA

#### Pin arrangement



### **Selection guide**

	-10	-12	-15	-20	Unit
Maximum address access time	10	12	15	20	ns
Maximum output enable access time	5	6	7	8	ns
Maximum operating current	110	100	90	80	mA
Maximum CMOS standby current	5	5	5	5	mA



### **Functional description**

The AS7C1025B is a high-performance CMOS 1,048,576-bit Static Random Access Memory (SRAM) devices organized as 131,072 x 8 bits. They are designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times  $(t_{AA}, t_{RC}, t_{\underline{WC}})$  of 10/12/15/20 ns with output enable access times  $(t_{OE})$  of 5/6/7/8 ns are ideal for high-performance applications. The chip enable input  $\overline{CE}$  permits easy memory and expansion with multiple-bank memory systems.

When  $\overline{\text{CE}}$  is high, the device enters standby mode. If inputs are still toggling, the device will consume  $I_{SB}$  power. If the bus is static, then full standby power is reached ( $I_{SB1}$ ). For example, the AS7C1026B is guaranteed not to exceed 28 mW under nominal full standby conditions.

A write cycle is accomplished by asserting write enable ( $\overline{WE}$ ) and chip enable ( $\overline{CE}$ ). Data on the input pins I/O0 through I/O7 is written on the rising edge of  $\overline{WE}$  (write cycle 1) or  $\overline{CE}$  (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ( $\overline{OE}$ ) or write enable ( $\overline{WE}$ ).

A read cycle is accomplished by asserting output enable  $(\overline{OE})$  and chip enable  $(\overline{CE})$ , with write enable  $(\overline{WE})$  high. The chips drive I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive or write enable is active, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible, and operation is from a single 5 V supply. The AS7C1025B is packaged in common industry standard packages.

#### **Absolute maximum ratings**

Parameter	Symbol	Min	Max	Unit
Voltage on V <sub>CC</sub> relative to GND	V <sub>t1</sub>	-0.50	+7.0	V
Voltage on any pin relative to GND	V <sub>t2</sub>	-0.50	$V_{CC} + 0.5$	V
Power dissipation	$P_{\mathrm{D}}$	_	1.0	W
Storage temperature (plastic)	T <sub>stg</sub>	-65	+150	° C
Ambient temperature with V <sub>CC</sub> applied	T <sub>bias</sub>	-55	+125	° C
DC current into outputs (low)	I <sub>OUT</sub>	_	20	mA

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### Truth table

CE	WE	OE	Data	Mode
Н	X	X	High Z	Standby (I <sub>SB</sub> , I <sub>SB1</sub> )
L	Н	Н	High Z	Output disable (I <sub>CC</sub> )
L	Н	L	D <sub>OUT</sub>	Read (I <sub>CC</sub> )
L	L	X	D <sub>IN</sub>	Write (I <sub>CC</sub> )

Key: X = don't care, L = low, H = high.



## **Recommended operating conditions**

Parameter	Symbol	Min	Nominal	Max	Unit	
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V	
Input voltage	$V_{IH}$	2.2	_	$V_{CC} + 0.5$	V	
Imput voltage	input voitage				0.8	V
Ambient operating temperature	commercial	$T_{A}$	0	_	70	° C
Amoient operating temperature	industrial	$T_{A}$	-40	_	85	° C

 $<sup>^{\</sup>dagger}$ V<sub>IL</sub> min. = -3.0 V for pulse width less than  $t_{RC}/2$ .

## DC operating characteristics (over the operating range) $^{I}$

			-1	10	-1	12	-15		-20		
Parameter	Symbol	<b>Test conditions</b>	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Input leakage current	I <sub>LI</sub>	$V_{CC} = Max$ , $V_{IN} = GND$ to $V_{CC}$	-	1	_	1	_	1	_	1	μΑ
Output leakage current	I <sub>LO</sub>	$V_{CC} = Max, \overline{CE} = V_{IH},$ $V_{out} = GND \text{ to } V_{CC}$	_	1	_	1	_	1	-	1	μА
Operating power supply current	I <sub>CC</sub>	$\overline{\text{CE}} = V_{\text{IL}}, f = f_{\text{Max}}, I_{\text{OUT}} = 0 \text{ mA}$	_	110	_	100	_	90	_	80	mA
Standby power supply current <sup>I</sup>	$I_{SB}$	$\overline{\text{CE}} = V_{\text{IH}},  f = f_{\text{Max}},  f_{\text{OUT}} = 0$	_	50	_	45	_	45	_	40	mA
	I <sub>SB1</sub>	$\label{eq:center_constraints} \begin{split} \overline{CE} & \geq V_{CC} - 0.2 \text{ V,} \\ V_{IN} \leq 0.2 \text{ V or } V_{IN} \geq V_{CC} - 0.2 \text{ V,} \\ f = 0,  f_{OUT} = 0 \end{split}$	_	5		5		5		5	mA
Output voltage	V <sub>OL</sub>	$I_{OL} = 8 \text{ mA}, V_{CC} = \text{Min}$	_	0.4	ĺ	0.4	_	0.4	ı	0.4	V
Output voltage	$V_{OH}$	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min}$	2.4		2.4	_	2.4	_	2.4	_	V

# Capacitance (f = 1 MHz, $T_a = 25^{\circ}$ C, $V_{CC} = NOMINAL)^2$

Parameter	Symbol	Signals	<b>Test conditions</b>	Max	Unit
Input capacitance	$C_{IN}$	$A, \overline{CE}, \overline{WE}, \overline{OE}$	$V_{IN} = 0 V$	5	pF
I/O capacitance	C <sub>I/O</sub>	I/O	$V_{IN} = V_{OUT} = 0 V$	7	pF



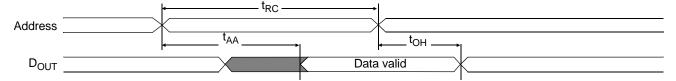
## Read cycle (over the operating range)<sup>3,9</sup>

		-1	10	-1	12	-1	15	-2	20		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Read cycle time	t <sub>RC</sub>	10	-	12	_	15	-	20	_	ns	
Address access time	t <sub>AA</sub>	-	10	_	12	-	15	-	20	ns	3
Chip enable (CE) access time	t <sub>ACE</sub>	-	10	_	12	_	15	_	20	ns	3
Output enable (OE) access time	t <sub>OE</sub>	-	5	-	6	_	7	1	8	ns	
Output hold from address change	t <sub>OH</sub>	3	-	3	_	3	-	3	-	ns	5
CE low to output in low Z	t <sub>CLZ</sub>	3	-	3	_	3	_	3	-	ns	4, 5
CE low to output in high Z	t <sub>CHZ</sub>	-	4	-	5	_	6	1	7	ns	4, 5
OE low to output in low Z	t <sub>OLZ</sub>	0	-	0	_	0	-	0	-	ns	4, 5
OE high to output in high Z	t <sub>OHZ</sub>	-	4	_	5	-	6	_	7	ns	4, 5
Power up time	t <sub>PU</sub>	0	-	0	-	0	-	0	-	ns	4, 5
Power down time	t <sub>PD</sub>	-	10	-	12	1	15	_	20	ns	4, 5

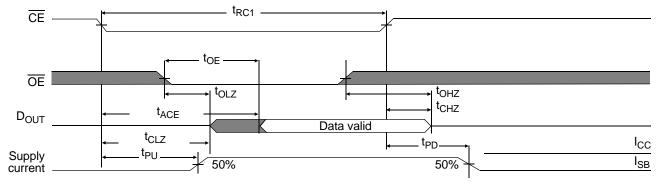
## Key to switching waveforms

Rising input Falling input Undefined/don't care

## Read waveform 1 (address controlled)<sup>3,6,7,9</sup>



## Read waveform 2 (CE and OE controlled)<sup>3,6,8,9</sup>

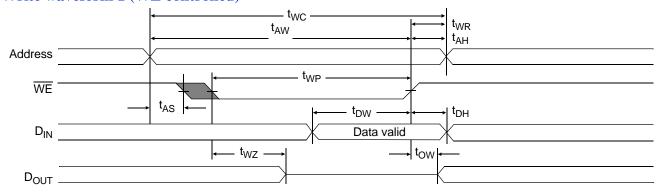




## Write cycle (over the operating range) $^{II}$

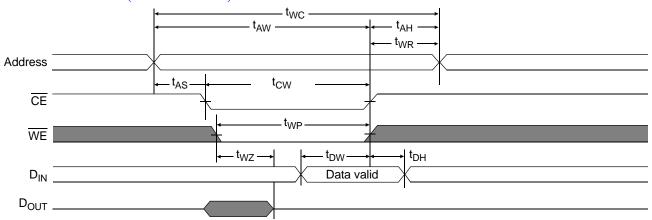
		-1	10	-1	12	-	15	-/	20		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Write cycle time	t <sub>WC</sub>	10	-	12	_	15	-	20	-	ns	
Chip enable $(\overline{CE})$ to write end	t <sub>CW</sub>	8	-	9	_	10	-	12	-	ns	
Address setup to write end	t <sub>AW</sub>	8	-	9	-	10	-	10	-	ns	
Address setup time	t <sub>AS</sub>	0	-	0	1	0	_	0	_	ns	
Write pulse width	t <sub>WP</sub>	7	-	8	_	9	-	12	-	ns	
Write recovery time	t <sub>WR</sub>	0	-	0	-	0	-	0	-	ns	
Address hold from end of write	t <sub>AH</sub>	0	-	0	1	0	_	0	_	ns	
Data valid to write end	t <sub>DW</sub>	5	-	6	_	8	-	10	-	ns	
Data hold time	t <sub>DH</sub>	0	-	0	_	0	-	0	-	ns	4, 5
Write enable to output in high Z	t <sub>WZ</sub>	-	5	_	6	-	7	_	8	ns	4, 5
Output active from write end	t <sub>OW</sub>	1	-	1	_	1	_	2	-	ns	4, 5

## Write waveform 1 (WE controlled)<sup>10,11</sup>



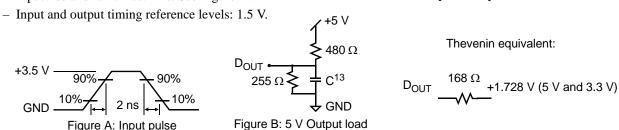


## Write waveform 2 (CE controlled)<sup>10,11</sup>



#### **AC** test conditions

- Output load: see Figure B.
- Input pulse level: GND to 3.5 V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.



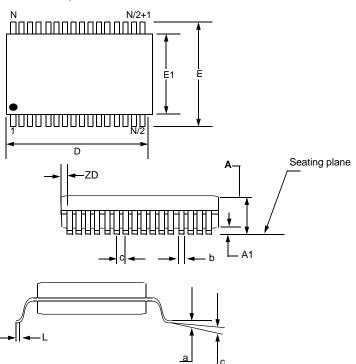
#### **Notes**

- 1 During  $V_{CC}$  power-up, a pull-up resistor to  $V_{CC}$  on  $\overline{CE}$  is required to meet  $I_{SB}$  specification.
- 2 This parameter is sampled, but not 100% tested.
- 3 For test conditions, see AC Test Conditions, Figures A and B.
- $4 t_{CLZ}$  and  $t_{CHZ}$  are specified with CL = 5 pF, as in Figure C. Transition is measured  $\pm 500$  mV from steady-state voltage.
- 5 This parameter is guaranteed, but not 100% tested.
- $\overline{\text{WE}}$  is high for read cycle.
- 7  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  are low for read cycle.
- 8 Address is valid prior to or coincident with  $\overline{\text{CE}}$  transition low.
- 9 All read cycle timings are referenced from the last valid address to the first transitioning address.
- $10 \quad \overline{CE} \text{ or } \overline{WE} \text{ must be high during address transitions. Either } \overline{CE} \text{ or } \overline{WE} \text{ asserting high terminates a write cycle.}$
- 11 All write cycle timings are referenced from the last valid address to the first transitioning address.
- 12 N/A.
- 13 C = 30 pF, except all high Z and low Z parameters where C = 5 pF.



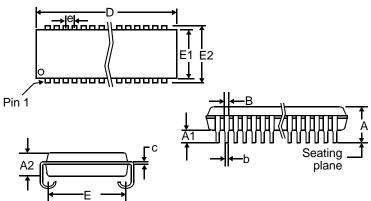
## **Package dimensions**

32-pin TSOP 2



	32-pin TS	OP 2 (mm)			
Symbol	Min	Max			
A	_	1.2			
A1	0.05	0.15			
b	0.3	0.52			
C	0.12	0.21			
D	20.82	21.08			
<b>E</b> 1	10.03	10.29			
E	11.56	11.96			
e	1.27	BSC			
L	0.40	0.60			
ZD	0.95 REF.				
α	0°	5°			





	32-pii 300		32-pin SOJ 400 mil		
Symbol	Min	Max	Min	Max	
A	-	0.145	-	0.145	
<b>A1</b>	0.025	-	0.025	-	
<b>A2</b>	0.086	0.105	0.086	0.115	
В	0.026	0.032	0.026	0.032	
b	0.014	0.020	0.015	0.020	
c	0.006	0.013	0.007	0.013	
D	0.820	0.830	0.820	0.830	
E	0.250	0.275	0.360	0.380	
<b>E</b> 1	0.292	0.305	0.395	0.405	
<b>E2</b>	0.330	0.340	0.435	0.445	
e	0.050	BSC	0.050	BSC	



### **Ordering Codes**

Package \ Access time	Temperature	10 ns	12 ns	15 ns	20 ns
TSOP 2	Commercial	AS7C1025B-10HFC	AS7C1025B-12HFC	AS7C1025B-15HFC	AS7C1025B-20HFC
	Industrial		AS7C1025B-12HFI	AS7C1025B-15HFI	AS7C1025B-20HFI
300-mil SOJ	Commercial	AS7C1025B-10TJC	AS7C1025B-12TJC	AS7C1025B-15TJC	AS7C1025B-20TJC
	Industrial		AS7C1025B-12TJI	AS7C1025B-15TJI	AS7C1025B-20TJI
400-mil SOJ	Commercial	AS7C1025B-10JC	AS7C1025B-12JC	AS7C1025B-15JC	AS7C1025B-20JC
	Industrial		AS7C1025B-12JI	AS7C1025B-15JI	AS7C1025B-20JI

Note: Add suffix 'N' to the above part number for LEAD FREE parts. (Ex AS7C1025B-10TJCN)

#### Part numbering system

AS7C	1025B	-XX	X	X	X
SRAM prefix	Device number	Access time	Package: HF = TSOP 2 / 32 pin TJ = SOJ 300 mil J = SOJ 400 mil	Temperature range C = commercial, 0° C to 70° C I = industrial, -40° C to 85° C	N = LEAD FREE PART

7/14/03, v.0.0.4 Alliance Semiconductor P. 8 of 8

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