



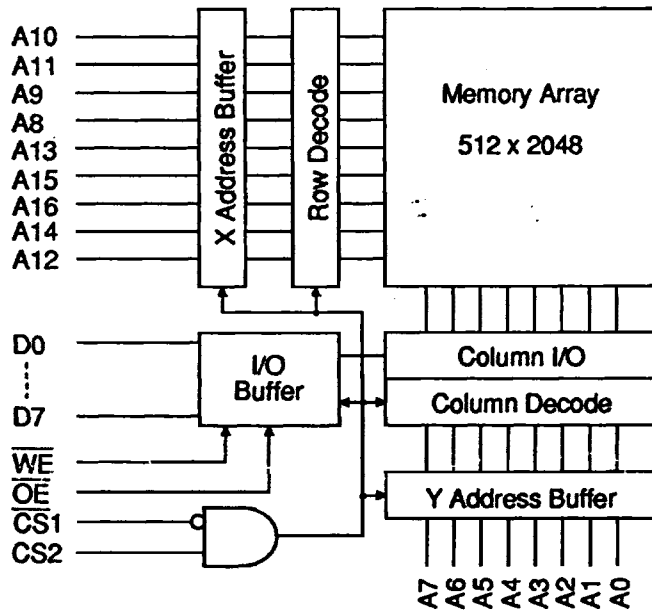
Mosaic Semiconductor Inc.

131,072 x 8 CMOS High Speed Static RAM

Features

- Very Fast Access Times of 020/025/35 ns
- JEDEC Standard 32 pin DIL footprint
- VIL™ High Density Package Available
- Low Power Standby 1.5mW (typ.)
- Low Power Operation 475mW(typ.)
- Completely Static Operation
- 3.0V Battery Back-up Capability.
- Directly TTL compatible
- Common data inputs & outputs
- May be processed in accordance with MIL-STD-883

Block Diagram



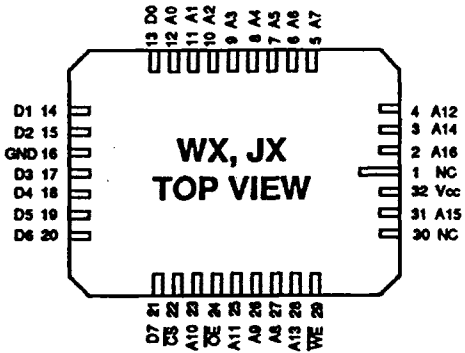
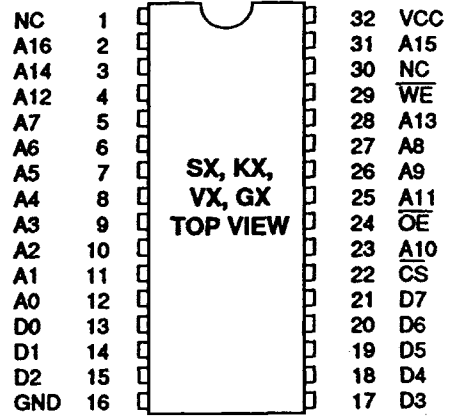
128K x 8 SRAM

MSM8128X-020/025/35

Issue 1.0 : September 1993

ADVANCE PRODUCT INFORMATION

Pin Definition



Pin Functions

- A0-A16** Address Inputs
- D0-7** Data Input/Output
- CS** Chip Select
- OE** Output Enable
- WE** Write Enable
- NC** No Connect
- V_{cc}** Power (+5V)
- GND** Ground

Package Details

Pin Count	Description	Package Type	Material	Pin Out
32	0.6" Dual-in-Line (DIP)	SX	Ceramic	JEDEC
32	0.4" Dual-in-Line (DIP)	KX	Ceramic	JEDEC
32	0.1" Vertical-in-Line (VIL™)	VX	Ceramic	JEDEC
32	Bottom Brazed Flat Pack	GX	Ceramic	JEDEC
32	Extended Leadless Chip Carrier (LCC)	WX	Ceramic	JEDEC PENDING
32	J-Leaded Chip Carrier (JLCC)	JX	Ceramic	JEDEC PENDING

Package dimensions and outlines are displayed on pages 6&7.
 VIL is a trademark of Mosaic Semiconductor, US patent No. D316251

Absolute Maximum Ratings

Voltage on any pin relative to V_{SS}	V_T	-0.5 to +7	V
Power Dissipation	P_T	1	W
Storage Temperature	T_{STG}	-65 to +150	°C

- Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
 (2) V_T can be -3.0V pulse of less than 30ns.

Recommended Operating Conditions

		min	typ	max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	6.5	V
Input Low Voltage	V_{IL}	-0.5	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (8128I)
	T_{AM}	-55	-	125	°C (8128M, MB, MC)

- Notes : (1) V_{IL} can be -3.0V pulse of less than 30ns.

DC Electrical Characteristics ($V_{CC} = 5.0V \pm 10\%$, $T_A = -55^\circ C$ to $+125^\circ C$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	$0V \leq V_{IN} \leq V_{CC}$	-5	-	5	μA
Output Leakage Current	I_{VO}	Outputs disabled, $0V \leq V_{OUT} \leq V_{CC}$	-5	-	5	μA
Operating Supply Current	I_{CC}	$\overline{CS} = V_{IL}$, $V_{CC} = MAX$, $f = MAX = 1/\tau_{RC}$	-	105	155	mA
Standby Supply Current	I_{SB}	$\overline{CS} = V_{IH}$, $V_{CC} = MAX$, $f = MAX = 1/\tau_{RC}$	-	17	40	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$, $V_{CC} = MAX$	-	0.3	10	mA
		$V_{IL} \leq V_{SS} + 0.2V$, $V_{IH} \geq V_{CC} - 0.2V$; $f = 0$	-	0.3	10	mA
"L" version	I_{SB2}	Same as above	-	-	5	mA
Output Voltage	V_{OL}	$I_{OL} = 8.0mA$	-	-	0.4	V
	V_{OH}	$I_{OH} = -4.0mA$	2.4	-	-	V

Note: Typical values are at $V_{CC} = 5.0V$, $T_A = 25^\circ C$ and specified loading.

Capacitance ($V_{CC} = 5V \pm 10\%$, $T_A = 25^\circ C$)

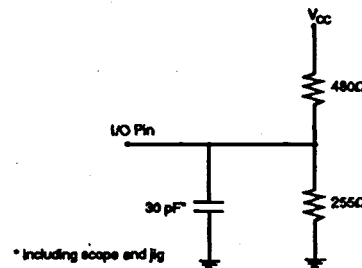
Parameter	Symbol	Test Condition	typ	max	Unit
I/P Capacitance	C_{IN}	$V_{IN} = 0V$	-	8	pF
I/O Capacitance	$C_{I/O}$	$V_{IO} = 0V$	-	8	pF

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

- * Input pulse levels: 0V to 3.0V
- * Input rise and fall times: 5ns
- * Input and Output timing reference levels: 1.5V
- * Output load: See Load Diagram
- * $V_{CC} = 5V \pm 10\%$

Output Load

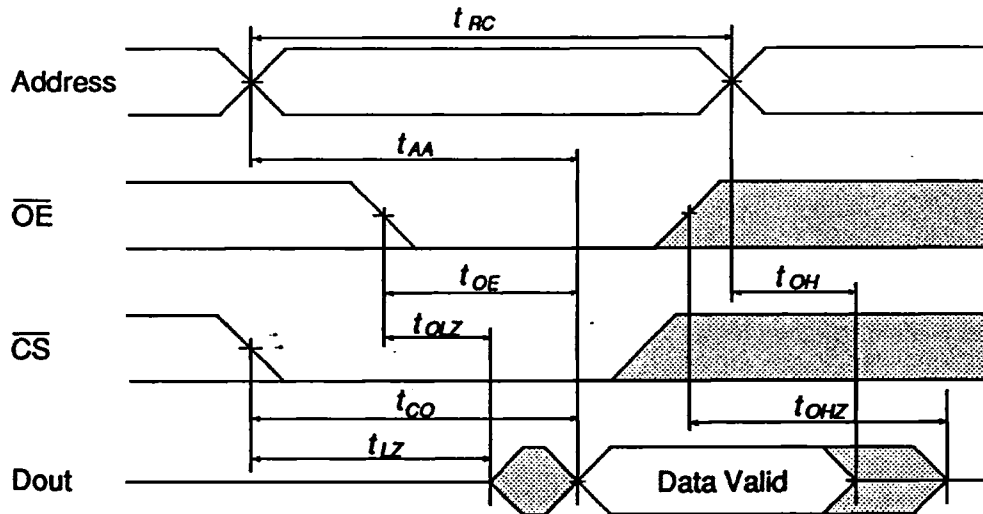


Electrical Characteristics & Recommended AC Operating Conditions

Read Cycle

Parameter	Symbol	-020		-025		-35		Units
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	20	-	25	-	35	-	ns
Address Access Time	t_{AA}	-	20	-	25	-	35	ns
Chip Selection (\overline{CS}) Access Time	t_{ACE}	-	20	-	25	-	35	ns
Output Enable to Output Valid	t_{OE}	-	7	-	8	-	12	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	5	-	ns
Chip Selection (\overline{CS}) to O/P in Low Z ⁽⁵⁾	t_{LZ1}	5	-	5	-	5	-	ns
Output Enable to Output in Low Z	t_{OLZ}	0	-	0	-	0	-	ns
Chip Deselect (\overline{CS}) to O/P in high Z ^(4,5)	t_{HZ1}	0	8	0	10	0	15	ns
Output Disable to Output in High Z ⁽⁴⁾	t_{OHZ}	0	6	-	10	-	12	ns

Read Cycle Timing Waveform ⁽¹⁾


Notes:

(1) \overline{WE} is High for Read Cycle.

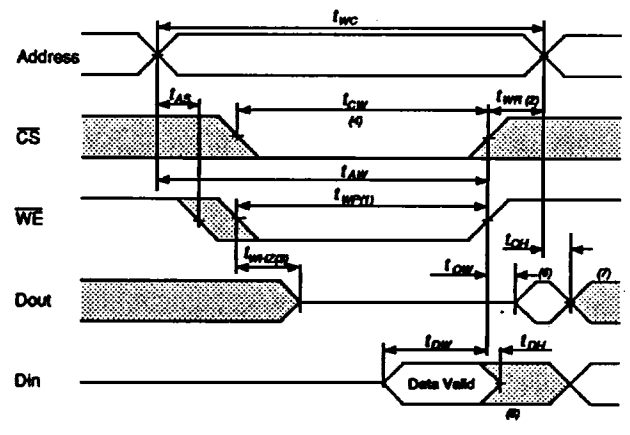
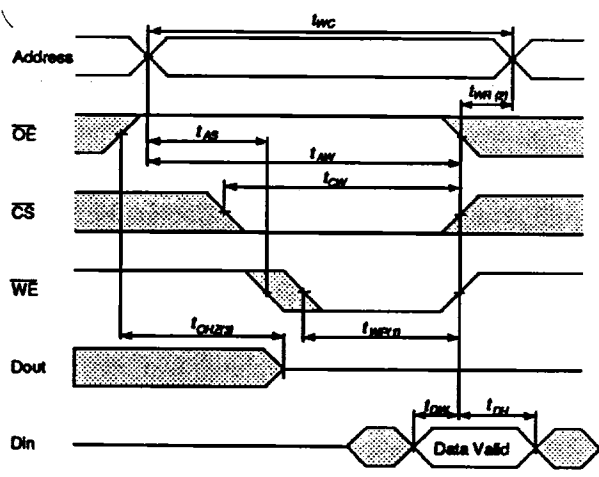
(2) t_{LZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. At any given temperature and voltage condition, t_{LZ} max is less than t_{LZ} min both for a given device and from device to device. This parameter is sampled and not 100% tested.

Write Cycle

Parameter	Symbol	-020		-025		-35		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	20	-	25	-	35	-	ns	
Chip Selection to End of Write	t_{CW}	15	-	16	-	20	-	ns	
Address Valid to End of Write	t_{AW}	15	-	16	-	20	-	ns	
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns	
Write Pulse Width	t_{WP}	15	-	15	-	20	-	ns	
Write Recovery Time	t_{WR}	3	-	3	-	3	-	ns	
Write to Output in High Z	t_{WHZ}	5	-	5	-	5	-	ns	
Write to Output in High Z	t_{WHZ}	0	8	0	10	0	15	ns	(4,5)
Data to Write Time Overlap	t_{DW}	8	-	10	-	15	-	ns	
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns	
Output Active from End of Write	t_{OW}	5	-	5	-	5	-	ns	

Write Cycle No.1 Timing Waveform

Write Cycle No.2 Timing Waveform



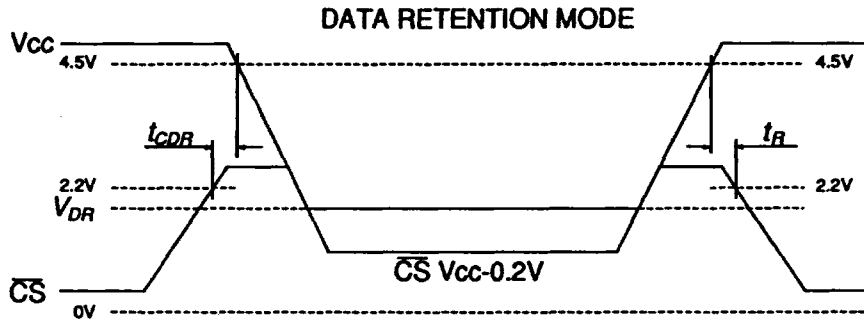
AC Characteristics Notes

- Note: (1) A write occurs during the overlap (t_{WR}) of a low \overline{CS} and a low \overline{WE} .
- (2) \overline{OE} is continuously high. ($\overline{OE}=V_{IH}$)
- (3) t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of write cycle.
- (4) Transition is measured $\pm 500mV$ typical from steady state voltage, allowing for actual tester RC time constant.
- (5) At any given temperature and voltage condition, t_{LZ} is less than $t_{LZ'}$, and t_{OHZ} is less than $t_{OHZ'}$.

Low V_{CC} Data Retention Characteristics - L Version Only ($T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$)

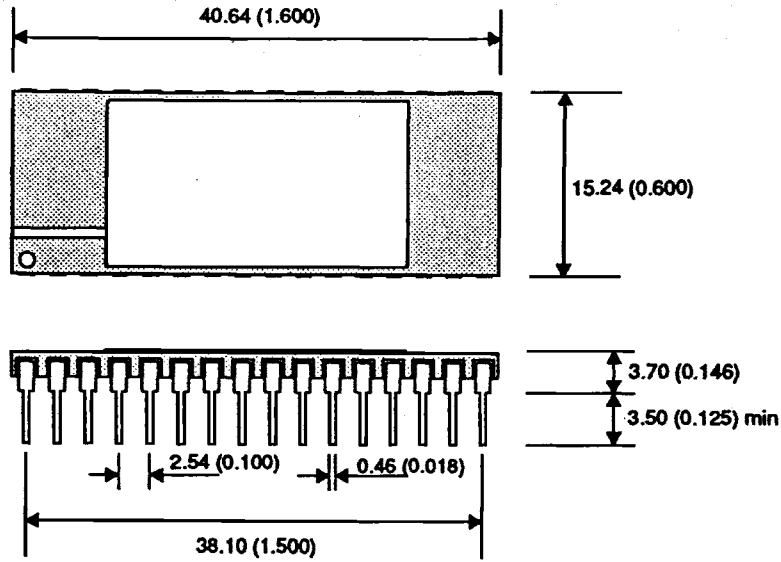
Parameter	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	-	-	V
Data Retention Current	I_{CCDR}	$V_{CC} = 3.0V, 0.2V \geq V_{IN} \geq 0V, \overline{CS} \geq V_{CC} - 0.2V$	-	-	1.5	mA
Chip Deselect to Data Retention	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	t_{RC}	-	-	ms

Low V_{CC} Data Retention Timing Waveform

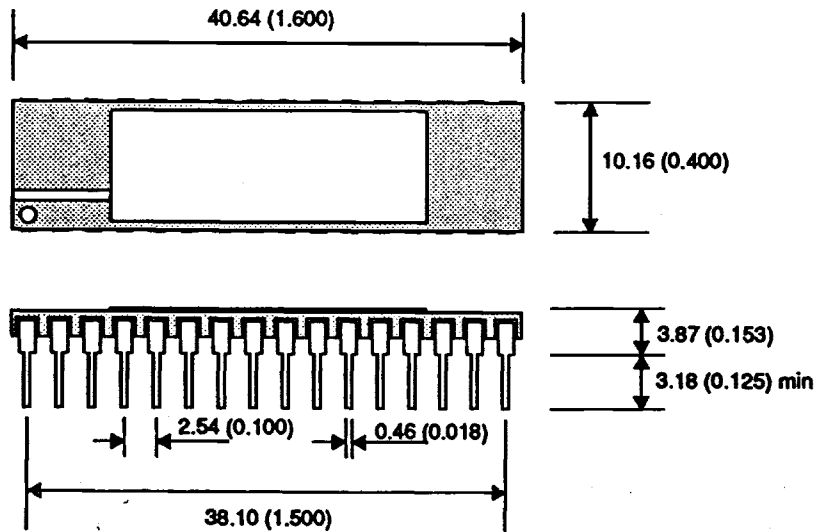


Package Details Dimensions in mm (inches). Tolerance on all dimensions ± 0.254 (0.01)

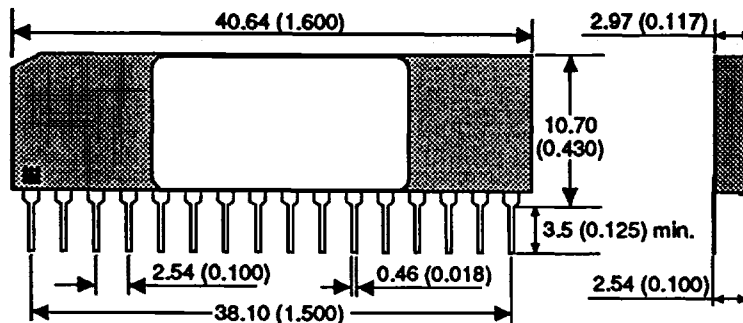
32 pin 0.6" Dual-In-Line (DIP) - 'SX' Package



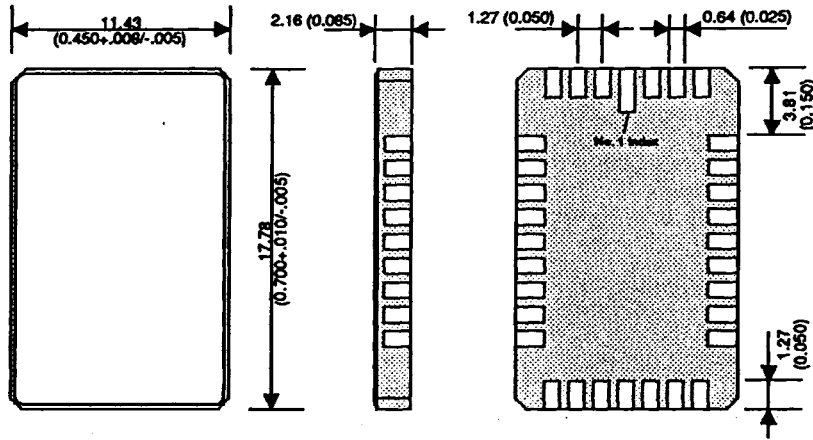
32 pin 0.4" Dual-In-Line (DIP) - 'KX' Package



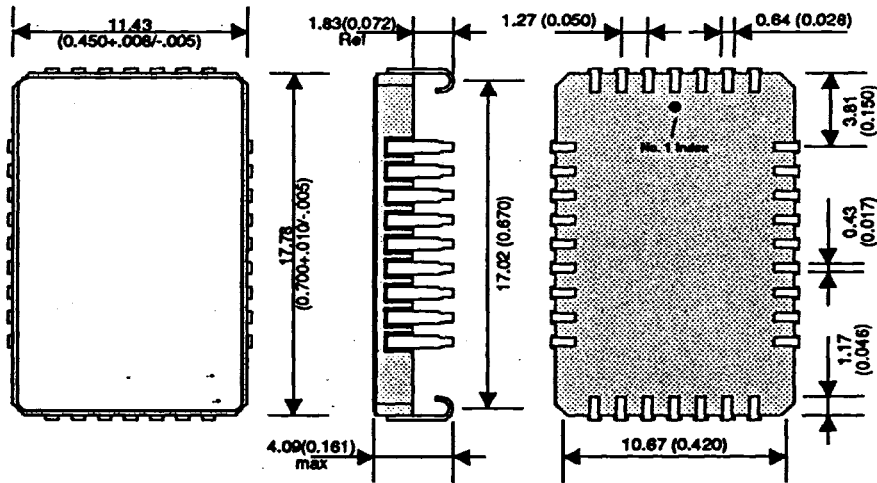
32 pin 0.1" Vertical-In-Line (VIL™) - 'VX' Package



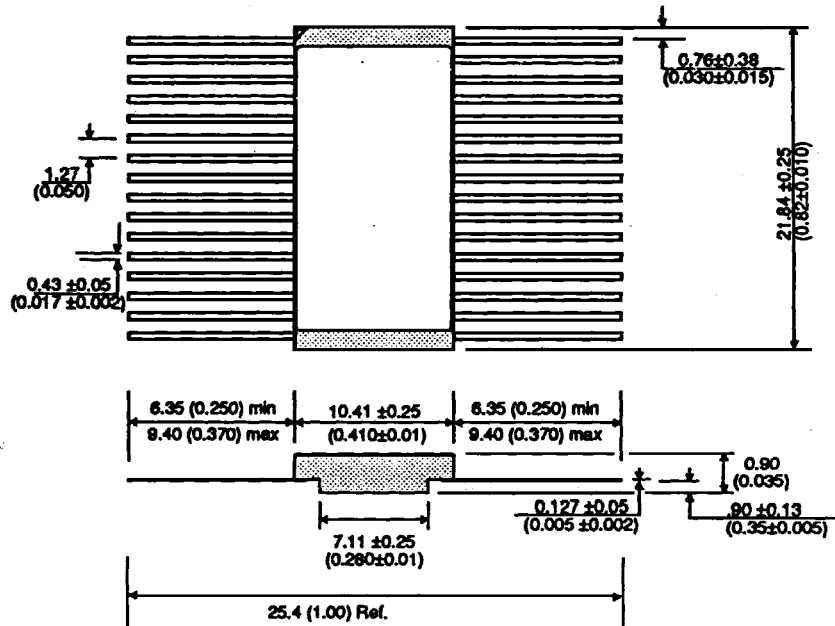
32 pin Extended Leadless Chip Carrier (LCC) - 'WX' Package



32 pin Extended 'J' Leaded Chip Carrier (JLCC) - 'JX' Package



32 pin Ceramic Flatpack - 'GX' Package



Ordering Information

MSM8128SLMB-020

	Speed	020 = 20 ns 025 = 25 ns 35 = 35 ns
	Temp. range/screening	Blank = Commercial I = Industrial M = Military MB = Processed in accordance with MIL-STD-883, Method 5004 non-compliant. MC = Compliant to MIL-STD-883
	Power Consumption	Blank = Standard Power L = Low Power
Package		SX = 32 pin 0.6" DIP KX = 32 pin 0.4" DIP VX = 32 pin 0.1" VIL GX = 32 lead Flatpack WX = 32 pad LCC JX = 32 Extended JLCC

Note: For more information regarding screening flows contact Mosaic Semiconductor Inc. for a 'Screening Flow Applications Note.'

mosaic

Mosaic
Semiconductor
Inc.

The policy of the company is one of continuous development and while the information presented in this data sheet is believed to be accurate, no liability is assumed for any data contained within. The company reserves the right to make changes without notice at any time.