SN74LS161A, SN74LS163A

BCD Decade Counters/ 4-Bit Binary Counters

The LS161A/163A are high-speed 4-bit synchronous counters. They are edge-triggered, synchronously presettable, and cascadable MSI building blocks for counting, memory addressing, frequency division and other applications. The LS161A and LS163A count modulo 16 (binary).

The LS161A has an asynchronous Master Reset (Clear) input that overrides, and is independent of, the clock and all other control inputs. The LS163A has a Synchronous Reset (Clear) input that overrides all other control inputs, but is active only during the rising clock edge.

	Binary (Modulo 16)
Asynchronous Reset	LS161A
Synchronous Reset	LS163A

- Synchronous Counting and Loading
- Two Count Enable Inputs for High Speed Synchronous Expansion
- Terminal Count Fully Decoded
- Edge-Triggered Operation
- Typical Count Rate of 35 MHz
- ESD > 3500 Volts

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			–0.4	mA
I_{OL}	Output Current – Low			8.0	mA

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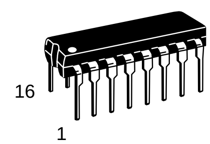
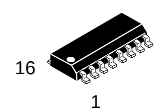
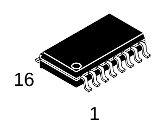
LOW POWER SCHOTTKY



PLASTIC N SUFFIX CASE 648



SOIC D SUFFIX CASE 751B



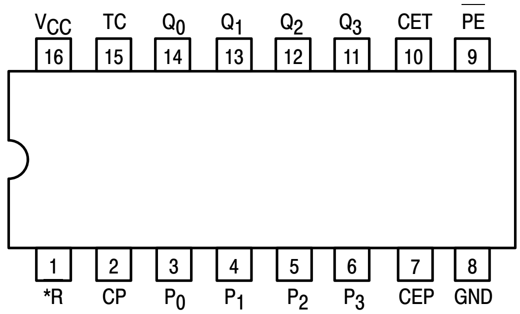
SOEIAJ M SUFFIX CASE 966

ORDERING INFORMATION

Device	Package	Shipping
SN74LS161AN	16 Pin DIP	2000 Units/Box
SN74LS161AD	SOIC–16	38 Units/Rail
SN74LS161ADR2	SOIC–16	2500/Tape & Reel
SN74LS161AM	SOEIAJ–16	See Note 1
SN74LS161AMEL	SOEIAJ–16	See Note 1
SN74LS163AN	16 Pin DIP	2000 Units/Box
SN74LS163AD	SOIC–16	38 Units/Rail
SN74LS163ADR2	SOIC–16	2500/Tape & Reel
SN74LS163AM	SOEIAJ–16	See Note 1
SN74LS163AMEL	SOEIAJ–16	See Note 1

1. For ordering information on the EIAJ version of the SOIC package, please contact your local ON Semiconductor representative.

CONNECTION DIAGRAM DIP (TOP VIEW)



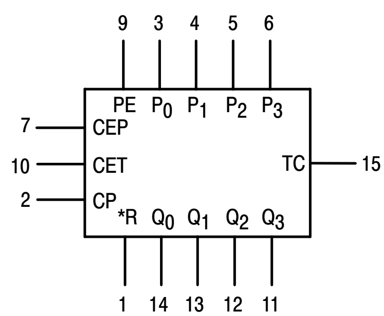
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

*MR for LS161A
*SR for LS163A

PIN NAMES		LOADING (Note a) HIGH	LOW
PE	Parallel Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
$P_0 - P_3$	Parallel Inputs	0.5 U.L.	0.25 U.L.
CEP	Count Enable Parallel Input	0.5 U.L.	0.25 U.L.
CET	Count Enable Trickle Input	1.0 U.L.	0.5 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
MR	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
SR	Synchronous Reset (Active LOW) Input	1.0 U.L.	0.5 U.L.
$Q_0 - Q_3$	Parallel Outputs	10 U.L.	5 U.L.
TC	Terminal Count Output	10 U.L.	5 U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

LOGIC SYMBOL

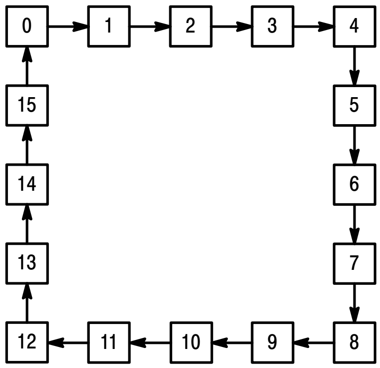


V_{CC} = PIN 16
GND = PIN 8

*MR for LS161A
*SR for LS163A

STATE DIAGRAM

LS161A • LS163A



LOGIC EQUATIONS

Count Enable = CEP • CET • PE
TC for LS161A & LS163A = CET • Q_0 • Q_1 • Q_2 • Q_3
Preset = PE • CP + (rising clock edge)
Reset = MR (LS161A)
Reset = SR • CP + (rising clock edge)
(LS163A)

FUNCTIONAL DESCRIPTION

The LS161A/163A are 4-bit synchronous counters with a synchronous Parallel Enable (Load) feature. The counters consist of four edge-triggered D flip-flops with the appropriate data routing networks feeding the D inputs. All changes of the Q outputs (except due to the asynchronous Master Reset in the LS161A) occur as a result of, and synchronous with, the LOW to HIGH transition of the Clock input (CP). As long as the set-up time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs.

Three control inputs — Parallel Enable (PE), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — select the mode of operation as shown in the tables below. The Count Mode is enabled when the CEP, CET, and PE inputs are HIGH. When the PE is LOW, the counters will synchronously load the data from the parallel inputs into the flip-flops on the LOW to HIGH transition of the clock. Either the CEP or CET can be used to inhibit the count sequence. With the PE held HIGH, a LOW on either the CEP or CET inputs at least one set-up time prior to the LOW to HIGH clock transition will cause the existing output states to be retained. The AND feature of the two Count Enable inputs (CET•CEP) allows synchronous cascading without external gating and without delay accumulation over any practical number of bits or digits.

The Terminal Count (TC) output is HIGH when the Count Enable Trickle (CET) input is HIGH while the counter is in its maximum count state (HLLH for the BCD counters, HHHH for the Binary counters). Note that TC is fully decoded and will, therefore, be HIGH only for one count state.

The LS161A and LS163A count modulo 16 following a binary sequence. They generate a TC when the CET input is HIGH while the counter is in state 15 (HHHH). From this state they increment to state 0 (LLLL).

The Master Reset (MR) of the LS161A is asynchronous. When the MR is LOW, it overrides all other input conditions and sets the outputs LOW. The MR pin should never be left open. If not used, the MR pin should be tied through a resistor to V_{CC}, or to a gate output which is permanently set to a HIGH logic level.

The active LOW Synchronous Reset (SR) input of the LS163A acts as an edge-triggered control input, overriding CET, CEP and PE, and resetting the four counter flip-flops on the LOW to HIGH transition of the clock. This simplifies the design from race-free logic controlled reset circuits, e.g., to reset the counter synchronously after reaching a predetermined value.

MODE SELECT TABLE

*SR	PE	CET	CEP	Action on the Rising Clock Edge ( )
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD ($P_n \rightarrow Q_n$)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

*For the LS163A only.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

LS161A

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage		–0.65	–1.5	V	V_{CC} = MIN, I_{IN} = –18 mA	
V_{OH}	Output HIGH Voltage	2.7	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
			0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current MR, Data, CEP, Clock PE, CET			20 40	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	MR, Data, CEP, Clock PE, CET			0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current MR, Data, CEP, Clock PE, CET			–0.4 –0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 2)	–20		–100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW			31 32	mA	V_{CC} = MAX	

2. Not more than one output should be shorted at a time, nor for more than 1 second.

LS163A

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage		–0.65	–1.5	V	V_{CC} = MIN, I_{IN} = –18 mA	
V_{OH}	Output HIGH Voltage	2.7	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
			0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current Data, CEP, Clock PE, CET, SR			20 40	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	Data, CEP, Clock PE, CET, SR			0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current Data, CEP, Clock, PE, SR CET			–0.4 –0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 3)	–20		–100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW			31 32	mA	V_{CC} = MAX	

3. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
f_{MAX}	Maximum Clock Frequency	25	32		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay Clock to TC		20 18	35 35	ns	
t_{PLH} t_{PHL}	Propagation Delay Clock to Q		13 18	24 27	ns	
t_{PLH} t_{PHL}	Propagation Delay CET to TC		9.0 9.0	14 14	ns	
t_{PHL}	$\overline{\text{MR}}$ or $\overline{\text{SR}}$ to Q		20	28	ns	

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
t_WCP	Clock Pulse Width Low	25			ns	V_{CC} = 5.0 V
t_W	$\overline{\text{MR}}$ or $\overline{\text{SR}}$ Pulse Width	20			ns	
t_s	Setup Time, other*	20			ns	
t_s	Setup Time $\overline{\text{PE}}$ or $\overline{\text{SR}}$	25			ns	
t_h	Hold Time, data	3			ns	
t_h	Hold Time, other	0			ns	
t_{rec}	Recovery Time $\overline{\text{MR}}$ to CP	15			ns	

*CEP, CET, or DATA

DEFINITION OF TERMS

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

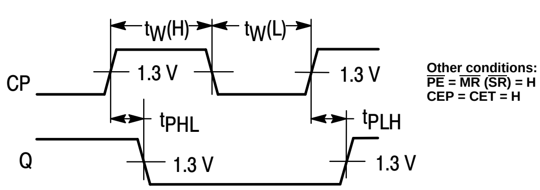


Figure 1. Clock to Output Delays, Count Frequency, and Clock Pulse Width

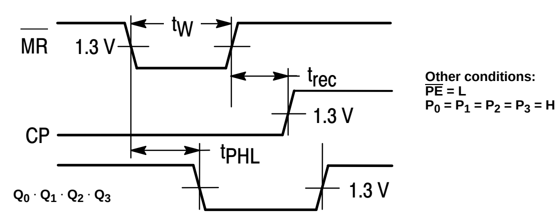


Figure 2. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time

AC WAVEFORMS (continued)

COUNT ENABLE TRICKLE INPUT TO TERMINAL COUNT OUTPUT DELAYS

The positive TC pulse occurs when the outputs are in the (Q_0 • Q_1 • Q_2 • Q_3) state for the LS161 and LS163.

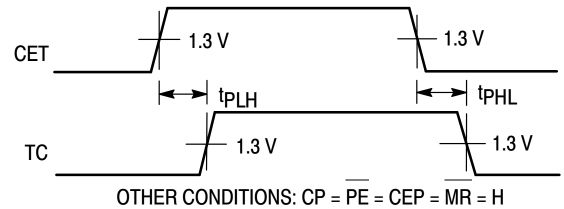


Figure 3.

CLOCK TO TERMINAL COUNT DELAYS

The positive TC pulse is coincident with the output state (Q_0 • Q_1 • Q_2 • Q_3) for the LS161 and LS163.

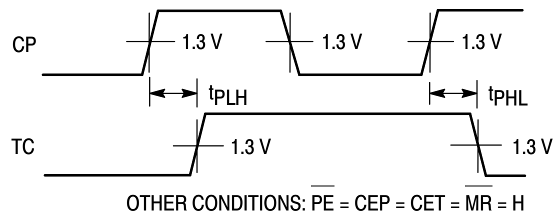


Figure 4.

SETUP TIME (t_S) AND HOLD TIME (t_h) FOR PARALLEL DATA INPUTS

The shaded areas indicate when the input is permitted to change for predictable output performance.

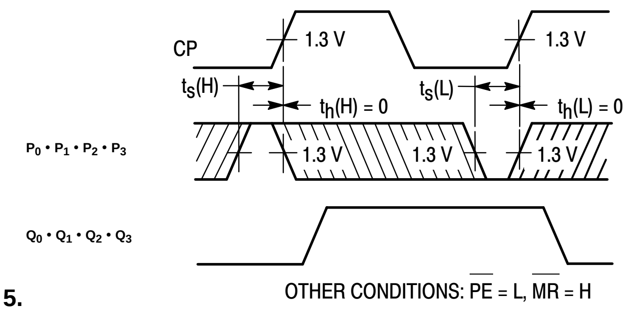


Figure 5.

SETUP TIME (t_S) AND HOLD TIME (t_h) FOR COUNT ENABLE (CEP) AND (CET) AND PARALLEL ENABLE (PE) INPUTS

The shaded areas indicate when the input is permitted to change for predictable output performance.

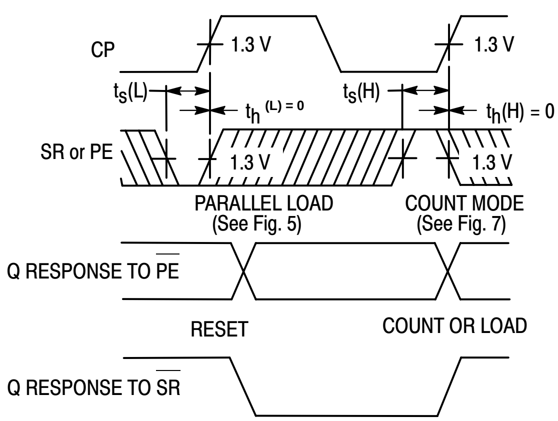


Figure 6.

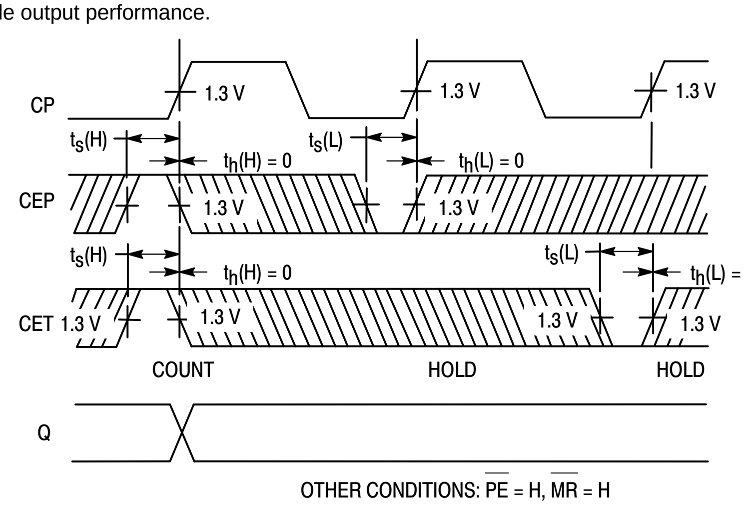
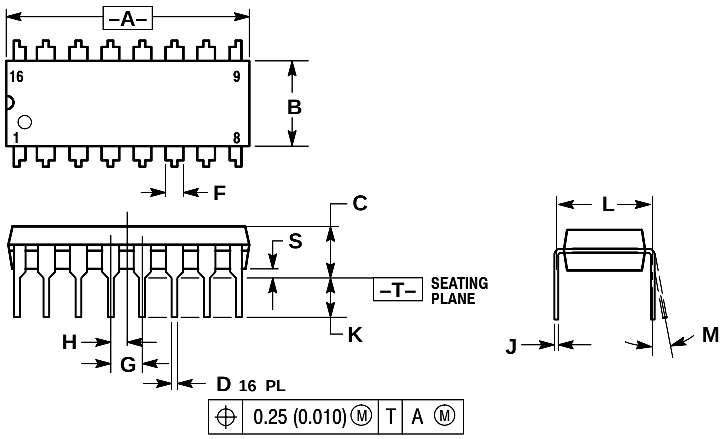


Figure 7.

PACKAGE DIMENSIONS

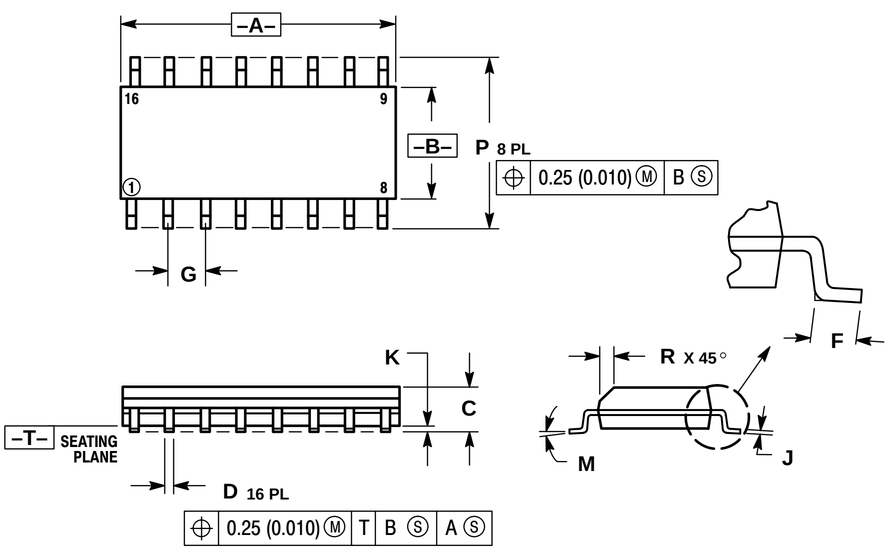
N SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J

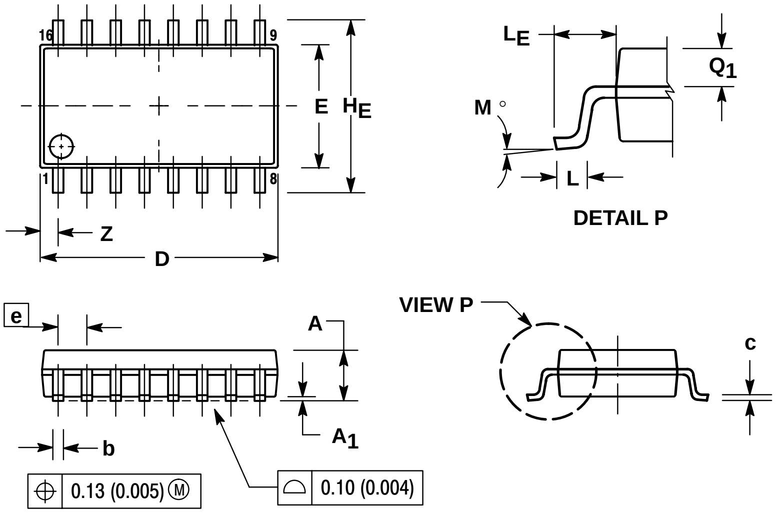


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

M SUFFIX
SOEIAJ PACKAGE
CASE 966–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
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Email: r14525@onsemi.com

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