SRM2267C45/55

HIGH SPEED CMOS 16K-BIT STATIC RAM

- **Access Time 45ns/55ns**
- **16,384 Words×1 Bit Asynchronous**
- **Low Supply Current**

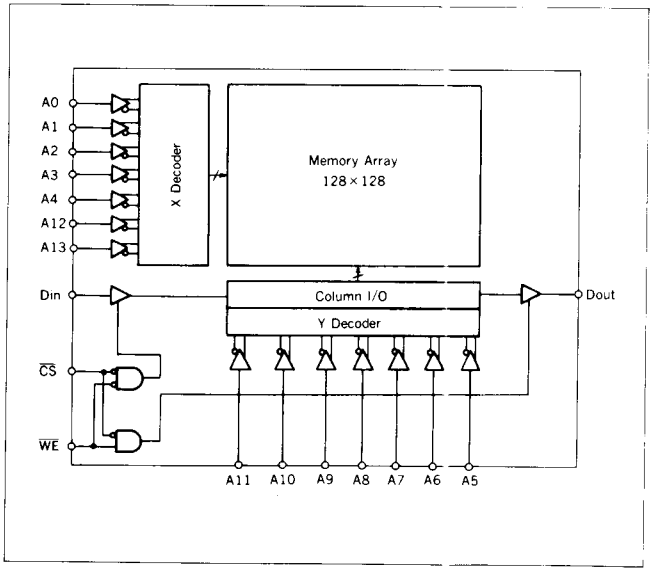
■DESCRIPTION

The SRM2267C45/55 is a 16,384 words×1 bit asynchronous, static, random access memory on a monolithic CMOS chip. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.

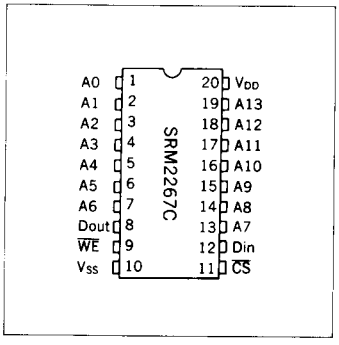
■FEATURES

- ●Fast access time ····· SRM2267C45 45ns (Max)
  SRM2267C55 55ns (Max)
- ●Low supply current ····· Standby : 20μA (Typ)
  Operation : 40mA (Typ)
- ●Completely static ····· No clock required
- ●Single power supply ····· 5V±10%
- ●TTL compatible inputs and outputs
- ●3-state output with wired-OR capability
- ●Package ····· 20-pin DIP (plastic)

■BLOCK DIAGRAM



■PIN CONFIGURATION



■PIN DESCRIPTION

A0 to A13	Address Input
WE	Write Enable
CS	Chip Select
Din	Data Input
Dout	Data output
VDD	Power Supply (5V)
Vss	Power Supply (0V)

■ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Input voltage*	V_I	−0.5 to 7.0	V
Power dissipation	P_D	1.0	W
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−55 to 125	°C
Temperature under bias	T_{bias}	−10 to 85	°C

*V_I (Min) = −3.5V (Pulse width 20ns)

■DC RECOMMENDED OPERATING CONDITIONS

(V_{SS}=0V, Ta=0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	—	4.5	5.0	5.5	V
	V_{SS}	—	0	0	0	V
Input voltage	V_{IH}	—	2.2	—	6.0	V
	V_{IL}	—	−3.0*	—	0.8	V

*Pulse width 20ns, DC : V_{IL} (Min) = −0.5V

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ*1	Max	Unit
Input leakage current	I_{LI}	V_I=0 to V_{DD}	−2.0	—	2.0	μA
Standby supply current	I_{DDS}	$\overline{CS}$=V_{IH}	—	10	20	mA
	I_{DDSI}	$\overline{CS}$≧V_{DD}−0.2V, V_I≦0.2V or V_I≧V_{DD}−0.2V	—	0.02	2.0	mA
Operating supply current	I_{DDO}	$\overline{CS}$=V_{IL}, Output Open	—	40	80	mA
Output leakage current	I_{LO}	$\overline{CS}$=V_{IH}, V_O=0 to V_{DD}	−2.0	—	2.0	μA
High level output voltage	V_{OH}	I_{OH}=−4.0mA	2.4	—	—	V
Low level output voltage	V_{OL}	I_{OL}=8.0mA	—	—	0.4	V

*1 Typical values are for Ta=25°C and V_{DD}=5.0V

●Terminal Capacitance*2

(f=1.0MHz, Ta=25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_I	V_I=0V	—	—	5	pF
Output capacitance	C_O	V_O=0V	—	—	7	pF

*2 This parameter is sampled and not 100% tested

●AC Electrical Characteristics

○Read Cycle

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

Parameter	Symbol	Conditions	SRM2267C$_{45}$		SRM2267C$_{55}$		Unit
			Min	Max	Min	Max	
Read cycle time	t_{RC}	*3	45	—	55	—	ns
Address access time	t_{ACC}		—	45	—	55	ns
Chip select access time	t_{ACS}		—	45	—	55	ns
Chip enable output set time	t_{CLZ}	*4, *5, *6	5	—	5	—	ns
Chip disable output floating	t_{CHZ}		0	30	0	30	ns
Chip selection to power up time	t_{PU}		0	—	0	—	ns
Chip deselection to power down time	t_{PD}		—	30	—	30	ns
Output hold time	t_{OH}		5	—	5	—	ns

*3 All Read Cycle timings are referenced from last valid address to the first transitioning address.
*4 At any given temperature and voltage condition, t_{CHZ} Max is less than t_{CLZ} Min both for a given device and from device to device.
*5 Transition is measured ±500 mV from steady state voltage with specified loading in Load B.
*6 This parameter is sampled and not 100% tested.

○Write Cycle

(V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = 0 to 70°C)

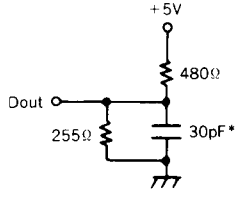
Parameter	Symbol	Conditions	SRM2267C$_{45}$		SRM2267C$_{55}$		Unit
			Min	Max	Min	Max	
Write cycle time	t_{WC}	*7	45	—	55	—	ns
Chip select time	t_{CW}		40	—	50	—	ns
Address enable time	t_{AW}		40	—	50	—	ns
Address setup time	t_{AS}		0	—	0	—	ns
Write pulse width	t_{WP}		25	—	35	—	ns
Address hold time	t_{WR}		0	—	0	—	ns
Input data setup time	t_{DW}		25	—	25	—	ns
Input data hold time	t_{DH}		0	—	0	—	ns
$\overline{WE}$ output floating	t_{WHZ}	*8, *9	0	25	0	25	ns
$\overline{WE}$ output setup time	t_{OW}		0	—	0	—	ns

*7 All Write Cycle timings are referenced from the last valid address to the first transitioning address.
*8 Transition is measured ±500mV from steady state voltage with specified loading in Load B.
*9 This parameter is sampled and not 100% tested.

○Test Conditions

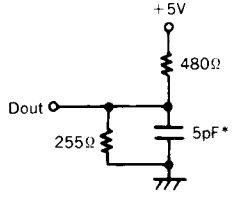
1. Input pulse levels : V_{SS} to 3.0V
2. Input rise and fall times : 5 ns
3. Input timing reference levels : 1.5V
4. Output reference levels : 1.5V
5. Output load : see figure

Output Load A



*Including scope and jig.

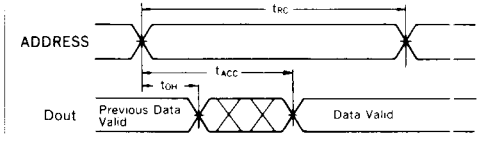
Output Load B
(for t_{CHZ}, t_{CLZ}, t_{WHZ} & t_{OW})



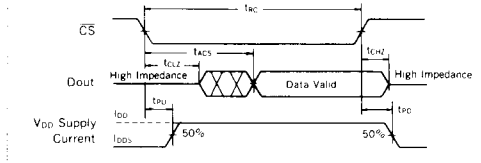
*Including scope and jig.

●Timing Chart

○Read Cycle (1)*10, *11

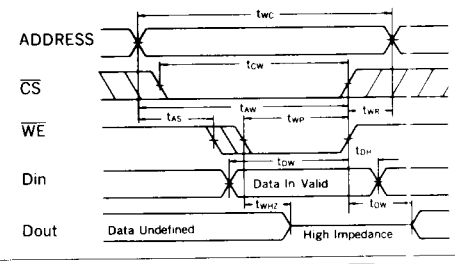


○Read Cycle (2)*10, *12

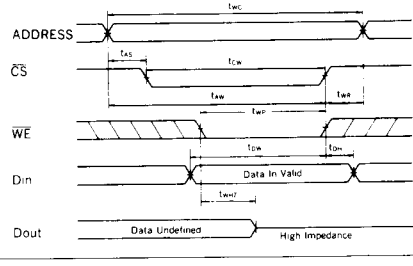


*10 $\overline{WE}$ is High for Read Cycle.
*11 Device is continuously selected, $\overline{CS}$ = V_{IL}.
*12 Addresses valid to or coincident with $\overline{CS}$ transition low.

○Write Cycle(1)($\overline{WE}$ Control)*13



○Write Cycle(2)($\overline{CS}$ Control)*13



*13 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.

■FUNCTIONS

●Truth Table

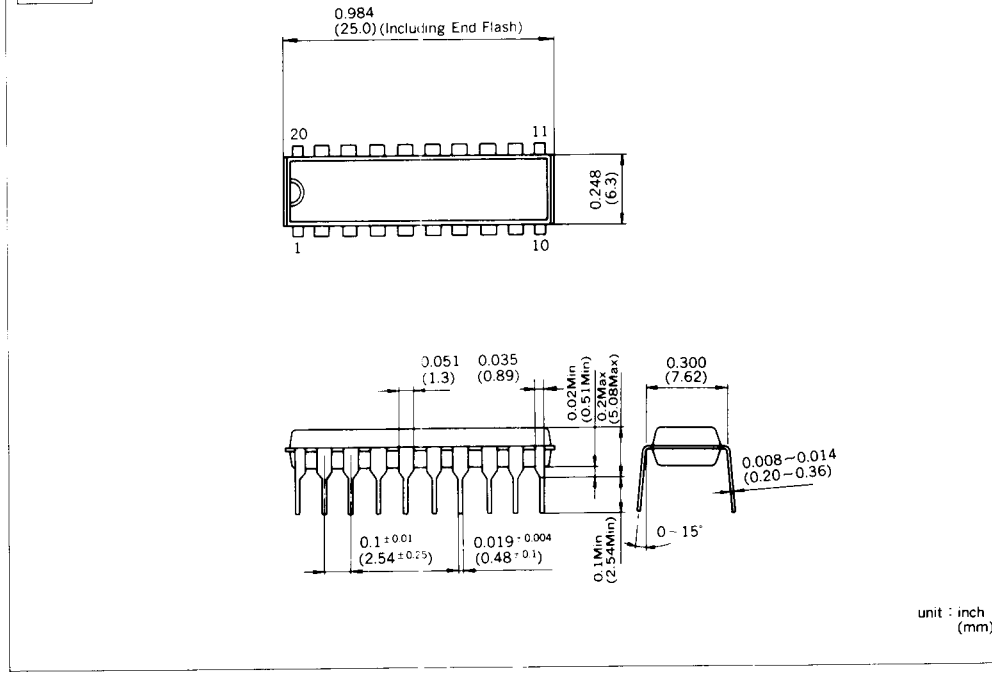
$\overline{CS}$	$\overline{WE}$	A0 to A13	Data I/O	Mode	I_{DD}
H	X	—	Hi - Z	Unselected	I_{DDS}, I_{DDSI}
L	H	Stable	Output data	Read	I_{DDO}
L	L	Stable	Input data	Write	I_{DDO}

x : "H" or "L", — : "H", "L" or "Hi-Z"

■PACKAGE DIMENSIONS

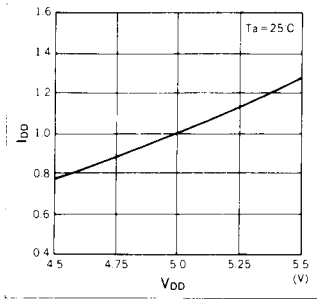
C20-9

20-pin DIP

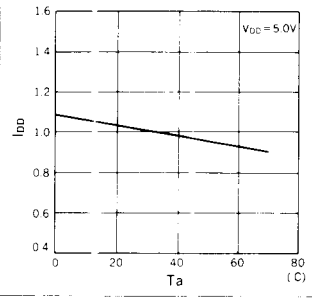


■CHARACTERISTICS CURVES

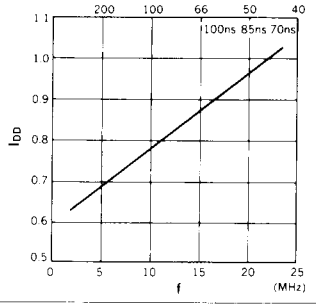
Normalized I_{DD}—V_{DD}



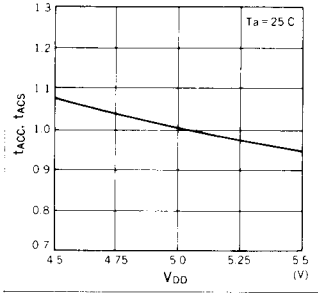
Normalized I_{DD}—Ta



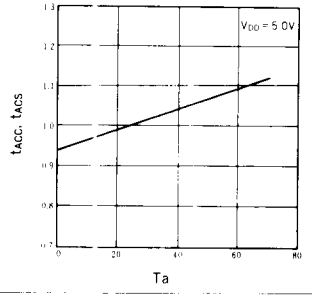
Normalized I_{DD}—f



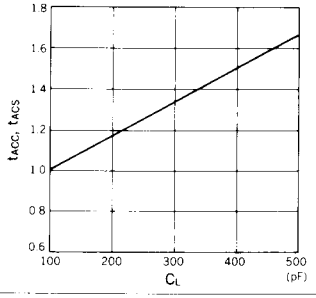
Normalized t_{ACC}, t_{ACS}—V_{DD}



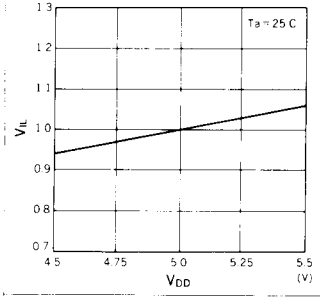
Normalized t_{ACC}, t_{ACS}—Ta



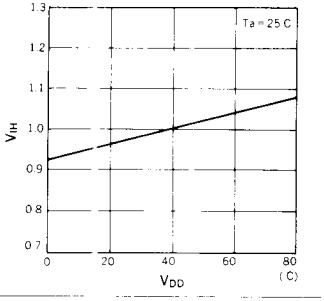
Normalized t_{ACC}, t_{ACS}—C_L



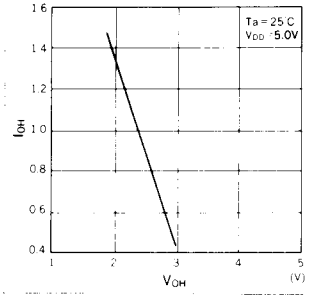
Normalized V_{IL}—V_{DD}



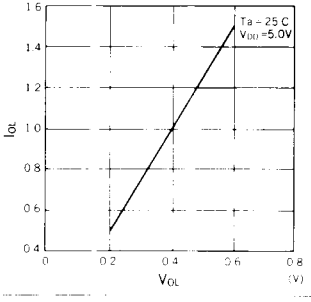
Normalized V_{IH}—V_{DD}



Normalized I_{OH}—V_{OH}

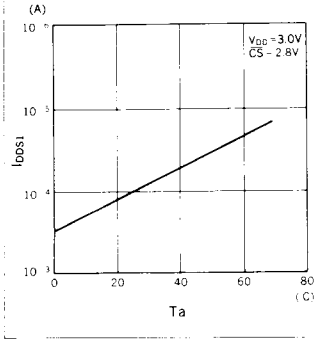


Normalized I_{OL}—V_{OL}

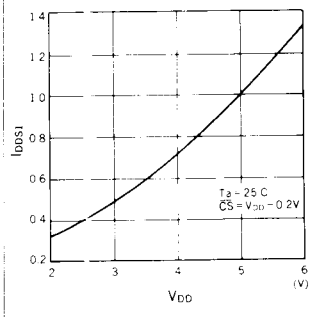


■CHARACTERISTICS CURVES (Continued)

I_{DDS1}—Ta



Normalized I_{DDS1}—V_{DD}



Normalized I_{DDS}—V_I