

74109, LS109A Flip-Flops

Dual J-K Positive Edge-Triggered Flip-Flop
Product Specification

Logic Products

DESCRIPTION

The '109 is dual positive edge-triggered JK-type flip-flop featuring individual J, K, Clock, Set and Reset inputs; also complementary Q and Q outputs.

Set (\bar{S}_D) and Reset (\bar{R}_D) are asynchronous active LOW inputs and operate independently of the Clock input.

The J and K are edge-triggered inputs which control the state changes of the flip-flops as described in the Mode Select-Truth Table.

The J and K inputs must be stable just one set-up time prior to the LOW-to-HIGH transition of the Clock for predictable operation. The JK design allows operation as a D flip-flop by tying the J and K inputs together.

Although the Clock input is level sensitive, the positive transition of the Clock pulse between the 0.8V and 2.0V levels should be equal to or less than the Clock to output delay time for reliable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74109	33MHz	9mA
74LS109A	33MHz	4mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74109N, N74LS109AN
Plastic SO	N74LS109D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

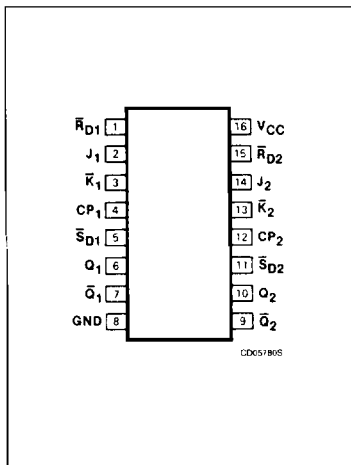
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
CP	Clock input	2ul	1LSul
\bar{R}_D	Reset input	4ul	2LSul
\bar{S}_D	Set input	2ul	2LSul
J, K	Data inputs	1ul	1LSul
Q, \bar{Q}	Outputs	10ul	10LSul

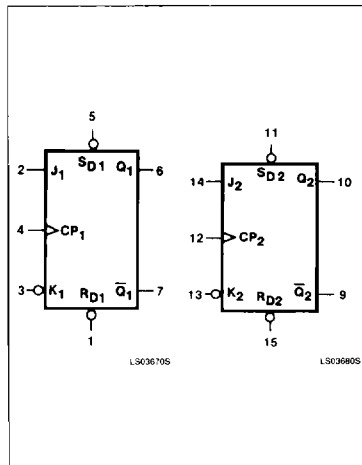
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

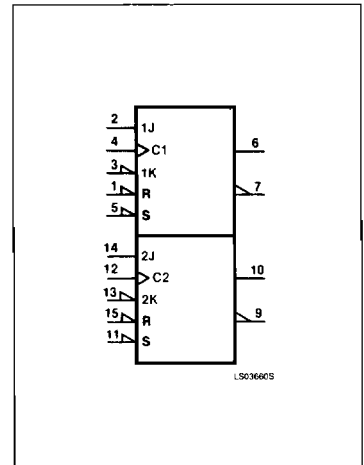
PIN CONFIGURATION



LOGIC SYMBOL



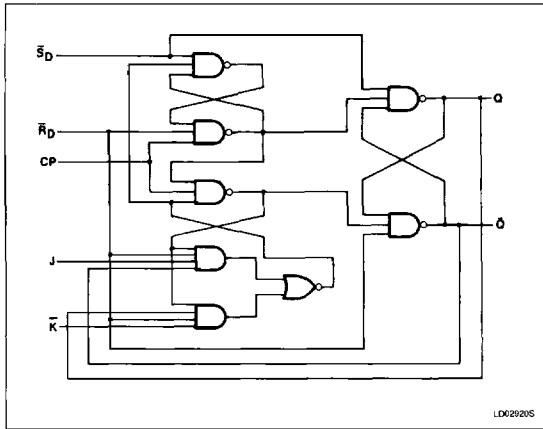
LOGIC SYMBOL (IEEE/IEC)



Flip-Flops

74109, LS109A

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	\bar{S}_D	\bar{R}_D	CP	J	K	Q	\bar{Q}
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset (clear)	H	L	X	X	X	L	H
Undetermined (note)	L	L	X	X	X	H	H
Toggle	H	H	\uparrow	h	l	\bar{q}	q
Load "0" (reset)	H	H	\uparrow	l	l	L	H
Load "1" (set)	H	H	\uparrow	h	h	H	L
Hold "no change"	H	H	\uparrow	l	h	q	\bar{q}

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH Clock transition.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH Clock transition.
 X = Don't care.
 q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH Clock transition.
 \uparrow = LOW-to-HIGH Clock transition.

NOTE:

Both outputs will be HIGH while both \bar{S}_D and \bar{R}_D are LOW, but the output states are unpredictable if \bar{S}_D and \bar{R}_D go HIGH simultaneously.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT
	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18	mA
I _{OH} HIGH-level output current			-800			-400	μA
I _{OL} LOW-level output current			16			8	mA
T _A Operating free-air temperature	0		70	0		70	°C

Flip-Flops

74109, LS109A

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74109			74LS109			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4	0.35	0.5	V
		I _{OL} = 4mA (74LS)				0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5		-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0			mA
		V _I = 7.0V	J, \bar{K} inputs				0.1	mA
			\bar{R}_D , \bar{S}_D inputs				0.2	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	J, \bar{K} inputs		40			μ A
			\bar{R}_D inputs		160			μ A
			\bar{S}_D , CP inputs		80			μ A
		V _I = 2.7V	J, \bar{K} inputs				20	μ A
			\bar{R}_D , \bar{S}_D inputs				40	μ A
			CP inputs				20	μ A
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	J, \bar{K} inputs		-1.6		-0.4	mA	
		\bar{R}_D inputs		-4.8		-0.8	mA	
		\bar{S}_D inputs		-3.2		-0.8	mA	
		CP inputs		-3.2		-0.4	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-30		-85	-20		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		9	30		4	8	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs HIGH in turn.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		C _L = 15pF, R _L = 400 Ω		C _L = 15pF, R _L = 2k Ω		
		Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	25		25		MHz
t _{PLH} Propagation delay	Waveform 1		16		25	ns
t _{PHL} Clock to output			28		40	
t _{PLH} Propagation delay	Waveform 2		15		25	ns
t _{PHL} Reset to output			25		40	
t _{PLH} Propagation delay	Waveform 2		15		25	ns
t _{PHL} Set to output			35		40	

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

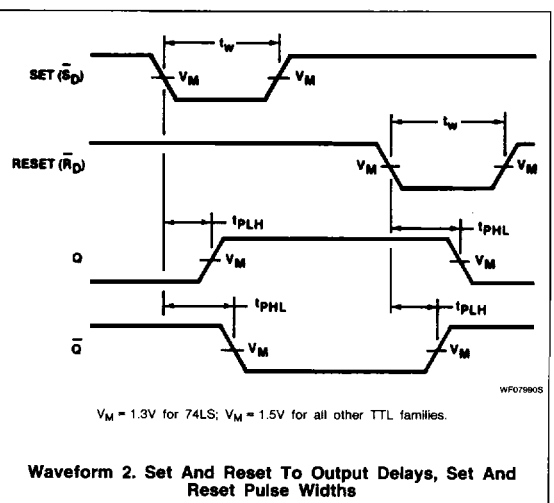
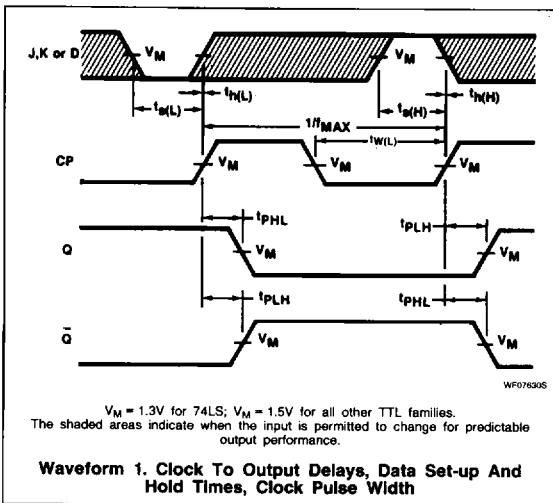
Flip-Flops

74109, LS109A

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		Min	Max	Min	Max	
$t_{w(H)}$ Clock pulse width (HIGH)	Waveform 1	20		25		ns
$t_{w(L)}$ Clock pulse width (LOW)	Waveform 1	20		15		ns
$t_{w(L)}$ Set or reset pulse width (LOW)	Waveform 2	20		25		ns
t_s Set-up time J or K to clock	Waveform 1	10		20		ns
t_h Hold time J or K to clock	Waveform 1	6.0		5.0		ns

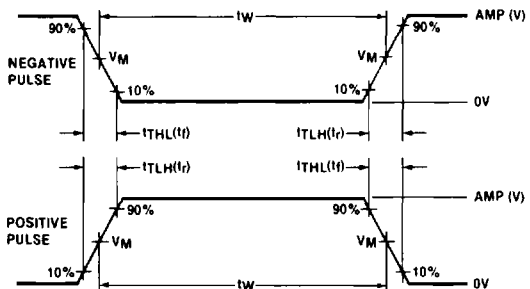
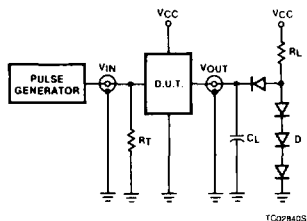
AC WAVEFORMS



Flip-Flops

74109, LS109A

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns