Integrated Circuit Systems, Inc.

# ICS9159-14

# Frequency Generator and Integrated Buffer for PENTIUM™

## General Description

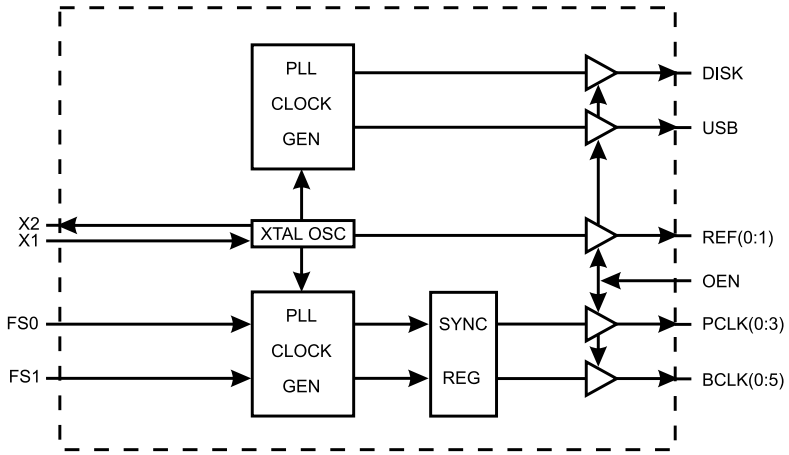
The **ICS9159-14** generates all clocks required for high speed RISC or CISC microprocessor systems such as 486, Pentium, PowerPC,™ etc. Four different reference frequency multiplying factors are externally selectable with smooth frequency transitions. These multiplying factors can be customized for specific applications.

High drive BCLK outputs provide typically greater than 1V/ns slew rate into 30pF loads. PCLK outputs provide typically better than 1V/ns slew rate into 20pF loads while maintaining ±5% duty cycle.

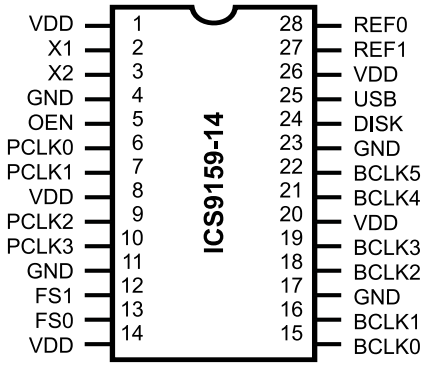
## Features

- Generates up to four processor and six bus clocks, plus disk, USB and reference clocks
- Synchronous clocks skew matched to 250ps window on PCLKs and 500ps window on BCLKs
- 3.0V - 5.5V supply range
- 28-pin SOIC package

## Block Diagram




## Pin Configuration




**28-Pin SOIC**

## Functionality

| FS1 | FS0 | *VCO | X1, REF (MHz) | CPU (MHz) |
|---|---|---|---|---|
| 0 | 0 | 118/17 x X1 | 14.318 | 50 (49.7) |
| 0 | 1 | 65/7 x X1 | 14.318 | 66.6 (66.5) |
| 1 | 0 | 92/11 x X1 | 14.318 | 60 (59.9) |
| 1 | 1 | 69/9 x X1 | 14.318 | 55 (54.9) |

*VCO range is limited from 60 - 200 MHz.

| PCLK(0:3) | BCLK(0:5) | USB | DISK |
|---|---|---|---|
| VCO/2 | PCLK/2 | 48 MHz | 24 MHz |

All frequencies in MHz, assuming 14.318 MHz input.

Pentium is a trademark of Intel Corporation.
PowerPC is a trademark of Motorola Corporation.

## Pin Descriptions

| PIN NUMBER | PIN NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 1, 8, 26 | VDD | PWR | Power for logic, CPU and fixed frequency output buffers. |
| 2 | X1 | IN | XTAL or external reference frequency input. This input includes XTAL load capacitance and feedback bias for a 12 - 16 MHz crystal, nominally 14.31818 MHz. |
| 3 | X2 | OUT | XTAL output which includes XTAL load capacitance. |
| 4, 11, 23 | GND | PWR | Ground for logic, CPU and fixed frequency output buffers. |
| 6, 7, 9, 10 | PCLK(0:3) | OUT | Processor clock outputs which are a multiple of the input reference frequency as shown in the table above. |
| 13, 12 | FS(0:1) | IN | Frequency multiplier select pins. See table above. These inputs have internal pull-up devices. |
| 14, 20 | VDD | PWR | Power for BCLK output buffers. |
| 15, 16, 18 19, 21, 22 | BCLK(0:5) | OUT | Bus clock outputs are fixed at one half the PCLK frequency. |
| 17 | GND | PWR | Ground for BCLK output buffers. |
| 5 | OEN | IN | OEN tristates all outputs when low. This input has an internal pull-up device. 24 DISK OUT The DISK controller clock is fixed at 24 MHz (with 14.318 MHz input). |
| 25 | USB | OUT | The USB clock is fixed at 48 MHz (with 14.318 MHz input). |
| 28, 27 | REF(0:1) | OUT | REF is a buffered copy of the crystal oscillator or reference input clock, nominally 14.31818 MHz. |

## Absolute Maximum Ratings

Supply Voltage ..... 7.0 V

Logic Inputs ..... GND –0.5 V to $V_{DD}$ +0.5 V

Ambient Operating Temperature ..... 0°C to +70°C

Storage Temperature ..... –65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## Electrical Characteristics at 3.3V

$V_{DD}$ = 3.0 – 3.7 V, $T_A$ = 0 – 70° C unless otherwise stated

| DC Characteristics | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
| Input Low Voltage | VIL | | - | - | 0.2VDD | V |
| Input High Voltage | VIH | | 0.7VDD | - | - | V |
| Input Low Current | IIL | VIN=0V | -28.0 | -10.5 | - | mA |
| Input High Current | IIH | VIN=VDD | -5.0 | - | 5.0 | mA |
| Output Low Current[1] | IOL | VOL=0.8V; for CPUs & BUSes | 30.0 | 47.0 | - | mA |
| Output High Current[1] | IOH | VOH=2.0V; for CPUs & BUSes | - | -66.0 | -42.0 | mA |
| Output Low Current[1] | IOL | VOL=0.8V; for fixed CLKs | 25.0 | 38.0 | - | mA |
| Output High Current[1] | IOH | VOH=2.0V; for fixed CLKs | - | -47.0 | -30.0 | mA |
| Output Low Voltage[1] | VOL | IOL=15mA; for CPUs & BUSes | - | 0.3 | 0.4 | V |
| Output High Voltage[1] | VOH | IOH=-30mA; for CPUs & BUSes | 2.4 | 2.8 | - | V |
| Output Low Voltage[1] | VOL | IOL=12.5mA; for fixed CLKs | - | 0.3 | 0.4 | V |
| Output High Voltage[1] | VOH | IOH=-20mA; for fixed CLKs | 2.4 | 2.8 | - | V |
| Supply Current | IDD | @66.5 MHz; all outputs unloaded | - | 55 | 110 | mA |

**Note 1:** Parameter is guaranteed by design and characterization. Not 100% tested in production.

## Electrical Characteristics at 3.3V

$V_{DD}$ = 3.1 – 3.7 V, $T_A$ = 0 – 70° C

| AC Characteristics | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
| Rise Time[1] | Tr1 | 20pF load, 0.8 to 2.0V CPU & BUS | - | 0.9 | 1.5 | ns |
| Fall Time[1] | Tf1 | 20pF load, 2.0 to 0.8V CPU & BUS | - | 0.8 | 1.4 | ns |
| Rise Time[1] | Tr2 | 20pF load, 20% to 80% CPU & BUS | - | 1.5 | 2.5 | ns |
| Fall Time[1] | Tf2 | 20pF load, 80% to 20% CPU & BUS | - | 1.4 | 2.4 | ns |
| Duty Cycle[1] | Dt | 20pF load @ VOUT=1.4V | 45 | 50 | 55 | % |
| Jitter, One Sigma[1] | Tj1s1 | CPU & BUS Clocks;<br>Load=20pF, FOUT>25 MHz | - | 50 | 150 | ps |
| Jitter, Absolute[1] | Tjab1 | CPU & BUS Clocks;<br>Load=20pF, FOUT>25 MHz | -250 | - | 250 | ps |
| Jitter, One Sigma[1] | Tj1s2 | Fixed CLK; Load=20pF | - | 1 | 3 | % |
| Jitter, Absolute[1] | Tjab2 | Fixed CLK; Load=20pF | -5 | 2 | 5 | % |
| Input Frequency[1] | Fi | | 12.0 | 14.318 | 16.0 | MHz |
| Logic Input Capacitance[1] | CIN | Logic input pins | - | 5 | - | pF |
| Crystal Oscillator Capacitance[1] | CINX | X1, X2 pins | - | 18 | - | pF |
| Power-on Time[1] | ton | From VDD=1.6V to 1 st crossing of 66.5 MHz<br>VDD supply ramp < 40ms | - | 2.5 | 4.5 | ms |
| Frequency Settling Time[1] | ts | From 1st crossing of acquisition to <<br>1% settling | - | 2.0 | 4.0 | ms |
| Clock Skew Window[1] | Tsk1 | CPU to CPU; Load=20pF; @1.4V | - | 150 | 250 | ps |
| Clock Skew Window[1] | Tsk2 | BUS to BUS; Load=20pF; @1.4V | - | 300 | 500 | ps |
| Clock Skew Window[1] | Tsk3 | CPU to BUS; Load=20pF; @1.4V | 1 | 2.6 | 5 | ns |

**Note 1:** Parameter is guaranteed by design and characterization. Not 100% tested in production.

## Electrical Characteristics at 5.0V

$V_{DD}$ = 4.5 – 5.5 V, $T_A$ = 0 – 70° C

| DC Characteristics | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
| Input Low Voltage | VIL | | - | - | 0.8 | V |
| Input High Voltage | VIH | | 2.4 | - | - | V |
| Input Low Current | IIL | VIN=0V | -45 | -15 | - | µA |
| Input High Current | IIH | VIN=VDD | -5.0 | - | 5.0 | µA |
| Output Low Current[1] | IOL | VOL=0.8V; for CPUs & BUSes | 36.0 | 62.0 | - | mA |
| Output High Current[1] | IOH | VOL=2.0V; for CPUs & BUSes | - | -152 | -90.0 | mA |
| Output Low Current[1] | IOL | VOL=0.8V; for fixed CLKs | 30.0 | 50.0 | - | mA |
| Output High Current[1] | IOH | VOL=2.0V; for fixed CLKs | - | -110.0 | -65.0 | mA |
| Output Low Voltage[1] | VOL | IOL=20mA; for CPUs & BUSes | - | 0.25 | 0.4 | V |
| Output High Voltage[1] | VOH | IOH=-70mA; for CPUs & BUSes | 2.4 | 4.0 | - | V |
| Output Low Voltage[1] | VOL | IOL=15mA; for fixed CLKs | - | 0.2 | 0.4 | V |
| Output High Voltage[1] | VOH | IOH=-50mA; for fixed CLKs | 2.4 | 4.7 | - | V |
| Supply Current | IDD | @66.5 MHz; all outputs unloaded | - | 80.0 | 160.0 | mA |

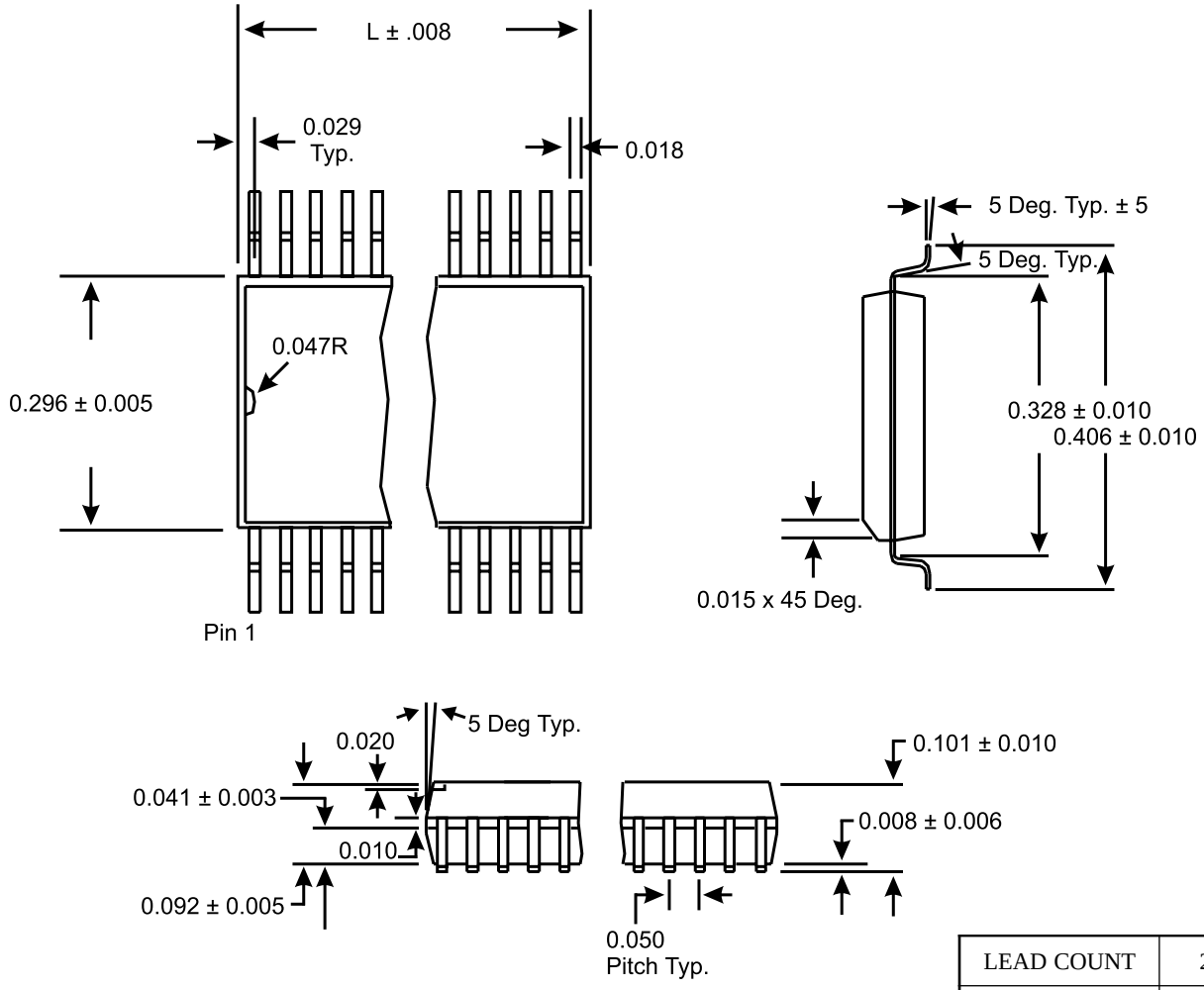
**Note 1:** Parameter is guaranteed by design and characterization. Not 100% tested in production.

## Electrical Characteristics at 5.5V

$V_{DD}$ = 4.5 – 5.5 V, $T_A$ = 0 – 70° C

| AC Characteristics | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
| Rise Time[1] | Tr1 | 20pF load, 0.8 to 2.0V CPU & BUS | - | 0.55 | 0.95 | ns |
| Fall Time[1] | Tf1 | 20pF load, 2.0 to 0.8V CPU & BUS | - | 0.52 | 0.90 | ns |
| Rise Time[1] | Tr2 | 20pF load, 20% to 80%CPU & BUS | - | 1.2 | 2.1 | ns |
| Fall Time[1] | Tf2 | 20pF load, 80% to 20% CPU & BUS | - | 1.1 | 2.0 | ns |
| Duty Cycle[1] | Dt1 | 20pF load @ $V_{OUT}$=1.4V | 52 | 57 | 62 | % |
| Duty Cycle[1] | Dt2 | 20pF load @ $V_{OUT}$=50% | 45 | 50 | 55 | % |
| Jitter, One Sigma[1] | Tj1s1 | CPU & BUS Clocks; Load=20pF, RS=33Ω FOUT>25 MHz | - | 50 | 150 | ps |
| Jitter, Absolute[1] | Tjab1 | CPU & BUS Clocks; Load=20pF, RS=33Ω FOUT>25 MHz | -250 | - | 250 | ps |
| Jitter, One Sigma[1] | Tj1s2 | REF CLKs; Load=20pF RS=33W | - | 1 | 3 | % |
| Jitter, Absolute[1] | Tjab2 | REF CLKs; Load=20pF RS=33W | -5 | 2 | 5 | % |
| Input Frequency[1] | Fi | | 12.0 | 14.318 | 16.0 | MHz |
| Logic Input Capacitance[1] | CIN | Logic input pins | - | 5 | - | pF |
| Crystal OscillatorCapacitance[1] | CINX | X1, X2 pins | - | 18 | - | pF |
| Power-on Time[1] | ton | From VDD=1.6V to 1 st crossing of 66.5 MHz VDD supply ramp < 40ms | - | 2.5 | 4.5 | ms |
| Frequency Settling Time[1] | ts | From 1st crossing of acquisition to < 1% settling | - | 2.0 | 4.0 | ms |
| Clock Skew Window[1] | Tsk1 | CPU to CPU; Load=20pF; @1.4V | - | 150 | 250 | ps |
| Clock Skew Window[1] | Tsk2 | BUS to BUS; Load=20pF; @1.4V | - | 300 | 500 | ps |
| Clock Skew Window[1] | Tsk3 | CPU & BUS; Load=20pF; @1.4V | 1 | 2.6 | 5 | ns |

**Note 1:** Parameter is guaranteed by design and characterization. Not 100% tested in production.




| | |
|---|---|
| LEAD COUNT | 28L |
| DIMENSIONL | 0.704 |

**SOIC Package**

## Ordering Information

### ICS9159M-14

Example:

**ICS XXXX M-PPP**

- **Pattern Number(2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  M=SOIC, SOP
- **Device Type**
  (consists of 3 or 4 digit numbers) plus one additional Alph designation
- **Prefix**
  ICS=Standard Device