



# Hex Parallel D Register With Enable

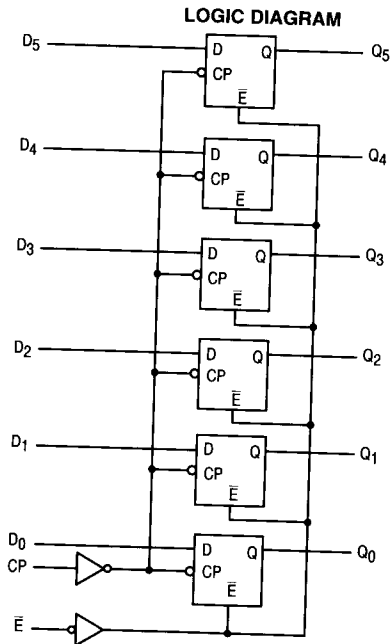
ELECTRICALLY TESTED PER:  
MIL-M-38510/34108

The 54F378 is a 6-Bit register with a buffered common enable. This device is similar to the 'F174, but features the common Enable rather than common Master Reset.

The 'F378 consists of six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable ( $\bar{E}$ ) inputs are common to all flip-flops.

When the  $\bar{E}$  input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When  $\bar{E}$  is HIGH, the register will retain the present data independent of the CP. This circuit is designed to prevent false clocking by transitions on the  $\bar{E}$  input.

- 6-Bit High-Speed Parallel Register
- Positive Edge Triggered D Type Inputs
- Fully Buffered Common Clock and Enable Inputs
- Input Clamp Diodes Limit High Speed Termination Effects
- Full TTL and CMOS Compatible



Please note that this logic diagram is provided for the understanding of logic operations and should not be used to estimate propagation delays.

## Military 54F378



### AVAILABLE AS:

- 1) JAN: JM38510/34108BXA
- 2) SMD: 5962-8855501
- 3) 883: 54F378/BXAJC

X = CASE OUTLINE AS FOLLOWS:  
PACKAGE: CERDIP: E  
CERFLAT: F  
LCC: 2

THE LETTER "M" APPEARS  
BEFORE THE / ON LCC.

### PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
$\bar{E}$	1	1	2	GND
Q <sub>0</sub>	2	2	3	OPEN
D <sub>0</sub>	3	3	4	VCC
D <sub>1</sub>	4	4	5	VCC
Q <sub>1</sub>	5	5	7	OPEN
D <sub>2</sub>	6	6	8	VCC
Q <sub>2</sub>	7	7	9	OPEN
GND	8	8	10	GND
CP	9	9	12	VCC
Q <sub>3</sub>	10	10	13	OPEN
D <sub>3</sub>	11	11	14	VCC
Q <sub>4</sub>	12	12	15	OPEN
D <sub>4</sub>	13	13	17	VCC
D <sub>5</sub>	14	14	18	VCC
Q <sub>5</sub>	15	15	19	OPEN
VCC	16	16	20	VCC

BURN-IN CONDITIONS:  
VCC = 5.0 V MIN/6.0 V MAX

### TRUTH TABLE

Inputs			Output
$\bar{E}$	CP	D <sub>n</sub>	Q <sub>n</sub>
H		X	No Change
L		H	H
L		L	L

H = HIGH Voltage Level

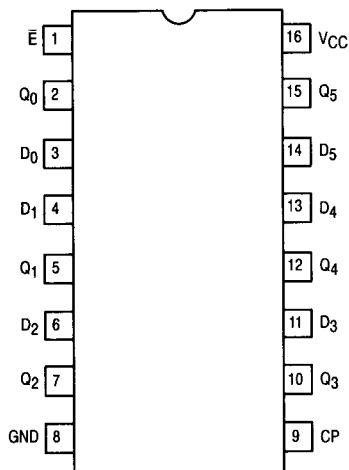
L = LOW Voltage Level

X = Irrelevant

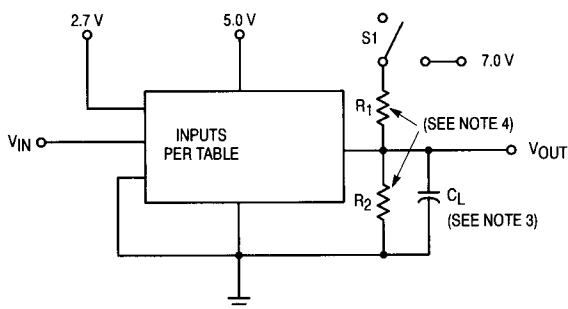
= Transition from Low to High Level

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## CONNECTION DIAGRAM



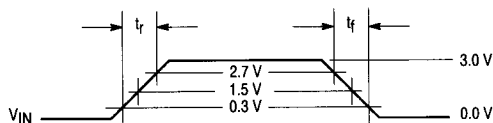
## AC TEST CIRCUIT



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Test Type	S1
$t_{PLH}$	open
$t_{PHL}$	open
$t_{PHZ}$	open
$t_{PZH}$	open
$t_{PLZ}$	closed
$t_{PZL}$	closed

## WAVEFORM

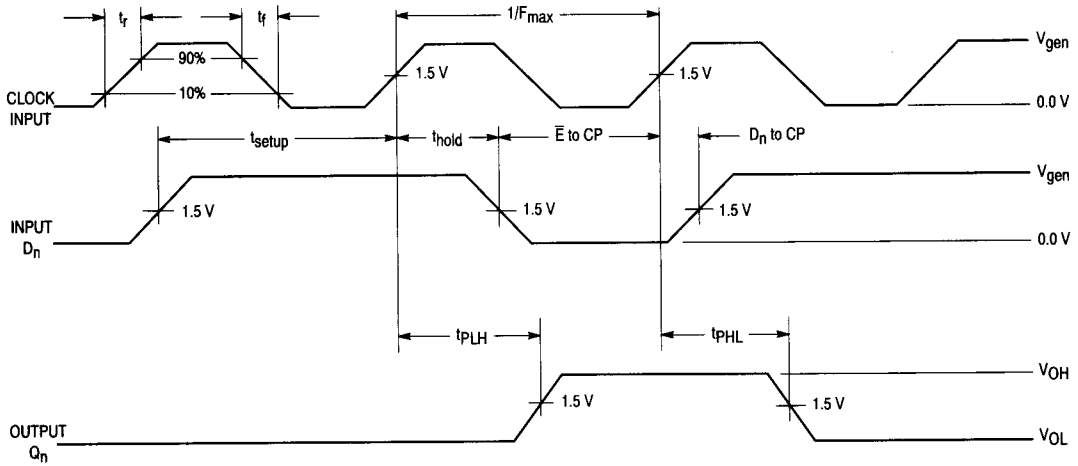


### NOTES:

- $V_{IN}$  = Input pulse and has the following characteristics:  
 $PRR \leq 1.0$  MHz,  $t_r = t_f \leq 2.5$  ns.
- Terminal conditions (pins not designated may be high  $\geq 2.0$  V, low  $\leq 0.8$  V, or open).
- $C_L = 50$  pF  $\pm 10\%$  including scope probe, wiring and stray capacitance, without package in test fixture.
- $R_1 = R_2 = 499 \Omega \pm 5.0\%$ .
- Voltage measurements are to be made with respect to network ground terminal.

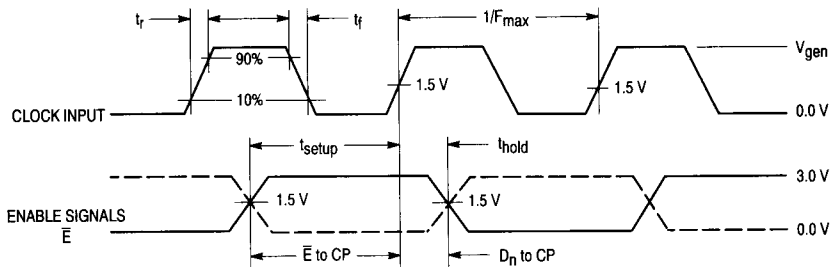
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WAVEFORMS



NOTES:

1. Clock input pulse has the following characteristics:  
 $V_{gen} = 3.0 \pm 0.2$  V,  $t_r = t_f \leq 2.5$  ns and  $PRR \leq 1.0$  MHz.
2. D input has the following characteristics:  
 $V_{gen} = 3.0 \pm 0.2$  V,  $\bar{E}$  to CP =  $t_{setup} = 3.0$  ns minimum  
 $(D_n > CLK)$ ,  $t_{hold} = 1.0$  ns minimum,  $D_n$  to CP =  $t_{hold}$  ( $D_n > CLK$ ).
3. For  $f_{MAX}$  testing, see table.



NOTES:

1. Clock input pulse has the following characteristics:  
 $V_{gen} = 3.0 \pm 0.2$  V,  $t_r = t_f \leq 2.5$  ns and  $PRR \leq 1.0$  MHz.
2. Enable characteristics are:  $t_{setup} = \bar{E}$  to CP = 6.0 ns ( $\bar{E} > CP$ ),  
 $t_{hold} = D_n$  to CP = 2.0 ns ( $\bar{E} > CP$ ).

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V <sub>OH</sub>	Logical "1" Output Voltage	2.5		2.5		2.5		V	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -1.0 mA, V <sub>IN</sub> = 2.0 V (all inputs), $\bar{E}$ = 0.8 V, CP = (See Note 1).
V <sub>OL</sub>	Logical "0" Output Voltage		0.5		0.5		0.5	V	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 20 mA, $\bar{E}$ = 0.8 V, V <sub>IN</sub> = 0.8 V (all inputs), CP = (See Note 1).
V <sub>IC</sub>	Input Clamping Voltage		-1.2					V	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA, other inputs are open.
I <sub>IH</sub>	Logical "1" Input Current		20		20		20	μA	V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.7 V, other inputs are open.
I <sub>IHH</sub>	Logical "1" Input Current		100		100		100	μA	V <sub>CC</sub> = 5.5 V, V <sub>IHH</sub> = 7.0 V, other inputs are open.
I <sub>IL</sub>	Logical "0" Input Current	-0.03	-0.6	-0.03	-0.6	-0.03	-0.6	mA	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> = 0.5 V, other inputs are open.
I <sub>OD</sub>	Diode Current	60		60		60		mA	V <sub>CC</sub> = 4.5 V, V <sub>IN</sub> = GND (all inputs), $\bar{E}$ = GND, V <sub>OUT</sub> = 2.5 V, CP = (See Note 1).
I <sub>OS</sub>	Output Short Circuit Current	-60	-150	-60	-150	-60	-150	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 4.5 V (all inputs) CP = (See Note 1), $\bar{E}$ = GND, V <sub>OUT</sub> = GND.
I <sub>CC</sub>	Power Supply Current		45		45		45	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = GND (all inputs), CP = (See Note 1), $\bar{E}$ = GND.
V <sub>IH</sub>	Logical "1" Input Voltage	2.0		2.0		2.0		V	V <sub>CC</sub> = 4.5 V.
V <sub>IL</sub>	Logical "0" Input Voltage		0.8		0.8		0.8	V	V <sub>CC</sub> = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V <sub>CC</sub> = 4.5 V, (Repeat at), V <sub>CC</sub> = 5.5 V, V <sub>INL</sub> = 0.5 V, V <sub>INH</sub> = 2.5 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t <sub>PHL1</sub>	Propagation Delay /Data-Output Output <u>High-Low</u>	3.0	8.5	2.5	10.5	2.5	10.5	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = R <sub>2</sub> = 499 Ω ± 5.0%.
t <sub>PLH1</sub>	Propagation Delay /Data-Output Output <u>Low-High</u>	2.5	7.5	2.0	9.5	2.0	9.5	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = R <sub>2</sub> = 499 Ω ± 5.0%.
f <sub>MAX</sub>	Maximum Clock Frequency	80		60		60		MHz	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = R <sub>2</sub> = 499 Ω ± 5.0%.

## NOTES:

1. Apply all voltages, then apply 0 V, 3.0 V, 0 V to clock pulse, then make measurement.
2. Apply all voltages, then apply 3.0 V, 0 V, 3.0 V to clock pulse, then make measurement.
3. Apply all voltages, then apply 0 V, 3.0 V to clock pulse, then make measurement.
4. f<sub>MAX</sub>, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.