

## Document Title

**512K x8 bit 3.3V Low Power CMOS slow SRAM**

## Revision History

<u>Revision No</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
03	Revision History Insert Revised - Improved standby current Isb1 : 30uA ; <del>20uA</del>	Jul.06.2000	Final
04	Revised - Change Iccdr Value : 15uA => 20uA	Aug.04.2000	Final
05	Marking Information Add Revised - E.T (-25~85°C), I.T (-40~85°C) Part Insert - AC Test Condition Add : 5pF Test Load - VIH max : Vcc + 0.2V => Vcc + 0.3V - VIL min : - 0.2V => - 0.3V	Dec.04.2000	Final
06	Changed Logo - HYUNDAI -> hynix - Marking Information Change	Apr.30.2001	Final

## DESCRIPTION

The HY62V8400A is a high-speed, low power and 4M bits CMOS SRAM organized as 512K words by 8 bits. The HY62V8400A uses Hynix's high performance twin tub CMOS process technology and was designed for high-speed and low power circuit technology. It is particularly well suited for use in high-density and low power system applications. This device has a data retention mode that guarantees data to remain valid at the minimum power supply voltage of 2.0V.

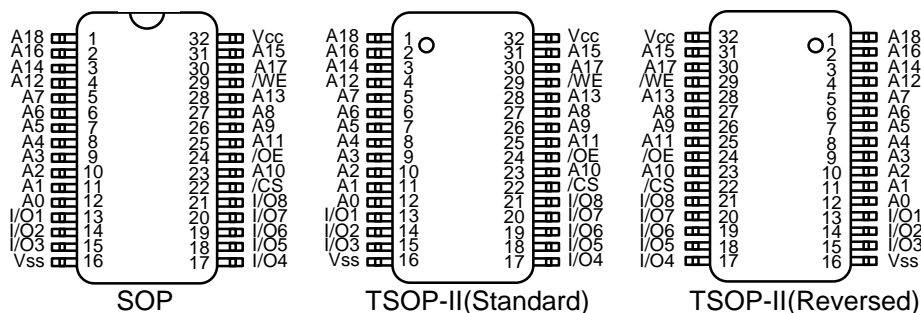
## FEATURES

- Fully static operation and Tri-state outputs
- TTL compatible inputs and outputs
- Low power consumption
- Battery backup(LL-part)
  - 2.0V(min) data retention
- Standard pin configuration
  - 32pin 525mil SOP
  - 32pin 400mil TSOP-II
 (Standard and Reversed)

Product No.	Voltage (V)	Speed (ns)	Operation Current/I <sub>cc</sub> (mA)	Standby Current(μA)	Temperature (°C)
				LL	
HY62V8400A	3.0~3.6	70/85/100	5	20	0~70
HY62V8400A-E	3.0~3.6	70/85/100	5	30	-25~70
HY62V8400A-I	3.0~3.6	70/85/100	5	30	-40~70

Note 1. Current value is max.

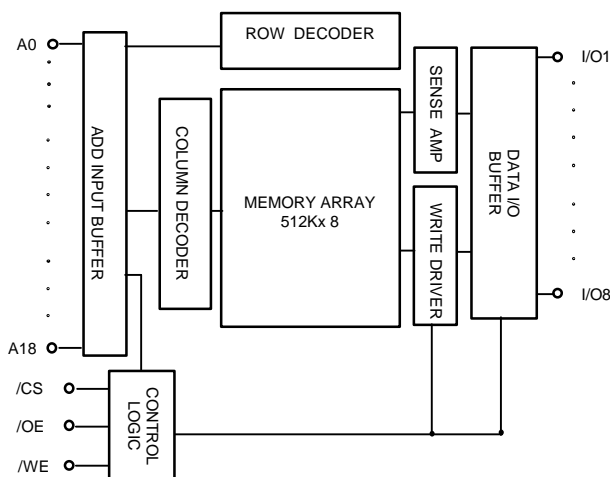
## PIN CONNECTION



## PIN DESCRIPTION

Pin Name	Pin Function
/CS	Chip Select
/WE	Write Enable
/OE	Output Enable
A0 ~ A18	Address Input
I/O1 ~ I/O8	Data Input/Output
Vcc	Power(3.0~3.6V)
Vss	Ground

## BLOCK DIAGRAM



**ORDERING INFORMATION**

Part No.	Speed	Power	Temp	Package
HY62V8400ALLG	70/85/100	LL-part	0~70 °C	SOP
HY62V8400ALLG-E	70/85/100	LL-part	-25~85 °C	SOP
HY62V8400ALLG-I	70/85/100	LL-part	-40~85 °C	SOP
HY62V8400ALLT2	70/85/100	LL-part	0~70 °C	TSOP-II (Standard)
HY62V8400ALLT2-E	70/85/100	LL-part	-25~85 °C	TSOP-II (Standard)
HY62V8400ALLT2-I	70/85/100	LL-part	-40~85 °C	TSOP-II (Standard)
HY62V8400ALLR2	70/85/100	LL-part	0~70 °C	TSOP-II (Reversed)
HY62V8400ALLR2-E	70/85/100	LL-part	-25~85 °C	TSOP-II (Reversed)
HY62V8400ALLR2-I	70/85/100	LL-part	-40~85 °C	TSOP-II (Reversed)

**ABSOLUTE MAXIMUM RATING (1)**

Symbol	Parameter	Rating	Unit
V <sub>CC</sub> , V <sub>IN</sub> , V <sub>OUT</sub>	Power Supply, Input/Output Voltage	-0.5 to 4.0	V
T <sub>A</sub>	Operating Temperature	HY62V8400A	0 to 70
		HY62V8400A-E	-25 to 85
		HY62V8400A-I	-40 to 85
T <sub>STG</sub>	Storage Temperature	-65 to 150	°C
P <sub>D</sub>	Power Dissipation	1.0	W
I <sub>OUT</sub>	Data Output Current	50	MA
T <sub>SOLDER</sub>	Lead Soldering Temperature & Time	260 •10	°C•sec

**Note**

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

**TRUTH TABLE**

/CS	/WE	/OE	MODE	I/O OPERATION	Power
H	X	X	Deselected	High-Z	Standby
L	H	H	Output Disabled	High-Z	Active
L	H	L	Read	Data Out	Active
L	L	X	Write	Data In	Active

**Note :**

- H=V<sub>IH</sub>, L=V<sub>IL</sub>, X=don't care (V<sub>IH</sub> or V<sub>IL</sub>)

## RECOMMENDED DC OPERATING CONDITION

$T_A = 0$ ;  $f = 70$ ; (Normal)/-25°C to 85°C (Extended) /-40°C to 85°C (Industrial), unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	3.0	3.3	3.6	V
V <sub>SS</sub>	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>CC</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3(1)	-	0.4	V

Note :

1. V<sub>IL</sub> = -1.5V for pulse width less than 30ns and not 100% tested.

## DC ELECTRICAL CHARACTERISTICS

$T_A = 0$ ;  $f = 70$ ; (Normal)/-25°C to 85°C (Extended) /-40°C to 85°C (Industrial), unless otherwise specified.

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	
I <sub>LI</sub>	Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{CC}$	-1	-	1	uA	
I <sub>LO</sub>	Output Leakage Current	$V_{SS} \leq V_{OUT} \leq V_{CC}$ , /CS = V <sub>IH</sub> or /OE = V <sub>IH</sub> or /WE = V <sub>IL</sub>	-1	-	1	uA	
I <sub>CC</sub>	Operating Power Supply Current	/CS = V <sub>IL</sub> , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>I/O</sub> = 0mA	-	-	5	mA	
I <sub>CC1</sub>	Average Operating Current	/CS = V <sub>IL</sub> Min Duty Cycle = 100%, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>I/O</sub> = 0mA	-	-	40	mA	
I <sub>SB</sub>	TTL Standby Current (TTL Input)	/CS = V <sub>IH</sub> , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	-	-	0.5	mA	
I <sub>SB1</sub>	Standby Current (CMOS Input)	/CS $\geq$ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> $\geq$ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> $\leq$ V <sub>SS</sub> + 0.2V	LL	-	-	20	uA
			LL-E/I	-	-	30	uA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA	-	-	0.4	V	
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -1mA	2.2	-	-	V	

Note : Typical values are at V<sub>CC</sub> = 3.3V, T<sub>A</sub> = 25°C

## CAPACITANCE

Temp = 25°C, f = 1.0MHz

Symbol	Parameter	Condition	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>I/O</sub> = 0V	8	pF

Note : This parameter is sampled and not 100% tested

**AC CHARACTERISTICS**

TA = 0; fto 70; (Normal)/-25°C to 85°C (Extended) /-40°C to 85°C (Industrial), unless otherwise specified.

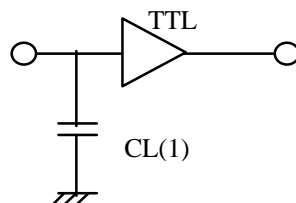
#	Symbol	Parameter	70ns		85ns		100ns		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
READ CYCLE									
1	tRC	Read Cycle Time	70	-	85	-	100	-	ns
2	tAA	Address Access Time	-	70	-	85	-	100	ns
3	tACS	Chip Select Access Time	-	70	-	85	-	100	ns
4	tOE	Output Enable to Output Valid	-	40	-	45	-	50	ns
5	tCLZ	Chip Select to Output in Low Z	10	-	10	-	10	-	ns
6	tOLZ	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
7	tCHZ	Chip Deselecting to Output in High Z	0	25	0	30	0	30	ns
8	tOHZ	Out Disable to Output in High Z	0	25	0	30	0	30	ns
9	tOH	Output Hold from Address Change	15	-	15	-	15	-	ns
WRITE CYCLE									
10	tWC	Write Cycle Time	70	-	85	-	100	-	ns
11	tCW	Chip Selection to End of Write	60	-	70	-	80	-	ns
12	tAW	Address Valid to End of Write	60	-	70	-	80	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width	50	-	60	-	70	-	ns
15	tWR	Write Recovery Time	0	-	0	-	0	-	ns
16	tWHZ	Write to Output in High Z	0	25	0	30	0	30	ns
17	tDW	Data to Write Time Overlap	30	-	35	-	40	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
19	tOW	Output Active from End of Write	5	-	5	-	5	-	ns

**AC TEST CONDITIONS**

TA = 0; fto 70; (Normal)/-25°C to 85°C (Extended) /-40°C to 85°C (Industrial), unless otherwise specified.

Parameter	Value	
Input Pulse Level	0.4V to 2.2V	
Input Rise and Fall Time	5ns	
Input and Output Timing Reference Level	1.5V	
Output Load	tCLZ,tOLZ,tCHZ,tOHZ,tWHZ	CL = 5pF + 1TTL Load
	Others	CL = 100pF + 1TTL Load

**AC TEST LOADS**

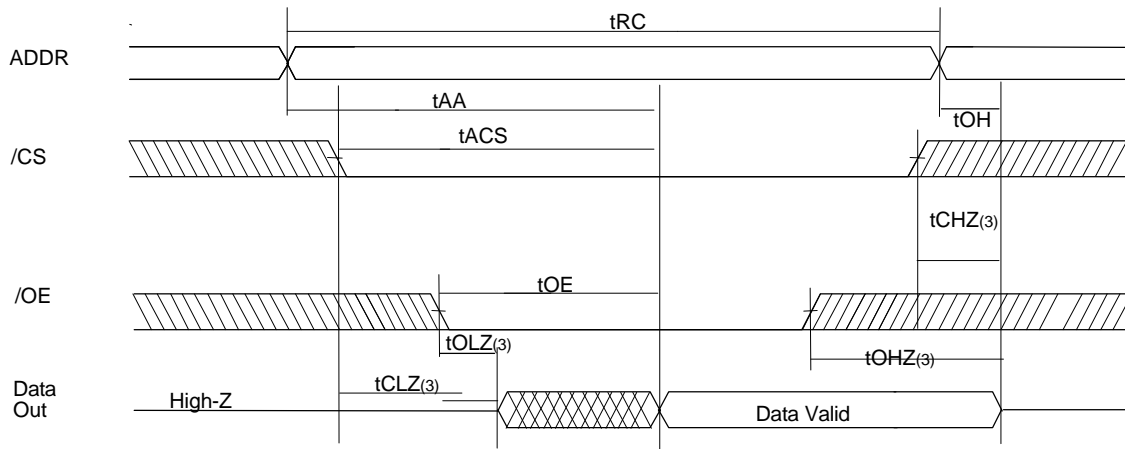


Note

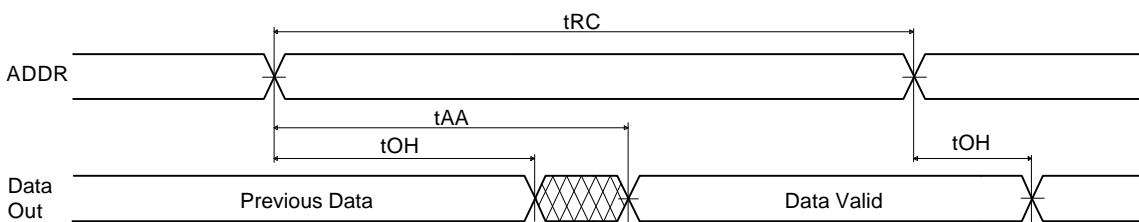
1. Including jig and scope capacitance

**TIMING DIAGRAM**

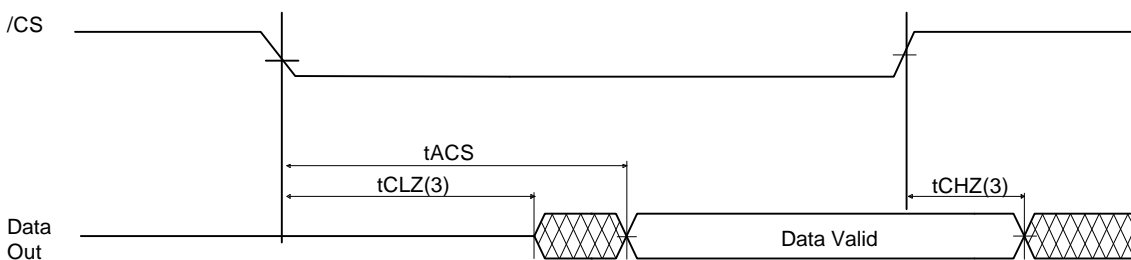
READ CYCLE 1 (Note 1,4)



READ CYCLE 2 (Note 1,2,4)



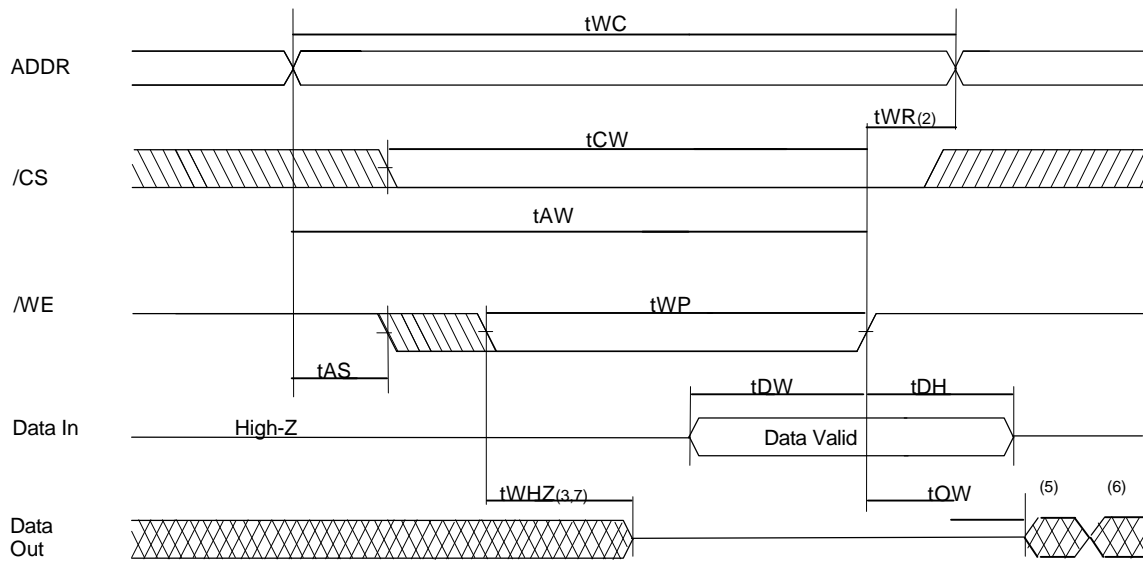
READ CYCLE 3 (Note 1,2,4)



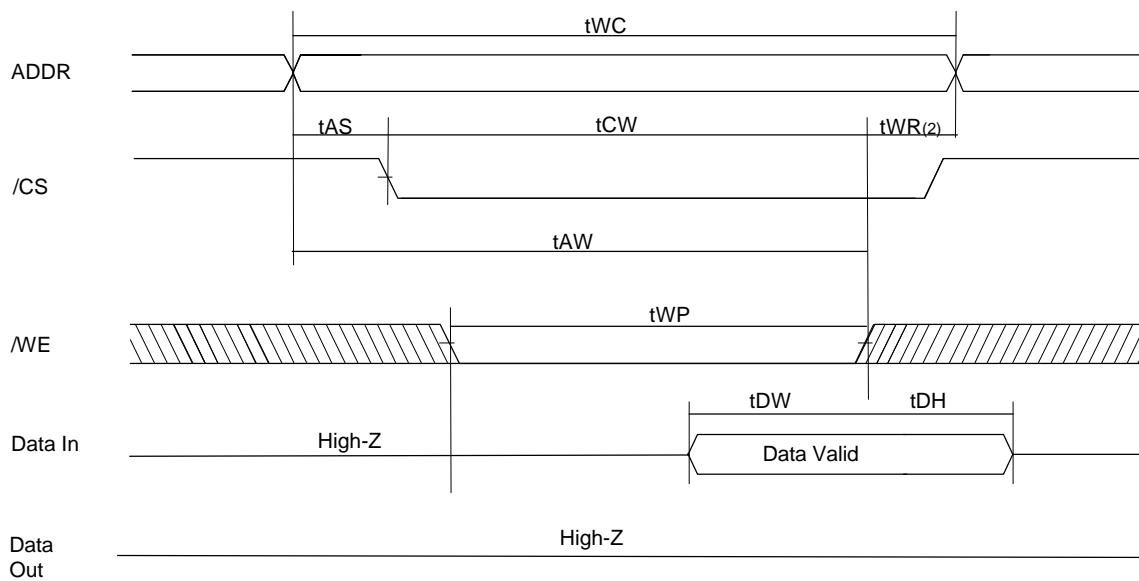
Notes:

1. A read occurs during the overlap of a low /OE, a high /WE, and a low /CS.
2. /OE =  $V_{IL}$
3. Transition is measured  $\pm 200mV$  from steady state voltage.  
This parameter is sampled and not 100% tested.
4. /CS in high for the standby, low for active

WRITE CYCLE 1(1,4,5,8) (/WE Controlled)



WRITE CYCLE 2 (Note 1,4,5,8) (/CS Controlled)



Notes:

1. A write occurs during the overlap of a low /WE and a low /CS.
2. tWR is measured from the earlier of /CS or /WE going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the /CS low transition occur simultaneously with the /WE low transition or after the /WE transition, outputs remain in a high impedance state.
5. Q(data out) is the same phase with the write data of this write cycle.
6. Q(data out) is the read data of the next address.
7. Transition is measured + 200mV from steady state.  
This parameter is sampled and not 100% tested.
8. /CS in high for the standby, low for active

**DATA RETENTION ELECTRIC CHARACTERISTIC**

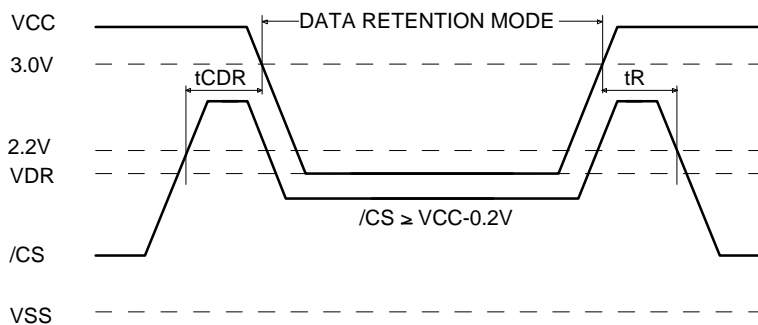
TA = 0; Ito 70; (Normal)/-25°C to 85°C (Extended) /-40°C to 85°C (Industrial), unless otherwise specified.

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	
VDR	Vcc for Data Retention	/CS ≥ Vcc - 0.2V, VIN ≥ Vcc - 0.2V or VIN ≤ Vss + 0.2V	2.0	-	-	V	
ICCDR	Data Retention Current	Vcc = 3.0V, /CS ≥ Vcc - 0.2V, VIN ≥ Vcc - 0.2V or VIN ≤ Vss + 0.2V	LL	-	-	20	uA
			LL-E	-	-	30	uA
			LL-I	-	-	30	uA
tCDR	Chip Deselect to Data Retention Time		0	-	-	ns	
tR	Operating Recovery Time		tRC(2)	-	-	ns	

Notes:

1. Typical values are at the condition of TA = 25°C.
2. tRC is read cycle time.

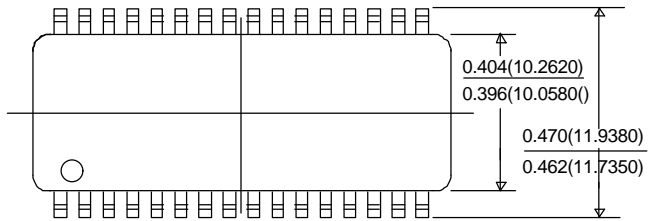
**DATA RETENTION TIMING DIAGRAM**



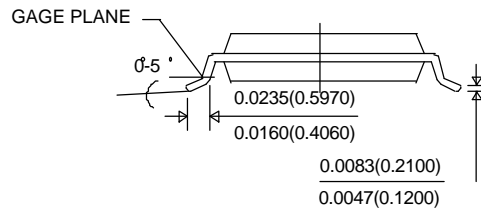
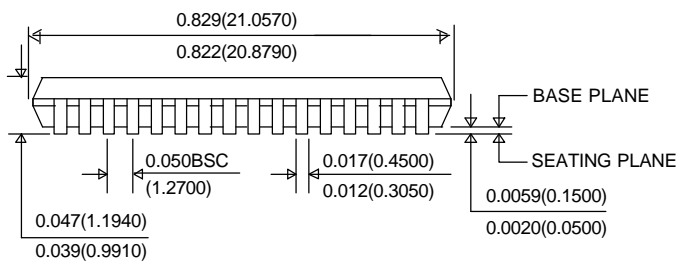


**PACKAGE INFORMATION**

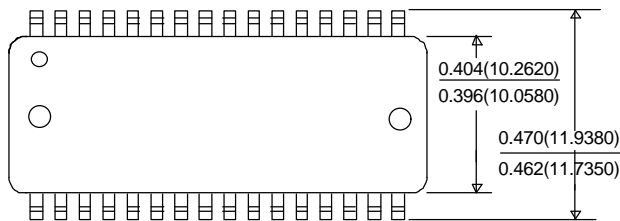
32pin 400mil Thin Small Outline Package Standard(T2)



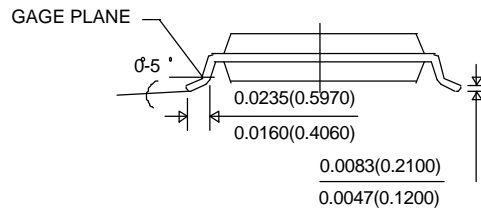
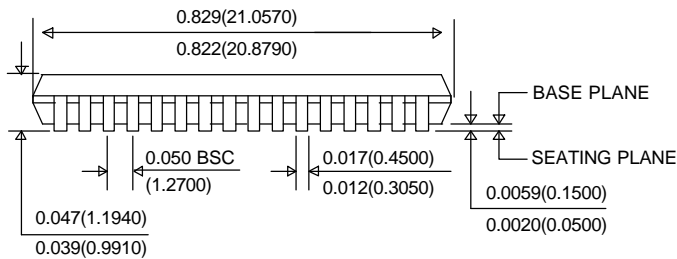
UNIT : INCH(mm) **MAX.**  
**MIN.**



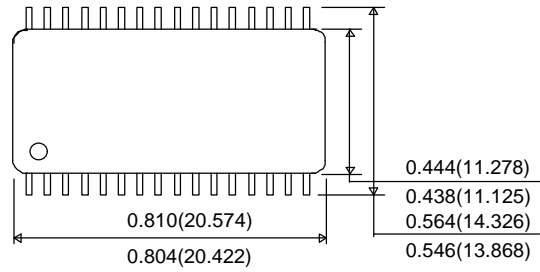
32pin 400mil Thin Small Outline Package Reversed(R2)



UNIT : INCH(mm) **MAX.**  
**MIN.**



32pin 525mil Small Outline Package(G)



UNIT : INCH(mm)

