

T.46-23-12

**CY7C130/CY7C131
CY7C140/CY7C141**



CYPRESS
SEMICONDUCTOR

**1024 x 8 Dual-Port
Static RAM**

Features

- 0.8-micron CMOS for optimum speed/power
- Automatic power-down
- TTL compatible
- Capable of withstanding greater than 2001V electrostatic discharge
- Fully asynchronous operation
- Master CY7C130/CY7C131 easily expands data bus width to 16 or more bits using SLAVE CY7C140/CY7C141
- BUSY output flag on CY7C130/CY7C131; BUSY input on CY7C140/CY7C141
- INT flag for port-to-port communication

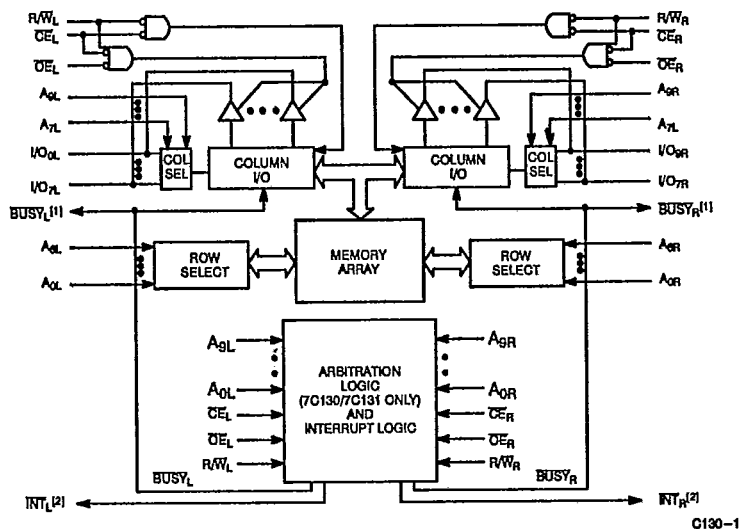
Functional Description

The CY7C130/CY7C131/CY7C140/CY7C141 are high-speed CMOS 1K by 8 dual-port static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C130/CY7C131 can be utilized as either a standalone 8-bit dual-port static RAM or as a master dual-port RAM in conjunction with the CY7C140/CY7C141 slave dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data, such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; chip enable (CE), write enable (R/W), and output enable (OE). Two flags are provided on each port, BUSY and INT. BUSY signals that the port is trying to access the same location currently being accessed by the other port. INT is an interrupt flag indicating that data has been placed in a unique location (3FF for the left port and 3FE for the right port). An automatic power-down feature is controlled independently on each port by the chip enable (CE) pins.

The CY7C130 and CY7C140 are available in both 48-pin DIP and 48-pin LCC. The CY7C131 and CY7C141 are available in both 52-pin LCC and PLCC.

Logic Block Diagram



Pin Configurations

DIP Top View

CE _L	1	48	V _{CC}
R/W _L	2	47	CE _R
BUSY _L	3	46	R/W _R
INT _L	4	45	BUSY _R
OEL	5	44	INT _R
A _{9L}	6	43	OER
A _{1L}	7	42	A _{9R}
A _{2L}	8	41	A _{1R}
A _{3L}	9	40	A _{2R}
A _{4L}	10	39	A _{3R}
A _{5L}	11	38	A _{4R}
A _{6L}	12	7C130 37	A _{5R}
A _{7L}	13	7C140 36	A _{6R}
A _{8L}	14	35	A _{7R}
A _{9L}	15	34	A _{8R}
IO _{9L}	16	33	A _{9R}
IO _{1L}	17	32	IO _{9R}
IO _{2L}	18	31	IO _{8R}
IO _{3L}	19	30	IO _{7R}
IO _{4L}	20	29	IO _{6R}
IO _{5L}	21	28	IO _{5R}
IO _{6L}	22	27	IO _{4R}
IO _{7L}	23	26	IO _{3R}
GND	24	25	IO _{2R}
			IO _{1R}
			IO _{0R}

Notes:

1. CY7C130/CY7C131 (Master): BUSY is open drain output and requires pull-up resistor. CY7C140/CY7C141 (Slave): BUSY is input.
2. Open drain outputs: pull-up resistor required.

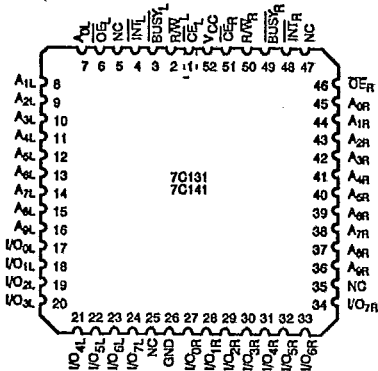


Pin Configurations (continued)

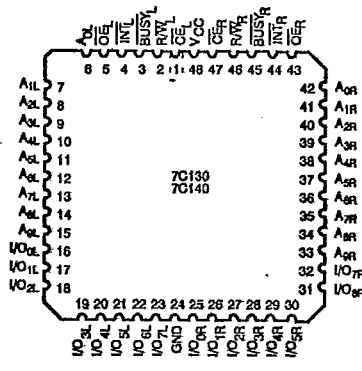
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52-Pin LCC/PLCC
Top View

48-Pin LCC/QFP
Top View



C130-3



C130-4



SRAMS

Selection Guide

	7C130-25 ^[3] 7C131-25 7C140-25 7C141-25	7C130-30 7C131-30 7C140-30 7C141-30	7C130-35 7C131-35 7C140-35 7C141-35	7C130-45 7C131-45 7C140-45 7C141-45	7C130-55 7C131-55 7C140-55 7C141-55
Maximum Access Time (ns)	25	30	35	45	55
Maximum Operating Current (mA)	Com'l/Ind	170	170	120	90
	Military			170	120
Maximum Standby Current (mA)	Com'l/Ind	65	65	45	35
	Military			65	45

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature - 65°C to +150 °C
- Ambient Temperature with Power Applied - 55°C to +125°C
- Supply Voltage to Ground Potential (Pin 48 to Pin 24) - 0.5V to +7.0V
- DC Voltage Applied to Outputs in High Z State - 0.5V to +7.0V
- DC Input Voltage - 3.5V to +7.0V
- Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	- 40°C to +85°C	5V ± 10%
Military ^[4]	- 55°C to +125°C	5V ± 10%

Notes:

3. 25-ns version available only in PLCC/LCC packages.

4. T_A is the "instant on" case temperature.



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CY7C130/CY7C131
CY7C140/CY7C141

Electrical Characteristics Over the Operating Range^[5]

Parameter	Description	Test Conditions	7C130-25,30 ^[3] 7C131-25,30 7C140-25,30 7C141-25,30		7C130-35 7C131-35 7C140-35 7C141-35		7C130-45,55 7C131-45,55 7C140-45,55 7C141-45,55		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	I _{OL} = 4.0 mA		0.4		0.4		0.4	V
		I _{OL} = 16.0 mA ^[6]		0.5		0.5		0.5	
V _{IH}	Input HIGH Voltage		2.2		2.2		2.2		V
V _{IL}	Input LOW Voltage			0.8		0.8		0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	- 5	+5	- 5	+5	- 5	+5	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	- 5	+5	- 5	+5	- 5	+5	μA
I _{OS}	Output Short Circuit Current ^[7,8]	V _{CC} = Max., V _{OUT} = GND		- 350		- 350		- 350	mA
I _{CC}	V _{CC} Operating Supply Current	C _E = V _{IL} , Outputs Open, f = f _{MAX} ^[9]	Com'l	170		120		90	mA
			Mil			170		120	
I _{SB1}	Standby Current Both Ports, TTL Inputs	C _E L and C _E R ≥ V _{IH} , f = f _{MAX} ^[9]	Com'l	65		45		35	mA
			Mil			65		45	
I _{SB2}	Standby Current One Port, TTL Inputs	C _E L or C _E R ≥ V _{IH} , Active Port Outputs Open, f = f _{MAX} ^[9]	Com'l	115		90		75	mA
			Mil			115		90	
I _{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports C _E L and C _E R ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0	Com'l	15		15		15	mA
			Mil			15		15	
I _{SB4}	Standby Current One Port, CMOS Inputs	One Port C _E L or C _E R ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, Active Port Outputs Open, f = f _{MAX} ^[9]	Com'l	105		85		70	mA
			Mil			105		85	

Capacitance^[8]

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	15	pF
C _{OUT}	Output Capacitance		10	pF

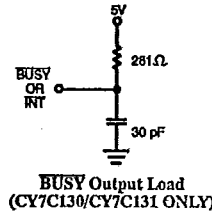
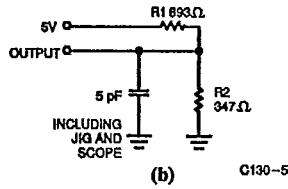
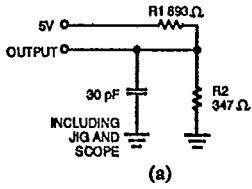
Notes:

- See the last page of this specification for Group A subgroup testing information.
- BUSY and INT pins only.
- Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.
- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of 1/t_{RC} and using AC Test Waveforms input levels of GND to 3V.
- AC Test conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
- AC Test Conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
- t_{IZCE}, t_{IzWE}, t_{HzOE}, t_{HzCE} and t_{HzWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
- At any given temperature and voltage condition, t_{HzCE} is less than t_{IzCE} for any given device.
- The internal write time of the memory is defined by the overlap of CS LOW and R/W LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

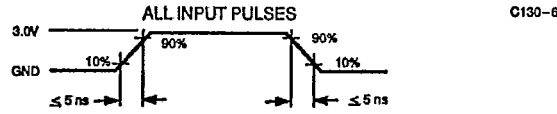


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AC Test Loads and Waveforms



Equivalent to: THEVENIN EQUIVALENT
OUTPUT — 250Ω — 1.40V



Switching Characteristics Over the Operating Range^[5,11]

Parameters	Description	7C130-25 ^[3]		7C130-30		7C130-35		7C130-45		7C130-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t _{RC}	Read Cycle Time	25		30		35		45		55		ns
t _{AA}	Address to Data Valid ^[12]		25		30		35		45		55	ns
t _{OHA}	Data Hold from Address Change	0		0		0		0		0		ns
t _{ACE}	CE LOW to Data Valid ^[12]		25		30		35		45		55	ns
t _{DOE}	OE LOW to Data Valid ^[12]		15		20		20		25		25	ns
t _{LZOE}	OE LOW to Low Z	3		3		3		3		3		ns
t _{HZOE}	OE HIGH to High Z ^[13]		15		15		20		20		25	ns
t _{LZCE}	CE LOW to Low Z ^[13,14]	5		5		5		5		5		ns
t _{HZCE}	CE HIGH to High Z ^[13,14]		15		15		20		20		25	ns
t _{PU}	CE LOW to Power-Up	0		0		0		0		0		ns
t _{PD}	CE HIGH to Power-Down		25		25		35		35		35	ns
WRITE CYCLE^[13]												
t _{WC}	Write Cycle Time	25		30		35		45		55		ns
t _{SCE}	CE LOW to Write End	20		25		30		35		40		ns
t _{AW}	Address Set-Up to Write End	20		25		30		35		40		ns
t _{HA}	Address Hold from Write End	2		2		2		2		2		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t _{PWE}	R/W Pulse Width	15		25		25		30		30		ns
t _{SD}	Data Set-Up to Write End	15		15		15		20		20		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		ns
t _{HZWE}	R/W LOW to High Z		15		15		20		20		25	ns
t _{LZWE}	R/W HIGH to Low Z	0		0		0		0		0		ns



Switching Characteristics Over the Operating Range^[5,11] (continued)

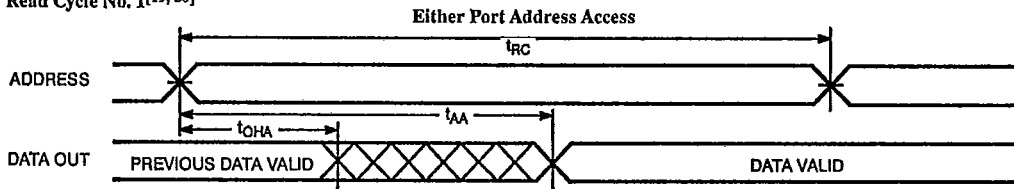
Parameters	Description	7C130-25 ^[3]		7C130-30		7C130-35		7C130-45		7C130-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
BUSY/INTERRUPT TIMING												
t _{BLA}	BUSY LOW from Address Match		20		20		20		25		30	ns
t _{BHA}	BUSY HIGH from Address Mismatch ^[16]		20		20		20		25		30	ns
t _{BLC}	BUSY LOW from \overline{CE} LOW		20		20		20		25		30	ns
t _{BHC}	BUSY HIGH from \overline{CE} HIGH ^[16]		20		20		20		25		30	ns
t _{PS}	Port Set Up for Priority	5		5		5		5		5		ns
t _{WB} ^[17]	R/W LOW after BUSY LOW	0		0		0		0		0		ns
t _{WH}	R/W HIGH after BUSY HIGH	20		30		30		35		35		ns
t _{BDD}	BUSY HIGH to Valid Data		25		30		35		45		45	ns
t _{DDD}	Write Data Valid to Read Data Valid		Note 18		Note 18		Note 18		Note 18		Note 18	ns
t _{WDD}	Write Pulse to Data Delay		Note 18		Note 18		Note 18		Note 18		Note 18	ns
INTERRUPT TIMING												
t _{WINS}	R/W to INTERRUPT Set Time		25		25		25		35		45	ns
t _{EINS}	\overline{CE} to INTERRUPT Set Time		25		25		25		35		45	ns
t _{INS}	Address to INTERRUPT Set Time		25		25		25		35		45	ns
t _{OINR}	\overline{OE} to INTERRUPT Reset Time ^[16]		25		25		25		35		45	ns
t _{EINR}	\overline{CE} to INTERRUPT Reset Time ^[16]		25		25		25		35		45	ns
t _{INR}	Address to INTERRUPT Reset Time ^[16]		25		25		25		35		45	ns

Notes:

16. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
17. CY7C140/CY7C141 only.
18. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
 - A. BUSY on Port B goes HIGH.
 - B. Port B's address is toggled.
 - C. \overline{CE} for Port B is toggled.
 - D. R/W for Port B is toggled during valid read.
19. R/W is HIGH for read cycle.
20. Device is continuously selected, $\overline{CE} = V_{IL}$ and $\overline{OE} = V_{IL}$.
21. Address valid prior to or coincident with \overline{CE} transition LOW.
22. If \overline{OE} is LOW during a R/W controlled write cycle, the write pulse width must be the larger of t_{PWZ} or $t_{HZWE} + t_{SD}$ to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD} .
23. If the \overline{CE} LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in the high-impedance state.

Switching Waveforms

Read Cycle No. 1^[19, 20]



C130-7

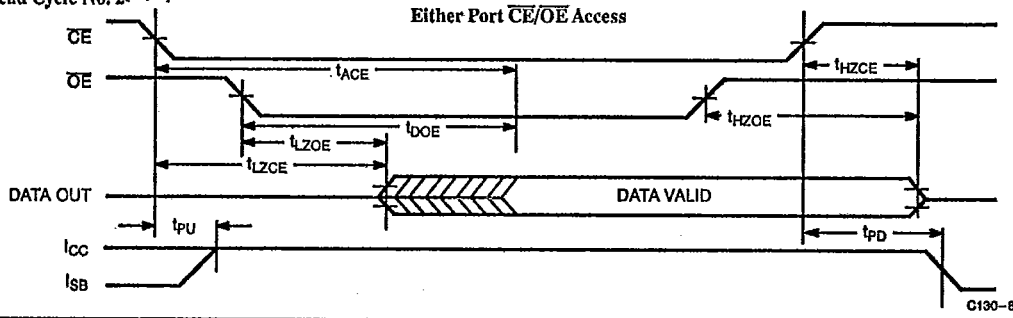


CY7C130/CY7C131
CY7C140/CY7C141

Switching Waveforms (continued)

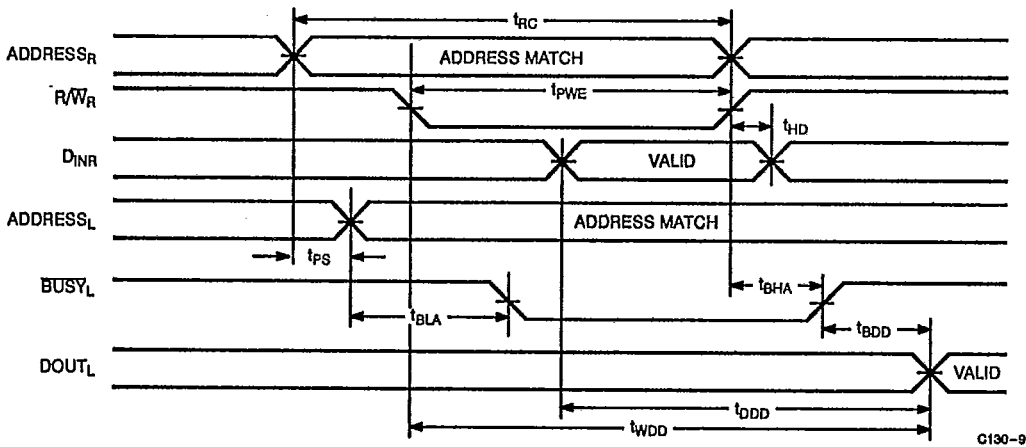
T-46-23-12

Read Cycle No. 2^[19,21]

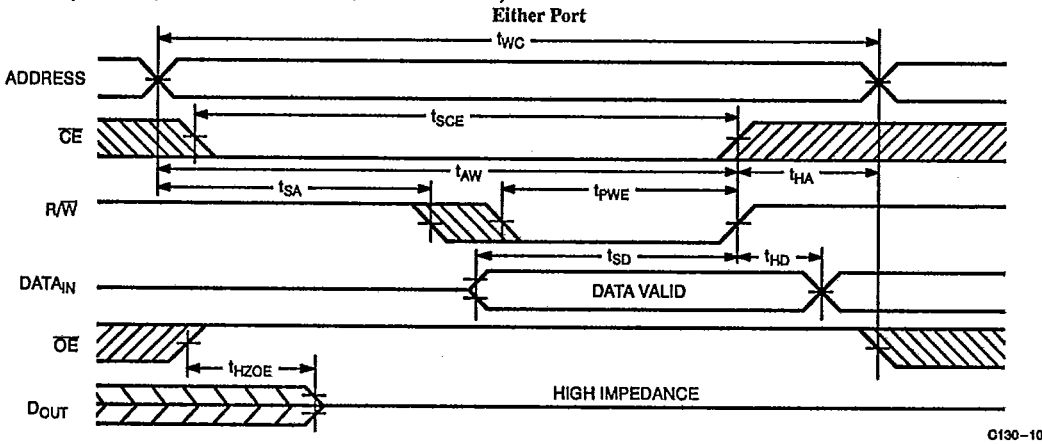


Read Cycle No. 3^[20]

Read with \overline{BUSY} , Master: CY7C130 and CY7C131



Write Cycle No.1 (OE Three-States Data I/Os - Either Port)^[15,22]



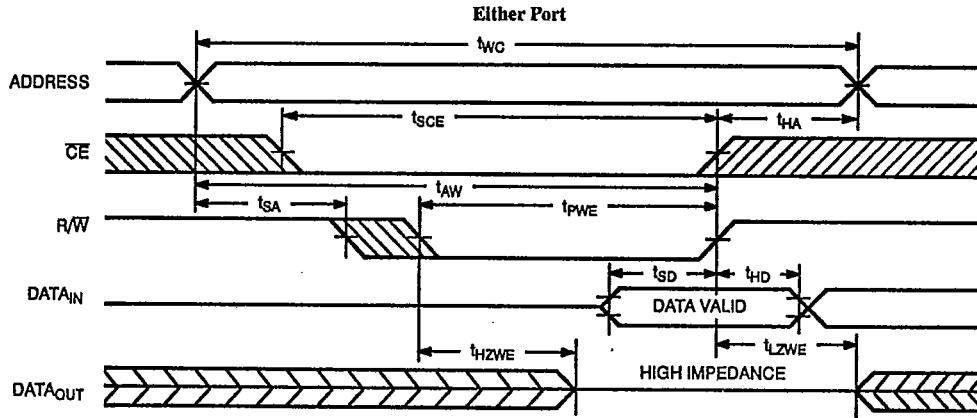


CY7C130/CY7C131
CY7C140/CY7C141

Switching Waveforms (continued)

T-46-23-12

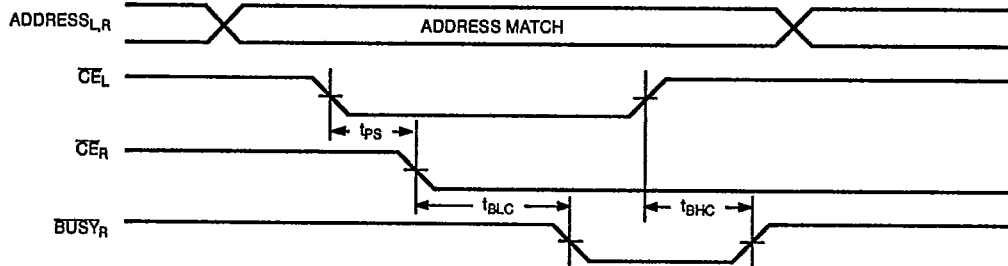
Write Cycle No. 2 (R/W Three-States Data I/Os - Either Port)^[15,23]



C130-11

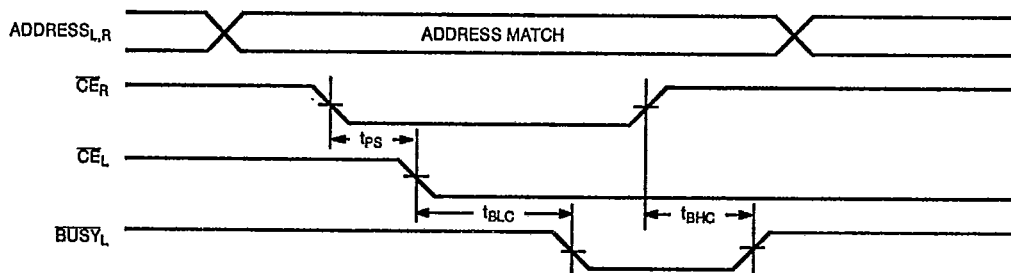
Busy Timing Diagram No. 1 (CE Arbitration)

\overline{CE}_L Valid First:



C130-12

\overline{CE}_R Valid First:



C130-13

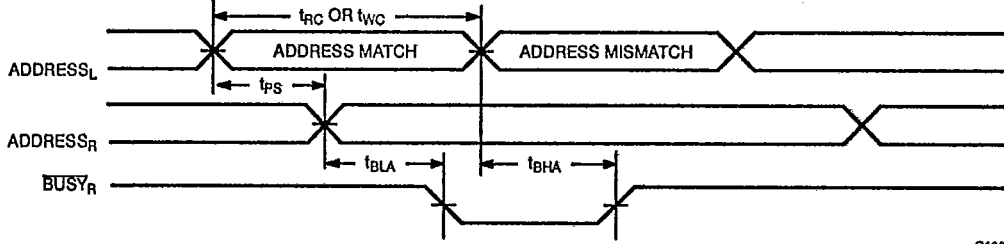


Switching Waveforms (continued)

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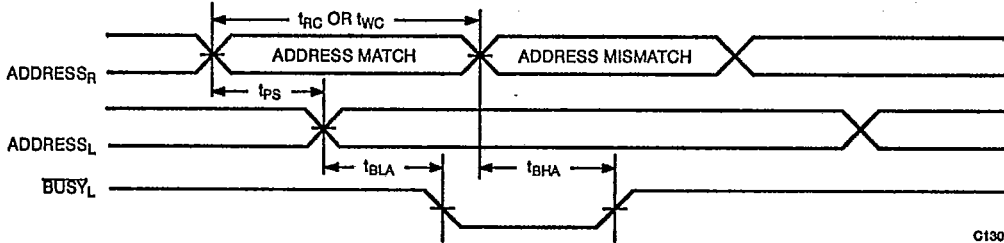
Busy Timing Diagram No. 2 (Address Arbitration)

Left Address Valid First:



G130-14

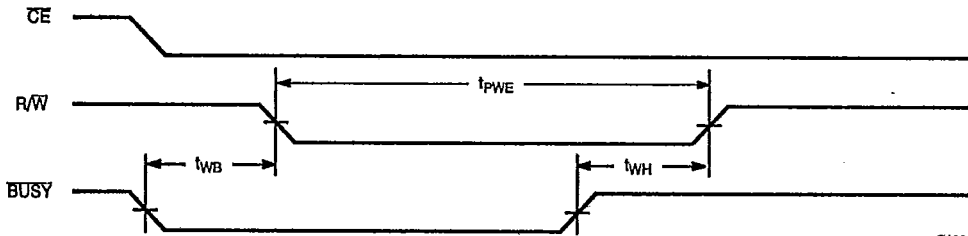
Right Address Valid First:



G130-15

Busy Timing Diagram No. 3

Write with $\overline{\text{BUSY}}$ (Slave: CY7C140/CY7C141)



G130-16





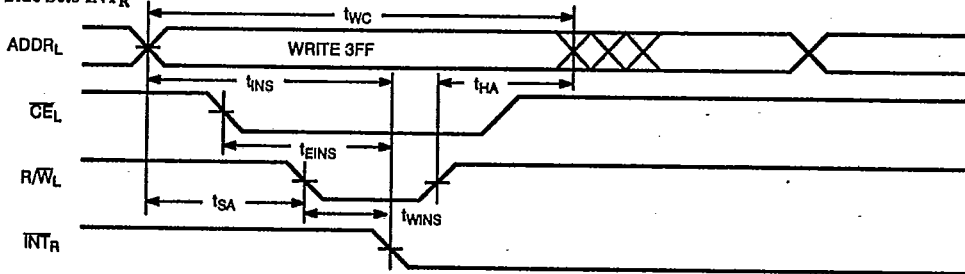
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CY7C130/CY7C131
CY7C140/CY7C141

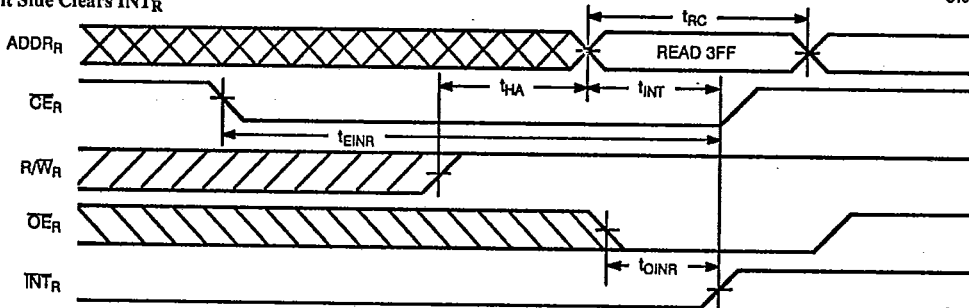
Switching Waveforms (continued)

Interrupt Timing Diagrams

Left Side Sets \overline{INT}_R



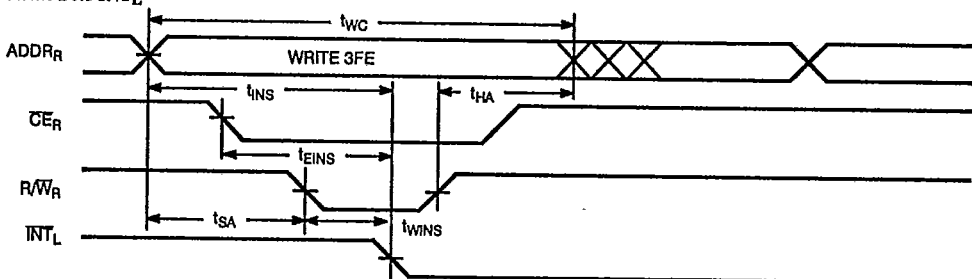
Right Side Clears \overline{INT}_R



C130-17

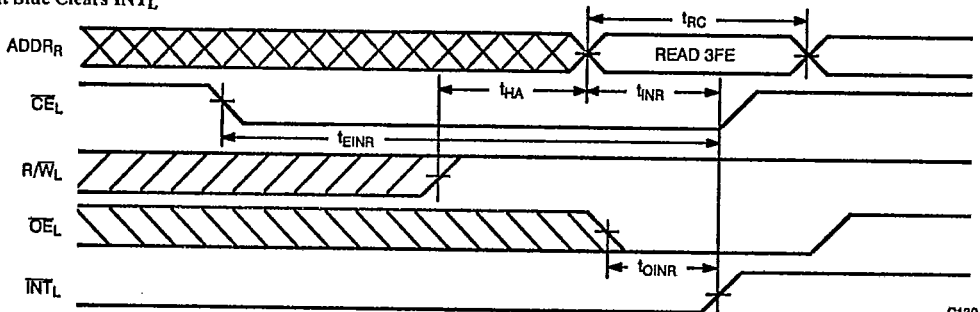
C130-18

Right Side Sets \overline{INT}_L



C130-19

Left Side Clears \overline{INT}_L



C130-20

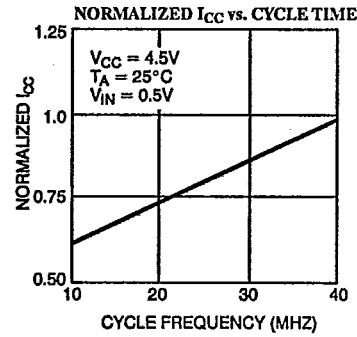
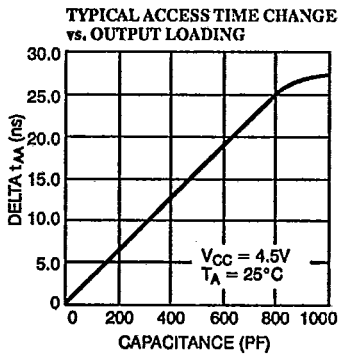
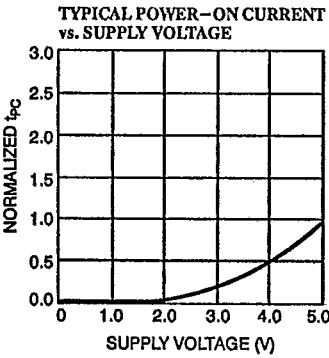
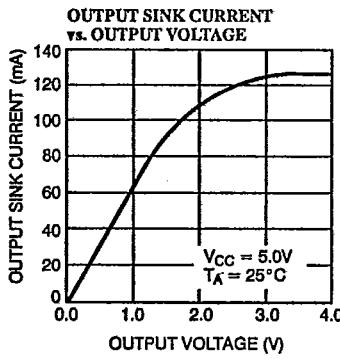
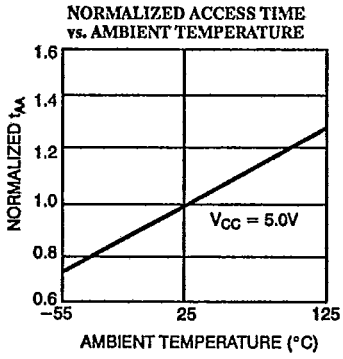
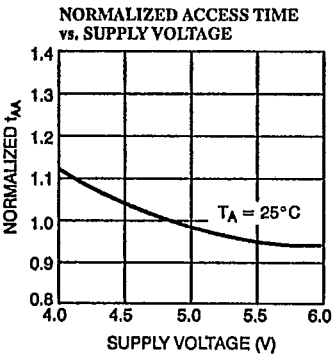
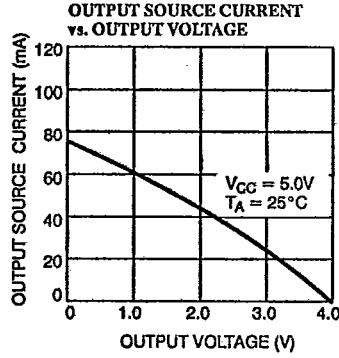
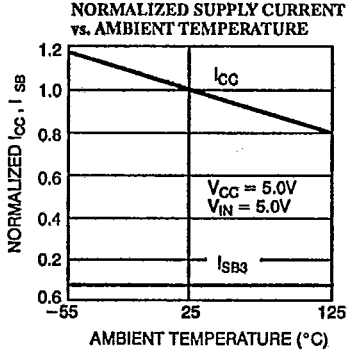
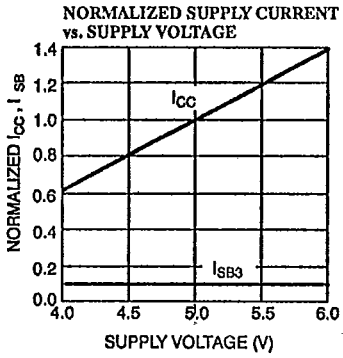


Typical DC and AC Characteristics

T-46-23-12



SRAMS





T-46-23-12

CY7C130/CY7C131
CY7C140/CY7C141

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C130-25LC	L68	Commercial
30	CY7C130-30DC	D26	Commercial
	CY7C130-30LC	L68	
	CY7C130-30PC	P25	
	CY7C130-30DI	D26	Industrial
	CY7C130-30PI	P25	
35	CY7C130-35DC	D26	Commercial
	CY7C130-35LC	L68	
	CY7C130-35PC	P25	
	CY7C130-35DI	D26	Industrial
	CY7C130-35PI	P25	
	CY7C130-35DMB	D26	Military
	CY7C130-35FMB	F78	
	CY7C130-35LMB	L68	
45	CY7C130-45DC	D26	Commercial
	CY7C130-45LC	L68	
	CY7C130-45PC	P25	
	CY7C130-45DI	D26	Industrial
	CY7C130-45PI	P25	
	CY7C130-45DMB	D26	Military
	CY7C130-45FMB	F78	
	CY7C130-45LMB	L68	
	55	CY7C130-55DC	D26
CY7C130-55LC		L68	
CY7C130-55PC		P25	
CY7C130-55DI		D26	Industrial
CY7C130-55PI		P25	
CY7C130-55DMB		D26	Military
CY7C130-55FMB		F78	
CY7C130-55LMB		L68	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C131-25JC	J69	Commercial
	CY7C131-25LC	L69	
30	CY7C131-30JC	J69	Commercial
	CY7C131-30LC	L69	
	CY7C131-30JI	J69	Industrial
35	CY7C131-35JC	J69	Commercial
	CY7C131-35LC	L69	
	CY7C131-35JI	J69	Industrial
	CY7C131-35FMB	F78	Military
	CY7C131-35LMB	L69	
45	CY7C131-45JC	J69	Commercial
	CY7C131-45LC	L69	
	CY7C131-45JI	J69	Industrial
	CY7C131-45FMB	F78	Military
	CY7C131-45LMB	L69	
55	CY7C131-55JC	J69	Commercial
	CY7C131-55LC	L69	
	CY7C131-55JI	J69	Industrial
	CY7C131-55FMB	F78	Military
	CY7C131-55MB	L69	



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CY7C130/CY7C131
CY7C140/CY7C141

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C140-25LC	L68	Commercial
30	CY7C140-30DC	D26	Commercial
	CY7C140-30LC	L68	
	CY7C140-30PC	P25	
	CY7C140-30DI	D26	Industrial
	CY7C140-30PI	P25	
35	CY7C140-35DC	D26	Commercial
	CY7C140-35LC	L68	
	CY7C140-35PC	P25	
	CY7C140-35DI	D26	Industrial
	CY7C140-35PI	P25	
	CY7C140-35DMB	D26	Military
	CY7C140-35FMB	F78	
	CY7C140-35LMB	L68	
45	CY7C140-45DC	D26	Commercial
	CY7C140-45LC	L68	
	CY7C140-45PC	P25	
	CY7C140-45DI	D26	Industrial
	CY7C140-45PI	P25	
	CY7C140-45DMB	D26	Military
	CY7C140-45FMB	F78	
	CY7C140-45LMB	L68	
55	CY7C140-55DC	D26	Commercial
	CY7C140-55LC	L68	
	CY7C140-55PC	P25	
	CY7C140-55DI	D26	Industrial
	CY7C140-55PI	P25	
	CY7C140-55DMB	D26	Military
	CY7C140-55FMB	F78	
	CY7C140-55LMB	L68	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C141-25JC	J69	Commercial
	CY7C141-25LC	L69	
30	CY7C141-30JC	J69	Commercial
	CY7C141-30LC	L69	
	CY7C141-30JI	J69	Industrial
35	CY7C141-35JC	J69	Commercial
	CY7C141-35LC	L69	
	CY7C141-35JI	J69	Industrial
	CY7C141-35FMB	F78	Military
	CY7C141-35LMB	L69	
45	CY7C141-45JC	J69	Commercial
	CY7C141-45LC	L69	
	CY7C141-45JI	J69	Industrial
	CY7C141-45FMB	F78	Military
	CY7C141-45LMB	L69	
55	CY7C141-55JC	J69	Commercial
	CY7C141-55LC	L69	
	CY7C141-55JI	J69	Industrial
	CY7C141-55FMB	F78	Military
	CY7C141-55LMB	L69	



SRAMS

**MILITARY SPECIFICATIONS****Group A Subgroup Testing****DC Characteristics**

Parameters	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL Max.}	1, 2, 3
I _{Ix}	1, 2, 3
I _{Oz}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3
I _{SB3}	1, 2, 3
I _{SB4}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
t _{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11

Parameters	Subgroups
BUSY/INTERRUPT TIMING	
t _{BLA}	7, 8, 9, 10, 11
t _{BHA}	7, 8, 9, 10, 11
t _{BLC}	7, 8, 9, 10, 11
t _{BHC}	7, 8, 9, 10, 11
t _{PS}	7, 8, 9, 10, 11
t _{WINS}	7, 8, 9, 10, 11
t _{EINS}	7, 8, 9, 10, 11
t _{INS}	7, 8, 9, 10, 11
t _{OINR}	7, 8, 9, 10, 11
t _{EINR}	7, 8, 9, 10, 11
t _{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t _{WB} ^[24]	7, 8, 9, 10, 11
t _{WH}	7, 8, 9, 10, 11
t _{BDD}	7, 8, 9, 10, 11

Note:

24. CY7C140/CY7C141 only.

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