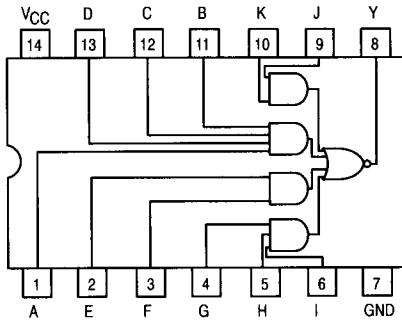




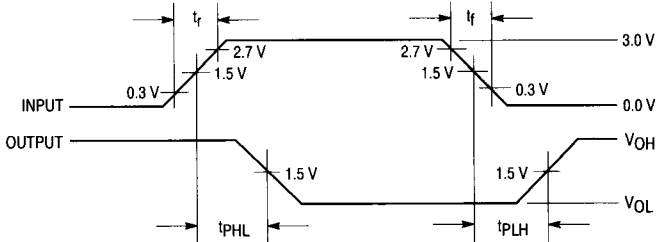
4-2-3-2-Input AND/OR/INVERT Gate

ELECTRICALLY TESTED PER:
MIL-M-38510/33401

LOGIC DIAGRAM



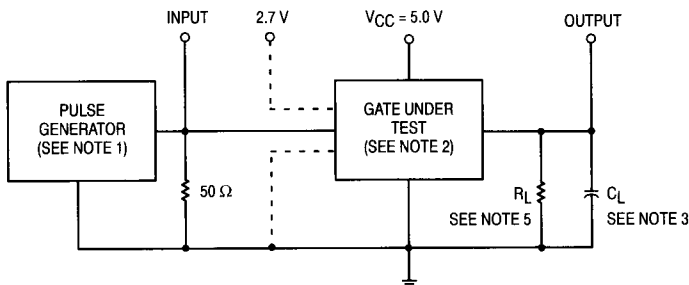
WAVEFORMS



NOTES:

1. Input pulse has the following characteristics: $t_r = t_f \leq 2.5$ ns, $PRR \leq 1.0$ MHz, and $Z_{OUT} \approx 50 \Omega$.
2. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.8 V, or open).
3. $C_L = 50$ pF $\pm 10\%$, including scope probe, wiring and stray capacitance, without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5. $R_L = 500 \Omega \pm 5.0\%$.

AC TEST CIRCUIT



Military 54F64



AVAILABLE AS:

- 1) JAN: JM38510/33401BXA
- 2) SMD: N/A
- 3) 883: 54F64/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	PIN ASSIGNMENTS			BURN-IN (COND. A)
	DIL 632-08	FLATS 717-04	LCC 756A-02	
A	1	1	2	VCC
E	2	2	3	VCC
F	3	3	4	VCC
G	4	4	6	VCC
H	5	5	8	VCC
I	6	6	9	VCC
GND	7	7	10	GND
Y	8	8	12	OPEN
J	9	9	13	VCC
K	10	10	14	VCC
B	11	11	16	VCC
C	12	12	18	VCC
D	13	13	19	VCC
VCC	14	14	20	VCC

BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX

4

54F64

4

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OH} = -1.0 mA, V _{OL} = 0.8 V, V _{IH} = 2.0 V, other inputs = 0 V.
V _{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V _{CC} = 4.5 V, I _{OL} = 20 mA, V _{IH} = 2.0 V, V _{IN} = 0 V, other inputs = 0 V.
V _{IC}	Input Clamping Voltage		-1.2					V	V _{CC} = 4.5 V, I _{IN} = -18 mA, other inputs are open.
I _{IH1}	Logical "1" Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs = 0 V.
I _{IH2}	Logical "1" Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 7.0 V, other inputs = 0 V.
I _{IL}	Logical "0" Input Current	-0.03	-0.6	-0.03	-0.6	-0.03	-0.6	mA	V _{CC} = 5.5 V, V _{INL} = 0.5 V, V _{IN} = 5.5 V.
I _{OD}	Diode Current	60		60		60		mA	V _{CC} = 4.5 V, V _{IN} (pins 9, 10) = 5.5 V, other inputs are open, V _{OUT} = 2.5 V.
I _{OS}	Output Short Circuit Current	-60	-150	-60	-150	-60	-150	mA	V _{CC} = 5.5 V, V _{IN} = 0 V (all inputs), V _{OUT} = 0 V.
I _{CCH}	Power Supply Current		2.8		2.8		2.8	mA	V _{CC} = 5.5 V, V _{IN} = 0 V (all inputs).
I _{CCL}	Power Supply Current		4.7		4.7		4.7	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V (all inputs).
V _{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 5.0 V, V _{INL} = 0.5 V, and V _{INH} = 2.5 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL}	Propagation Delay /Data-Output Output <u>High-Low</u>	1.5	4.5	1.0	6.5	1.0	6.5	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 500 Ω.
t _{PLH}	Propagation Delay /Data-Output Output <u>Low-High</u>	1.5	6.0	1.0	8.0	1.0	8.0	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 500 Ω.