M82384
CLOCK GENERATOR AND RESET INTERFACE FOR MILITARY 386™ PROCESSORS

Military

- **Generates All Clock Signals for M386™ Processors**
- **Generates Synchronous Reset from Schmitt-Trigger Input**
- **Generates Address Status Signal Synchronous to CLK**
- **CHMOS III Technology**
- **Uses Crystal or TTL Signal for Frequency Source**
- **Military Temperature Range: −55°C to +125°C (T_C)**
- **18-Pin Cerdip Package and 28-Pin Leadless Chip Carrier**
  (See Packaging Specification, Order #231369)
- **16 MHz Operation**

INTRODUCTION

The M82384 combines a third-overtone crystal oscillator, reset synchronizing circuitry, and address status circuitry onto a single chip for easy timing and control of Military 386 microprocessor-based systems.

The M82384 contains a clock generator/driver that provides two clock signals for the Military 386 microprocessor-based systems. The CLK2 signal generated by the M82384 meets the Military 386 processor CLK2 requirements, and the CLK signal indicates the Military 386 processor phase. The M82384 also generates a synchronous reset signal from a schmitt-trigger reset input, and provides an Address Status signal that has guaranteed setup and hold timing with respect to the CLK output.

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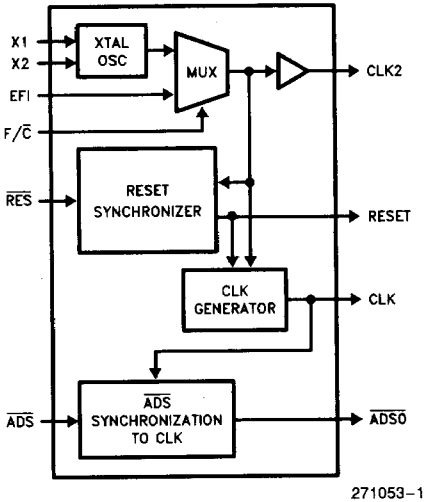

Figure 1. Block Diagram

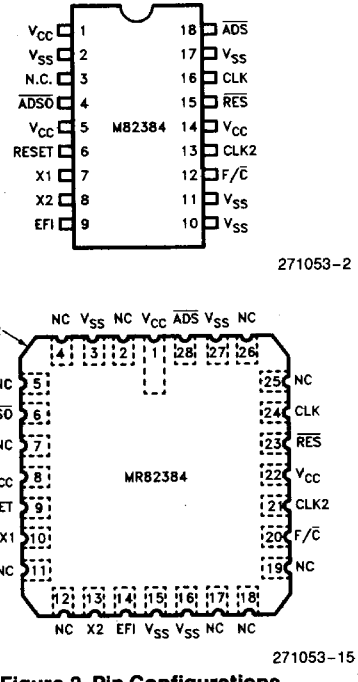

Figure 2. Pin Configurations

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Order Number: 271053-005

1.0 SIGNAL DESCRIPTION

Table 1 gives a brief description of the M82384 input and output signals arranged by functional groups.

Table 1. Signal Descriptions

Symbol*	Input/ Output	Name and Function
F/$\overline{C}$	I	**Frequency/Crystal Select** is a strapping option to select the source for the CLK2 and CLK outputs. When F/$\overline{C}$ is strapped low, the crystal and internal crystal oscillator drives these outputs. When F/$\overline{C}$ is strapped high, the EFI signal drives these outputs.
X1, X2,	I	**Crystal In** are the connections to which a parallel-resonant third-overtone crystal is connected to the internal oscillator. When F/$\overline{C}$ is strapped low, the internal oscillator will drive the CLK2 output at the crystal frequency. The third overtone frequency must be twice the desired processor frequency.
EFI	I	**External Frequency In** accepts a TTL-level signal to drive CLK2 and CLK when the F/$\overline{C}$ input is strapped high. The EFI input frequency must be twice the desired processor frequency.
CLK2	O	**CLK2** is the timing signal used by the M386 processor and support circuits that must be synchronous with the processor. The frequency of CLK2 is twice the M386 processor frequency. CLK2 can drive both TTL-level and MOS-level inputs.
CLK	O	**CLK** is half the CLK2 frequency and indicates the phase of the M386 microprocessor's internal clock. CLK goes low during M386 microprocessor's phase 1 and high during M386 microprocessor's phase 2. CLK can also be used to drive M80286 support components which may be present in the system.
$\overline{RES}$	I	**Reset In** is an active low input signal which generates the RESET output synchronously to CLK2. Signals into $\overline{RES}$ may be applied asynchronously to CLK2. $\overline{RES}$ is synchronized to CLK2 internally. A schmitt-trigger input is provided on $\overline{RES}$ so that an RC circuit can be used to provide a single reset pulse on the RESET output.
RESET	O	**Reset** is an active high output derived from the $\overline{RES}$ input. RESET is synchronous to CLK2. RESET is used to initialize the M386 processor and surrounding circuitry. At the rising edge of its RESET output signal, the M82384 synchronizes the phase of its CLK output with the phase the M386 processor will have after the M82384 negates RESET (See **2.5 Reset Operation**).
$\overline{ADS}$	I	**Address Status** is the active low input used to synchronize the $\overline{ADS}$ output of the M386 microprocessor with the CLK output of the M82384. Therefore, M386 microprocessor's $\overline{ADS}$ output signal should be connected to this input when the $\overline{ADSO}$ output signal is required.
$\overline{ADSO}$	O	**Address Status Output** is the active low output providing an address status signal synchronous to CLK, as timing parameters t21 and t22 indicate in Tables 5 and 6. $\overline{ADSO}$ is generated from the $\overline{ADS}$ input.
V_{CC}	I	**+5V Power Supply** inputs should all be connected to V_{CC}.
V_{SS} (GND)	I	**Ground** inputs should all be connected to 0V.
N.C.	—	**No Connect** pins should remain completely unconnected.

2.0 FUNCTIONAL DESCRIPTION

2.1 Oscillator

The oscillator circuit for the M82384 is a third-overtone crystal oscillator. The output of the oscillator is internally buffered and amplified to become the CLK2 output. The crystal frequency chosen should be twice the required processor frequency. The recommended crystal characteristics are shown in Table 2.

Table 2. Recommended Crystal Specifications

Crystal Wattage:	Crystal should be capable of dissipating 1 mW
Maximum Shunt Capacitance:	7 pF
Maximum Series Resistance:	40Ω
Resonance:	Third-overtone parallel-resonant (third-overtone series-resonant can be also used, but frequency may be 0.01% from nominal frequency)

The X1 and X2 inputs are the oscillator crystal connections. For stable operation of the oscillator, the tank oscillator circuit shown in Figure 3 is recommended. The sum of the stray board capacitances and loading capacitors should equal the values shown. It is advisable to limit stray board capacitance between the X1 and X2 pins to less than 10 pF.

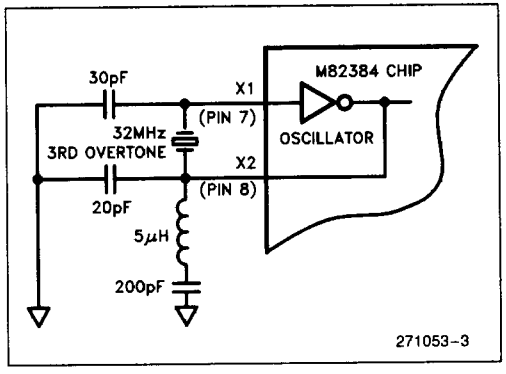

Figure 3. Crystal Oscillator Connections

Compared to fundamental frequency oscillators (such as the M82284), third overtone oscillators such as the M82384 may require slightly longer to begin oscillation and stabilize. Whereas fundamental oscillators require approximately 1 ms for this purpose, third overtone oscillators may require approximately 1 to 3 ms to stabilize.

2.2 CLK2 Generator

The CLK2 output provides the basic timing control for an M386 microprocessor-based system. CLK2 has output characteristics to meet MOS drive levels of the M386 microprocessor's CLK2 input. CLK2 is generated by either a crystal and the internal crystal oscillator or by an external signal on the EFI input, as selected by the F/$\overline{C}$ strapping option. When F/$\overline{C}$ is strapped low, the crystal oscillator drives the CLK2 output. When F/$\overline{C}$ is strapped high, the EFI input drives the CLK2 output.

SPECIAL NOTE ON EFI INPUT: When using the EFI input to create CLK2 minimum high and minimum high low times required by the M386 microprocessor, the EFI input must be driven with minimum high and low times shown by AC parameters t14 and t15, respectively. Note that the values of t14, t15 and achievable rise/fall times require the EFI input frequency to be somewhat less than 32 MHz for compatibility with M386 microprocessor's CLK2 high time and low time requirements.

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2.3 CLK Generator

The M82384 provides a second timing output, CLK, to indicate the phase of the M386 microprocessor. CLK is CLK2 divided by two. CLK has a duty cycle of 50% and MOS output drive characteristics.

As shown in Figure 7, CLK is synchronized to the phase the M386 microprocessor will have after the M82384 RESET output is negated. CLK goes low during phase 1 of the M386 microprocessor's bus state. CLK goes high during phase 2 of the M386 microprocessor's bus state. Since the phase of the M386 microprocessor will not change except during reset, the phase of the M82384 CLK output will not change except at the rising edge of the M82384 RESET output.

2.4 CLK2 and CLK Termination

The CLK2 and CLK outputs have very fast rise and fall times. They are both capable of driving loads up to 160 pF within the delay times specified in Tables 5 and 6. Due to the sharp level transitions these outputs generate, they require proper termination on the printed circuit board to avoid signal reflections and ringing.

Proper termination can be implemented by series resistor termination, and, if necessary, by a small load capacitor to bring the capacitive load up to a minimum of 80 pF. The appropriate termination components are illustrated in Figure 4. Note that the loading capacitor shown in Figure 4 is needed only if the signal load would otherwise be less than 80 pF. In such a case, the load capacitor value should be chosen to bring the total signal load to a minimum of 80 pF. The appropriate value of the series resistor terminator is based on the total signal capacitance (including load capacitor if any), and can be determined according to the graph in Figure 5.

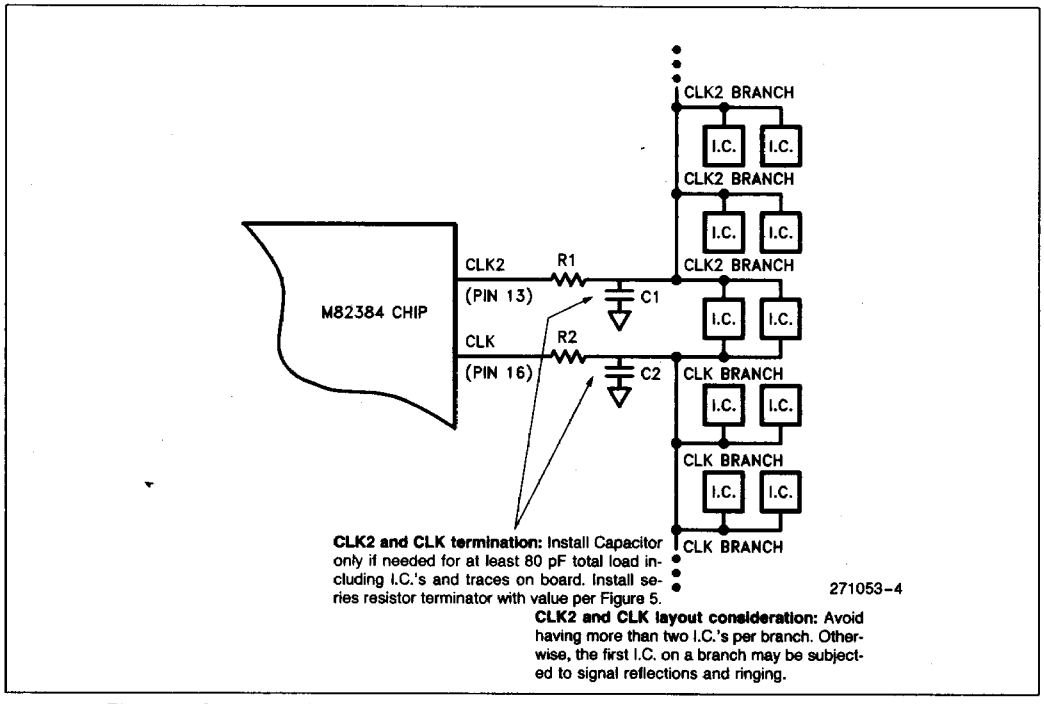

Figure 4. CLK2 and CLK Series Resistor Terminators and Layout Recommendation

When laying out the CLK2 and CLK signal paths of the printed circuit board, place the series resistor termination immediately next to the M82384. Place the capacitor, if it is needed, immediately after the series resistor terminator. Attempt to layout the remaining portion of the CLK2 and CLK signal traces in a branch or star arrangement, such that the capacitive loading and trace length of each branch is approximately equal to the other branches of the same signal.

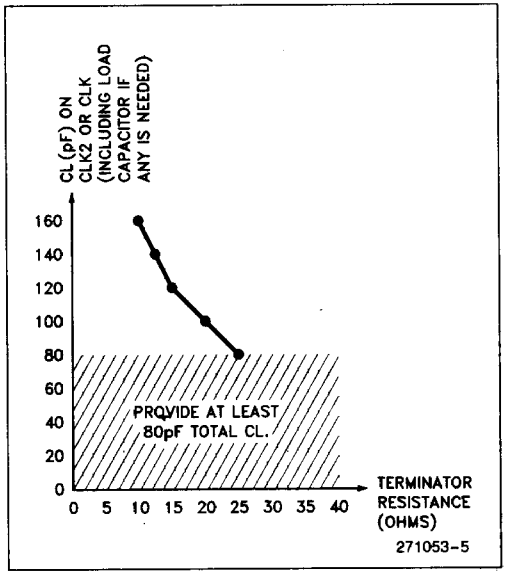

Figure 5. Values for Series Resistor Terminators

2.5 Reset Operation

The reset logic provides a RESET ouput to force the system into a known initial state. When the $\overline{RES}$ input is asserted the RESET output is asserted.

$\overline{RES}$ is synchronized to CLK2 internally at the rising edge of CLK2 before generating the RESET output. Synchronization of the $\overline{RES}$ input produces a delay of one or two CLK2 periods before the RESET output is affected.

At power up, a system does not have stable V_{CC} and CLK2 signals. To prevent spurious activity, $\overline{RES}$ should be asserted until V_{CC} and CLK2 stabilize at their operating values. The M386 microprocessors and other circuits also require RESET be active a minimum number of cycles to guarantee recognition of RESET. An R-C network, as shown in Figure 6, will keep $\overline{RES}$ asserted long enough to satisfy both needs.

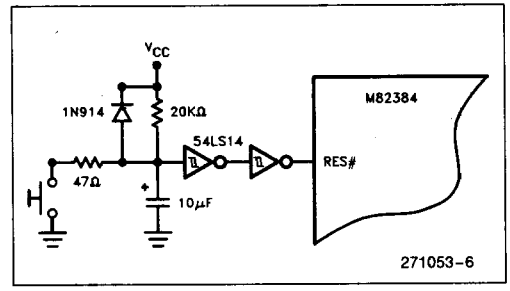

Figure 6. Typical R-C Reset Timing Circuit (Including Schmitt Trigger Interface)

A schmitt trigger input on the $\overline{RES}$ input provides hysteresis to assure a single transition of RESET when $\overline{RES}$ is driven with an R-C circuit such as Figure 6. The hysteresis separates the $\overline{RES}$ input voltage level at which the RESET output switches between high to low from the input level at which the RESET output switches between low to high. The $\overline{RES}$ high to low input transition voltage is lower than the $\overline{RES}$ low to high input transition voltage. The $\overline{RES}$ hysteresis voltage is the voltage difference between these transition levels. Provided the slope of the $\overline{RES}$ input remains in the same direction (increasing or decreasing) around the $\overline{RES}$ input transition levels, the RESET output will make a single transition as desired.

The phase of the M82384 CLK output is set at the rising edge of the RESET output, as shown in Figure 7. CLK is driven low during phase one, and is driven high during phase two. The M82384 then ensures that the falling edge of its RESET output occurs only during phase two of CLK. The M386 microprocessor assumes the falling edge of RESET occurs during phase two (a correct assumption when RESET is generated by the M82384) and sets its internal phase to match the phase of CLK, making the M82384 CLK output an accurate indicator of the M386 microprocessor's internal phase.

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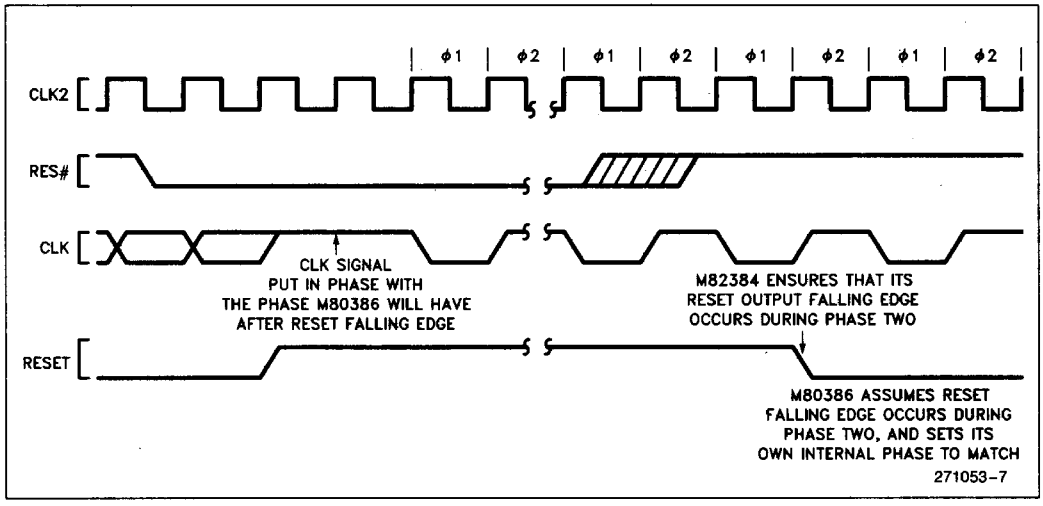

Figure 7. Reset Function

2.6 Address Strobe Operation

The address status logic provides an $\overline{ADSO}$ output signal with setup timing and hold timings specified relative to the CLK signal falling edge. Such timing characteristics can be useful for circuitry being driven from the CLK signal. (Note that the M386 microprocessor provides an $\overline{ADS}$ signal with timings specified relative to the CLK2 rising edge.)

3.0 MAXIMUM RATINGS

Table 3. M82384 Maximum Ratings

Parameter	M82384 Maximum Rating
Storage Temperature	−65°C to +150°C
Case Temperature Under Bias	−55°C to +125°C
Supply Voltage with Respect to V_{SS}	−0.5V to 6.5V
Voltage on Other Pins	0.5V to V_{CC}+0.5V

Table 3 is a stress rating only, and functional operation at the maximums is not guaranteed. Functional operating conditions are given in **Table 4, M82384 D.C. Characteristics** and **Tables 5 and 6, M82384 A.C. Characteristics.**

Extended exposure to the Maximum Ratings may affect device reliability. Furthermore, although the M82384 contains protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

4.0 Operating Conditions

Symbol	Description	Min	Max	Units
T_C	Case Temperature (Instant On)	−55	+125	°C
V_{CC}	Digital Supply Voltage	4.75	5.25	V

5.0 D.C. SPECIFICATIONS (Over Specified Operating Conditions)

Table 4. M82384 D.C. Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.4		V	
V_{ILE}	EFI Input Low Voltage		0.6	V	
V_{IHR}	$\overline{RES}$ Input High Voltage	2.6		V	
V_{OL}	Output Low Voltage		0.45	V	at I_{OL} = 5 mA
V_{OH}	Output High Voltage	2.4		V	at I_{OH} = −1 mA
V_{OLC2}	CLK2 Output Low Voltage		0.45	V	at I_{OL} = 8 mA
V_{OHC2}	CLK2 Output High Voltage	V_{CC}−0.6		V	at I_{OH} = −1 mA
V_{OLC}	CLK Output Low Voltage		0.45	V	at I_{OL} = 5 mA
V_{OHC}	CLK Output High Voltage	4.0		V	at I_{OH} = −1 mA
I_{LI}	Input Leakage Current		±10	μA	0V ≤ V_{in} ≤ V_{CC}
I_{CC}	Supply Current		105	mA	
C_I	Input Capacitance		10	pF	FC = 1 MHz

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6.0 A.C. SPEC DEFINITIONS

The A.C. specifications, given in Tables 5 and 6, consist of output delays, input setup requirements, and input hold requirements. Inputs must be driven to the voltage levels indicated in Figure 8 when A.C. specifications are measured. M82384 output delays are specified with minimum and maximum limits, measured as shown. The M82384 minimum delay times are also "hold times" provided to external circuitry. M82384 input setup and hold times for synchronous inputs are specified as minimums, defining the smallest acceptable sampling window. Within the sampling window, a synchronous input signal must be stable for correct M82384 operation. A special case, specifying setup and hold times (t21 and t22) for the $\overline{ADSO}$ output signal is present to relate the $\overline{ADSO}$ output timing with that of the CLK output.

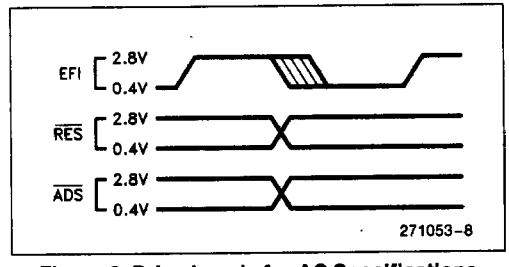

Figure 8. Drive Levels for AC Specifications

7.0 A.C. SPECIFICATIONS (Over Specified Operating Conditions)

Table 5. M82384-16 A.C. Characteristics

NOTE: To guarantee compatibility with all speed selections of the M386 microprocessor, parameters t2a, t2b, t3a, t3b, t9, t10, t14 and t15 are specified for each speed selection of the M386 microprocessor.

Symbol	Parameter	M82384-16 Min	M82384-16 Max	Unit	Ref. Figure	Notes
t1	CLK2 Period	31		ns		
t2a	CLK2 High Time (at 32 MHz)	9		ns	10	at 2V; C_L = 160 pF
t2b	CLK2 High Time (at 32 MHz)	5		ns	10	at (V_{CC} − 0.8V); C_L = 160 pF
t3a	CLK2 Low Time (at 32 MHz)	9		ns	10	at 2.0V; C_L = 160 pF
t3b	CLK2 Low Time (at 32 MHz)	7		ns	10	at 0.8V; C_L = 160 pF
t4	CLK2 Fall Time		8	ns	10	from (V_{CC} − 0.8V) to 0.8V); C_L = 160 pF
t5	CLK2 Rise Time		8	ns	10	from 0.8V to (V_{CC} − 0.8V); C_L = 160 pF
t6	CLK Delay from CLK2	1	15	ns	11	(Note 1)
t7	CLK Fall Time		10	ns	10	from 3.5V to 1V
t8	CLK Rise Time		10	ns	10	from 1V to 3.5V
t9	CLK Low Time (at 16 MHz)	15		ns	10	at 0.6V; C_L = 160 pF
t10	CLK High Time (at 16 MHz)	20		ns	10	at 3.8V; C_L = 160 pF
t11	EFI to CLK2 Delay		30	ns	11	C_L = 160 pF
t12	EFI Fall Time		3	ns	10	from 2.4V to 0.6V
t13	EFI Rise Time		3	ns	10	from 0.6V to 2.4V
t14	EFI Low Time (at 32 MHz)	17		ns	10	at 0.6V
t15	EFI High Time (at 32 MHz)	15		ns	10	at 2.4V
t16	$\overline{RES}$ Setup Time to CLK2	17		ns	12	
t17	$\overline{RES}$ Hold Time from CLK2	0		ns	12	
t18	RESET Delay from CLK2	4	18	ns	13	C_L = 125 pF
t19	$\overline{ADS}$ Input Delay	5	34	ns	14	
t20	$\overline{ADSO}$ Setup to CLK	16		ns	14	C_L = 125 pF
t21	$\overline{ADSO}$ Hold from CLK	16		ns	14	

NOTE:
1. Capacitive loads on CLK2 and CLK should each be between 80 pF and 160 pF.

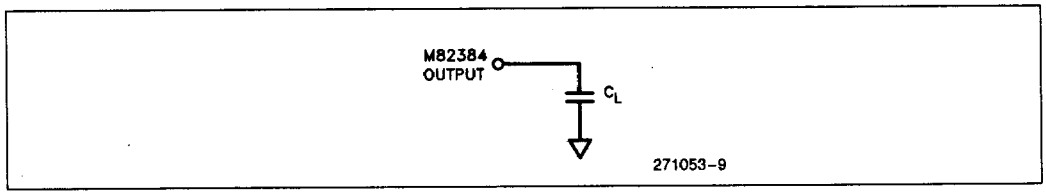

Figure 9. AC Test Load

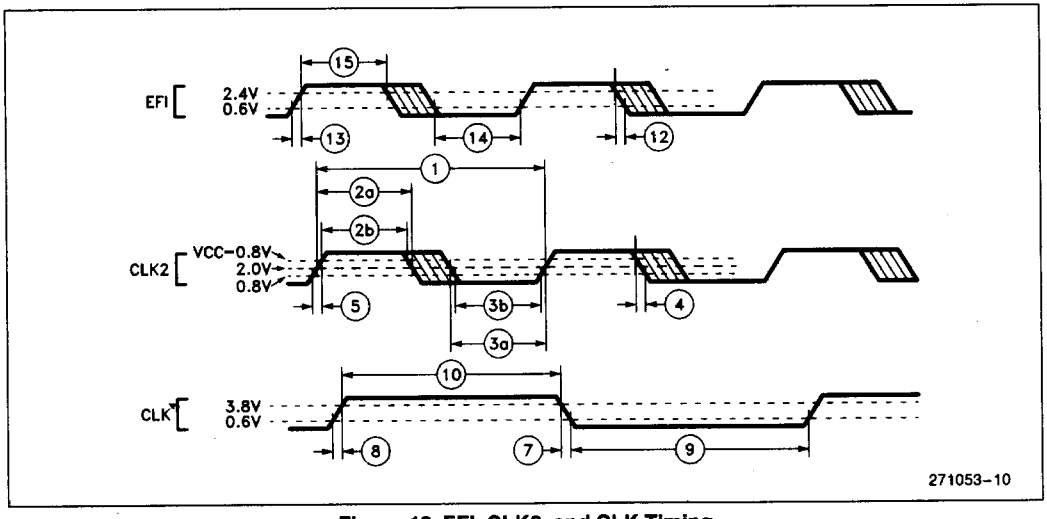

Figure 10. EFI, CLK2, and CLK Timing

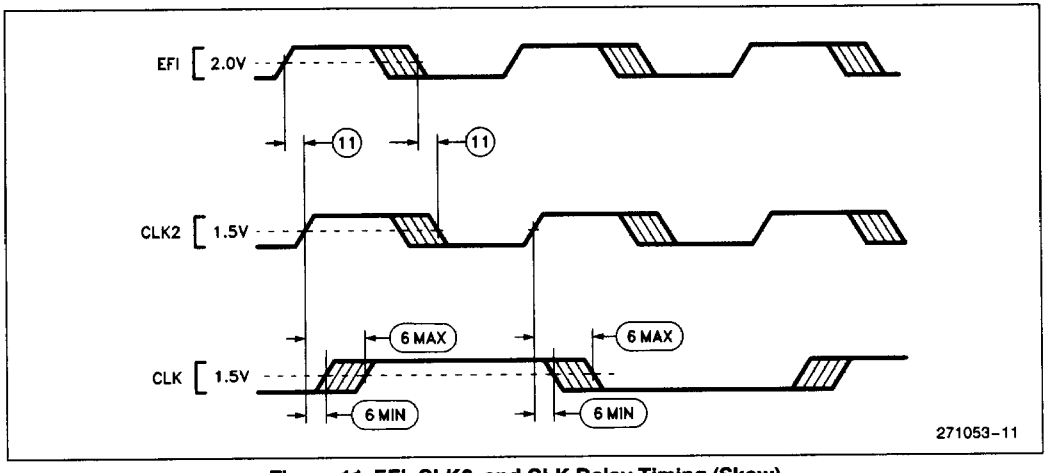

Figure 11. EFI, CLK2, and CLK Delay Timing (Skew)

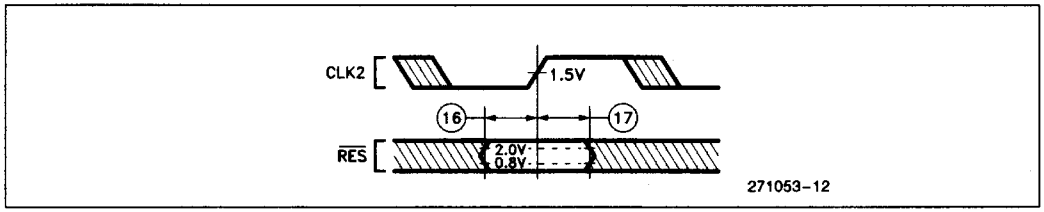

Figure 12. $\overline{RES}$ Input Setup and Hold Timing

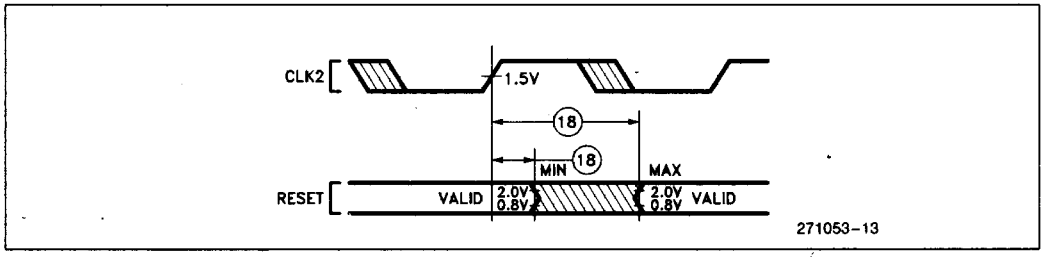

Figure 13. RESET Output Valid Delay Timing

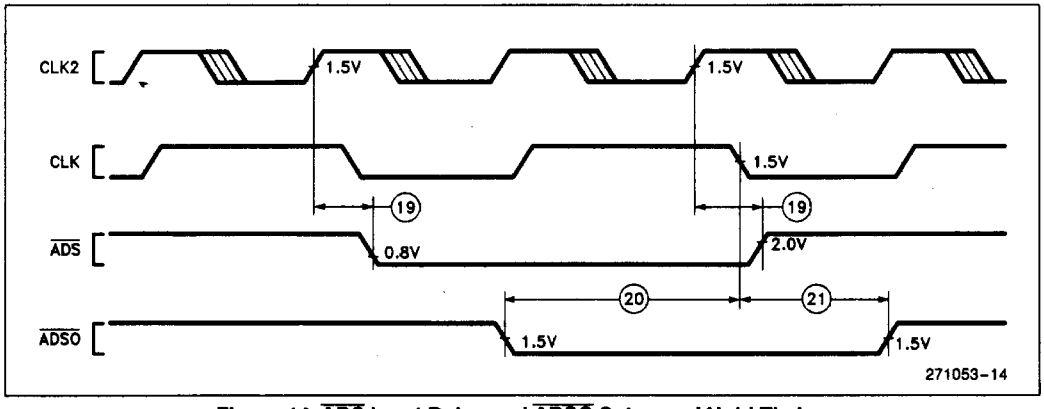

Figure 14. $\overline{ADS}$ Input Delay and $\overline{ADSO}$ Setup and Hold Timing