FINAL

Am29F010

1 Megabit (131,072 x 8-Bit) CMOS 5.0 Volt-only, Sector Erase Flash Memory

DISTINCTIVE CHARACTERISTICS

- **5.0 V ± 10% for read and write operations**
  - — Minimizes system level power requirements
- **Compatible with JEDEC-standards**
  - — Pinout and software compatible with single-power-supply Flash
  - — Superior inadvertent write protection
- **32-pin PLCC**
  32-pin TSOP
  32-pin PDIP
- **Minimum 100,000 write/erase cycles guaranteed**
- **High performance**
  - — 45 ns maximum access time
- **Sector erase architecture**
  - — Uniform sectors of 16 Kbytes each
  - — Any combination of sectors can be erased. Also supports full chip erase
- **Sector protection**
  - — Hardware method that disables any combination of sector(s) from write or erase operations
- **Embedded Erase™ Algorithms**
  - — Automatically preprograms and erases the chip or any sector
- **Embedded Program™ Algorithms**
  - — Automatically programs and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Low power consumption**
  - — 30 mA maximum active read current
  - — 50 mA maximum program/erase current
- **Enhanced power management for standby mode**
  - — <25 µA typical standby current

5.0 V-only Flash

GENERAL DESCRIPTION

The Am29F010 is a 1 Mbit, 5.0 Volt-only Flash memory organized as 128 Kbytes of 8 bits each. The 1 Mbit of data is divided into 8 sectors of 16 Kbytes for flexible erase capability. The 8 bits of data will appear on DQ0–DQ7. The Am29F010 is offered in 32-pin packages which allows for upgrades to 4 Mbit densities in the same pin out. This device is designed to be programmed in-system with the standard system 5.0 Volt V_{CC} supply. 12.0 Volt V_{PP} is not required for program or erase operations. The device can also be reprogrammed in standard EPROM programmers.

The standard Am29F010 offers access times between 45 ns and 120 ns allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable ($\overline{\text{CE}}$), write enable ($\overline{\text{WE}}$), and output enable ($\overline{\text{OE}}$) controls.

The Am29F010 is entirely command set compatible with the JEDEC single-power-supply Flash standard. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 Volt Flash or EPROM devices.

The Am29F010 is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

This device also features a sector erase architecture. This allows for sectors of memory to be erased and reprogrammed without affecting the data contents of

Publication# **16736** Rev: **F** Amendment/**+1**
Issue Date: **April 1997**

other sectors. A sector is typically erased and verified within one second. The Am29F010 is erased when shipped from the factory.

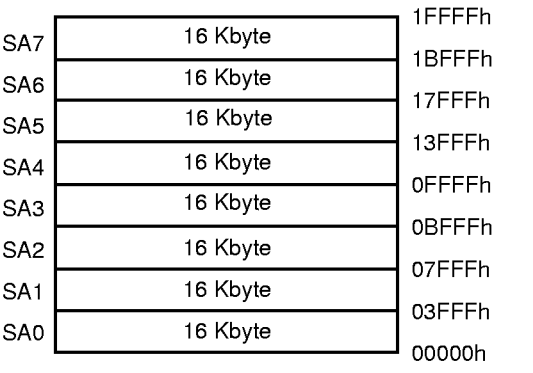
The Am29F010 device also features hardware sector protection. This feature will disable both program and erase operations in any combination of eight sectors of memory.

The device features single 5.0 Volt power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations during power transitions. The end of program or erase is detected by the $\overline{\text{Data}}$ Polling of DQ7 or by the Toggle Bit (DQ6). Once the end of a program or erase cycle has been completed, the device automatically resets to the read mode.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The Am29F010 memory electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

Flexible Sector-Erase Architecture

- Eight 16 Kbyte sectors
- Individual-sector or multiple-sector erase capability
- Sector protection is user definable

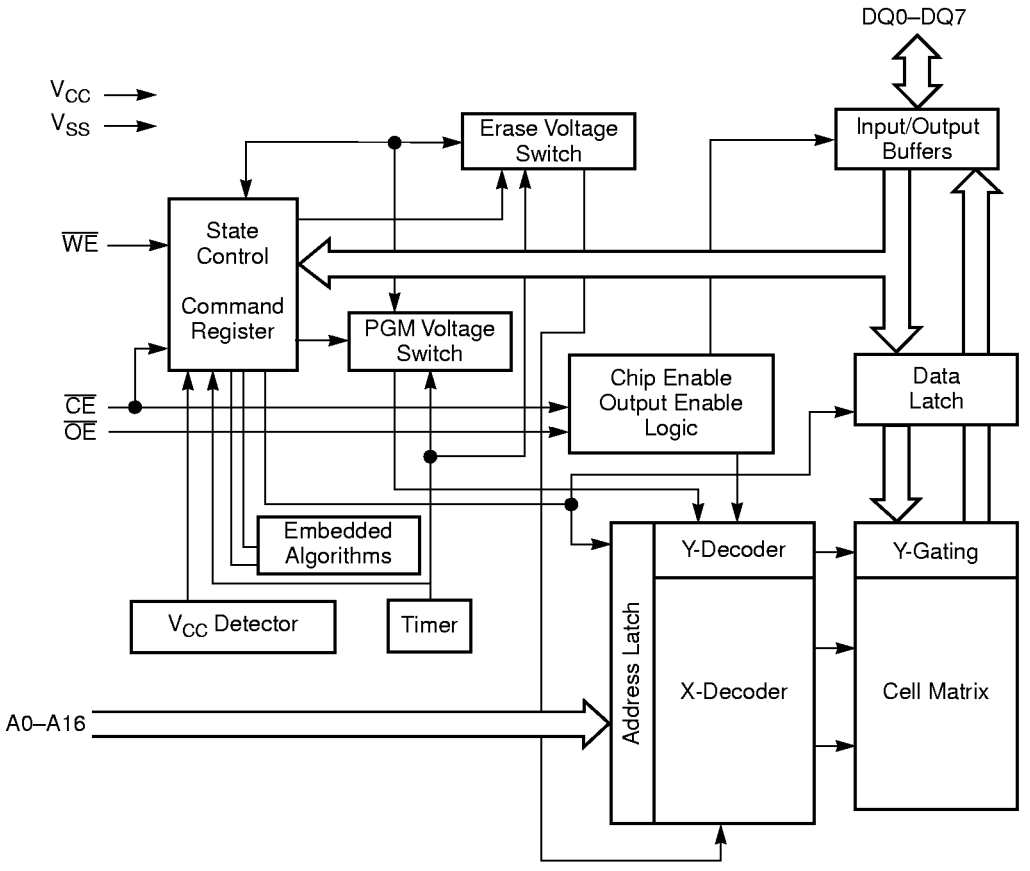


16736F-1

PRODUCT SELECTOR GUIDE

Family Part No:	Am29F010				
Ordering Part No: V_{CC} = 5.0 V ± 5%	**-45**	**-55 (P)**			
V_{CC} = 5.0 V ± 10%		**-55 (J,E,F)**	**-70**	**-90**	**-120**
Max Access Time (ns)	45	55	70	90	120
$\overline{CE}$ ($\overline{E}$) Access (ns)	45	55	70	90	120
$\overline{OE}$ ($\overline{G}$) Access (ns)	25	30	30	35	50

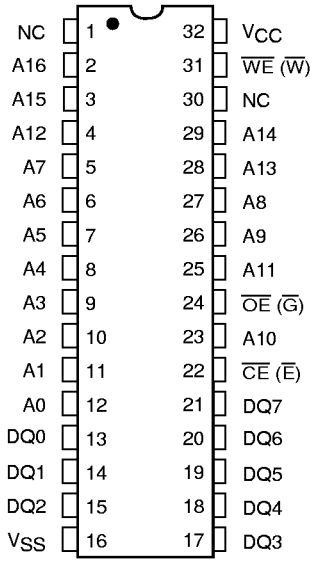
BLOCK DIAGRAM



16736F-2

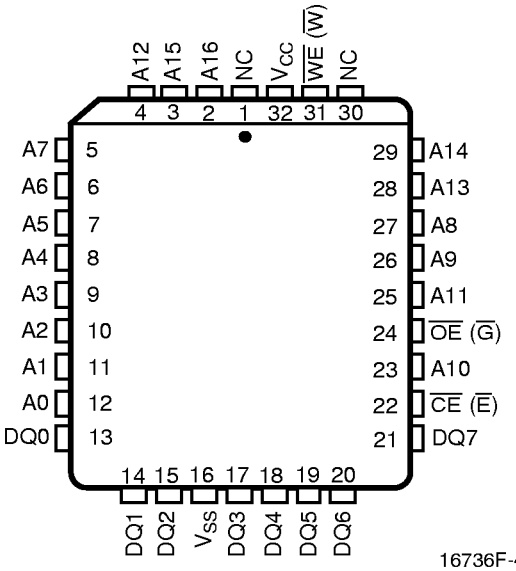
CONNECTION DIAGRAMS

PDIP



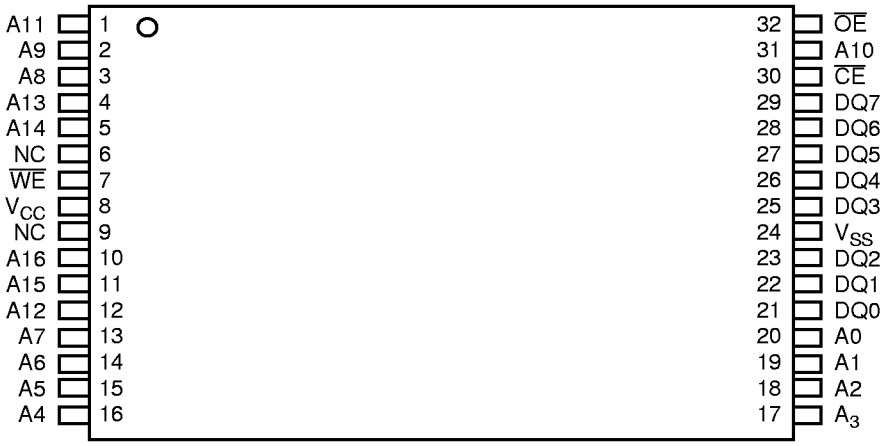
16736F-3

PLCC



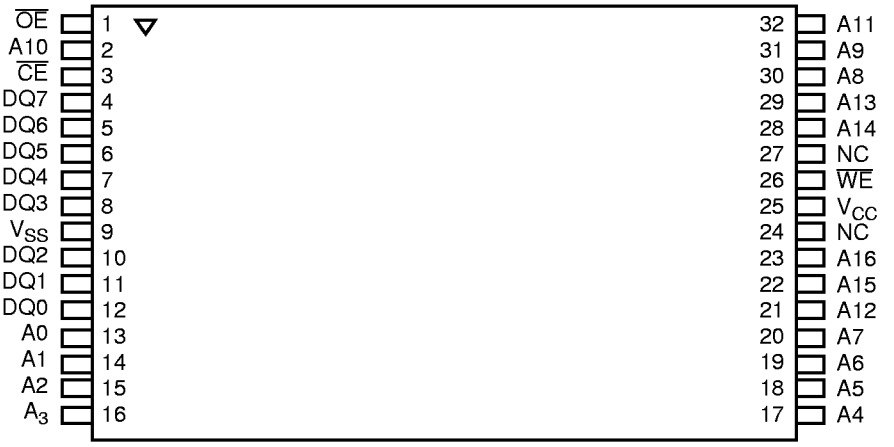
16736F-4

TSOP



29F010 Standard Pinout

16736F-5



29F010 Reverse Pinout

16736F-6

PIN CONFIGURATION

A0–A16 = 17 Addresses

$\overline{CE}$ = Chip Enable

DQ0–DQ7 = 8 Data Inputs/Outputs

NC = Pin Not Connected Internally

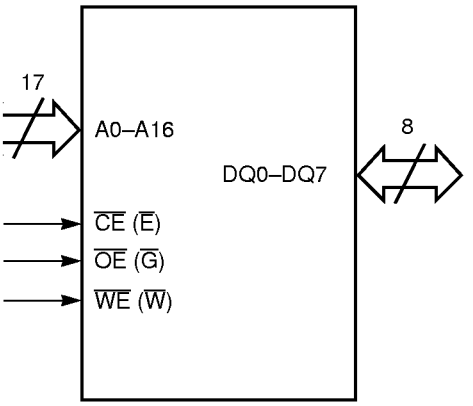
$\overline{OE}$ = Output Enable

V_{CC} = +5.0 Volt Single-Power Supply
(±10% for -55, -70, -90, -120) or
(±5% for -45)

V_{SS} = Device Ground

$\overline{WE}$ = Write Enable

LOGIC SYMBOL

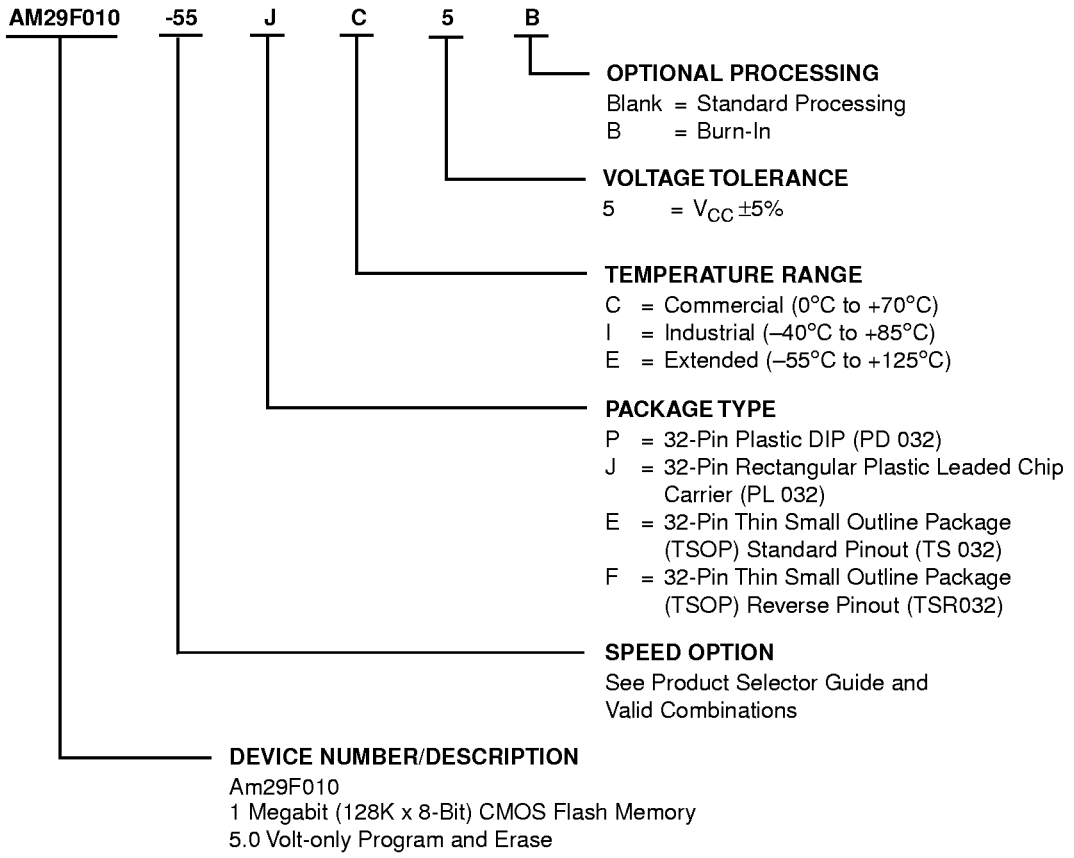


16736F-7

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM29F010-45 V_{CC} = 5.0 V ±5%	PC, JC, EC, FC
AM29F010-55 V_{CC} = 5.0 V ±5%	PC5, PC5B, PI5, PI5B
AM29F010-55 V_{CC} = 5.0 V ±10%	JC, JCB, JI, JIB, EC, ECB, EI, EIB, FC, FCB, FI, FIB
AM29F010-70 AM29F010-90 AM29F010-120	PC, PCB, PI, PIB, PE, PEB, JC, JCB, JI, JIB, JE, JEB, EC, ECB, EI, EIB, EE, EEB, FC, FCB, FI, FIB, FE, FEB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Am29F010 User Bus Operations

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A9	DQ0–DQ7
Autoselect, AMD Manuf. Code (1)	L	L	H	L	L	V_{ID}	Code
Autoselect Device Code (1)	L	L	H	H	L	V_{ID}	Code
Read	L	L	X	A0	A1	A9	D_{OUT}
Standby	H	X	X	X	X	X	HIGH Z
Output Disable	L	H	H	X	X	X	HIGH Z
Write	L	H	L	A0	A1	A9	D_{IN}
Verify Sector Protect (2)	L	L	H	L	H	V_{ID}	Code

Legend:
L = logic 0, H = logic 1, X = Don't Care. See DC Characteristics for voltage levels.

Notes:
1. *Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3.*
2. *Refer to the section on Sector Protection.*

Read Mode

The Am29F010 has two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if the device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable for at least t_{ACC}–t_{OE} time).

Standby Mode

There are two ways to implement the standby mode on the Am29F010 device, both using the $\overline{CE}$ pin.

A CMOS standby mode is achieved with $\overline{CE}$ held at $V_{CC} \pm 0.5$ V. Under this condition the current is typically reduced to less than 25 µA. A TTL standby mode is achieved with $\overline{CE}$ held at V_{IH}. Under this condition the current is typically reduced to 1 mA.

In the standby mode the outputs are in the high impedance state, independent of the $\overline{OE}$ input.

Output Disable

With the $\overline{OE}$ input at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The autoselect mode allows the reading of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 12.5 V) on address pin A9.Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from V_{IL} to V_{IH}. All addresses are don't cares except A0 and A1 (see Table 1).

The manufacturer and device codes may also be read via the command register, for instances when the Am29F010 is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 3 (see Autoselect Command Sequence).

Byte 0 (A0 = V_{IL}) represents the manufacturer's code (AMD = 01H) and byte 1 (A0 = V_{IH}) the device identifier code for Am29F010 = 20H. These two bytes are given in the table below. All identifiers for manufacturer and device will exhibit odd parity with DQ7 defined as the parity bit. In order to read the proper device codes when executing the Autoselect, A1 must be V_{IL} (see Table 1).

The autoselect mode also facilitates the determination of sector protection in the system. By performing a read operation at the address location XX02H with the higher order address bits A14, A15, and A16 set to the desired sector address, the device will return 01H for a protected sector and 00H for a non-protected sector.

Table 1. Am29F010 Sector Protection Verify Autoselect Codes

Type	A14 to A16			A1	A0	Code (HEX)	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacturer Code - AMD	X	X	X	V_{IL}	V_{IL}	01H	0	0	0	0	0	0	0	1
Am29F010 Device	X	X	X	V_{IL}	V_{IH}	20H	0	0	1	0	0	0	0	0
Sector Protection	Sector Address			V_{IH}	V_{IL}	01H*	0	0	0	0	0	0	0	1

**Outputs 01H at protected sector addresses*

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later; while data is latched on the rising edge of the $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Sector Protection

The Am29F010 features hardware sector protection. This feature will disable both program and erase operations in any combination of eight sectors of memory. The sector protect feature is enabled using programming equipment at the user's site. The device is shipped with all sectors unprotected. Alternatively, AMD may program and protect sectors in the factory prior to shipping the device (AMD's *ExpressFlashService).*

Table 2. Sector Address Table

	A16	A15	A14	Address Range
SA0	0	0	0	00000h-03FFFh
SA1	0	0	1	04000h-07FFFh
SA2	0	1	0	08000h-0BFFFh
SA3	0	1	1	0C000h-0FFFFh
SA4	1	0	0	10000h-13FFFh
SA5	1	0	1	14000h-17FFFh
SA6	1	1	0	18000h-1BFFFh
SA7	1	1	1	1C000h-1FFFFh

It is possible to determine if a sector is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02H, where the higher order address bits A14, A15, and A16 is the desired sector address, will produce a logical "1" at DQ0 for a protected sector. See Table 1 for Autoselect codes.

Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. **Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode.** Table 3 defines the valid register command sequences.

Table 3. Am29F010 Command Definitions

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset/Read	3	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
Autoselect	3	5555H	AAH	2AAAH	55H	5555H	90H	XX00H/ XX01H	01H/20H				
Byte Program	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	PD				
Chip Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H

Notes:

1. *Bus operations are defined in Table .*
2. *RA = Address of the memory location to be read.*
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   SA = Address of the sector to be erased. The combination of A16, A15, and A14 will uniquely select any sector.
3. *RD = Data read from location RA during read operation.*
   PD = Data to be programmed at location PA. Data is latched on the rising edge of $\overline{WE}$.
4. *Address bit A15 = X, X = Don't Care.*
5. *Address bit A16 = X, X = Don't Care for all address commands except for Program Address (PA) and Sector Address (SA).*

Read/Reset Command

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Autoselect Command

Flash memories are intended for use in applications where the local CPU can alter memory contents. As such, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally a desirable system design practice.

The device contains an autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the autoselect command sequence into the command register. Following the command write, a read cycle from address XX00H retrieves the manufacturer code of 01H. A read cycle from address XX01H returns the device code 20H (see Table 1).

All manufacturer and device codes will exhibit odd parity with DQ7 defined as the parity bit.

Furthermore, the write protect status of sectors can be read in this mode. Scanning the sector addresses (A14, A15, and A16) while (A1, A0) = (1, 0) will produce a logical "1" at device output DQ0 for a protected sector.

To terminate the operation, it is necessary to write the read/reset command sequence into the register.

Byte Programming

The device is programmed on a byte-by-byte basis. Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming using the Embedded Program Algorithm. Upon executing the algorithm, the system is *not* required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is completed when the data on DQ7 (also used as $\overline{Data}$ Polling) is equivalent to data written to this bit at which time the device returns to the read mode and addresses are no longer latched (See Table 4, Write Operation Status).

Therefore, the device requires that a valid address to the device be supplied by the system at this particular instance of time for $\overline{\text{Data}}$ Polling operations. $\overline{\text{Data}}$ Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during the Embedded Program Algorithm will be ignored.

Programming is allowed in any sequence and across sector boundaries. Beware that a data "0" cannot be programmed back to a "1". Attempting to do so may cause the device to exceed programming time limits (DQ5 = 1) or result in an apparent success, according to the data polling algorithm, but a read from reset/read mode will show that the data is still "0". Only erase operations can convert "0"s to "1"s.

Figure 1 illustrates the Embedded Programming Algorithm using typical command strings and bus operations.

Chip Erase

Chip erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the chip erase command.

The chip erase command should not be used on devices that use sector erase commands. Likewise, sector erase commands should not be used on devices that use the chip erase command.

Chip erase does *not* require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device will automatically program and verify the entire memory for an all zero data pattern prior to electrical erase. The erase is performed concurrently on all sectors at the same time (see Table "Erase and Programming Performance" for erase times). The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last $\overline{\text{WE}}$ pulse in the command sequence and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to read mode.

Figure 2 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

Sector Erase

Sector erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{\text{WE}}$, while the command (30H) is latched on the rising edge of $\overline{\text{WE}}$. After a time-out of 80 µs from the rising edge of the last sector erase command, the sector erase operation will begin.

Multiple sectors may be erased concurrently by writing the six bus cycle operations as described above. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than 80 µs otherwise that command will not be accepted and erasure will start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 80 µs from the rising edge of the last $\overline{\text{WE}}$ will initiate the execution of the Sector Erase command(s). If another falling edge of the $\overline{\text{WE}}$ occurs within the 80 µs time-out window the timer is reset. (Monitor DQ3 to determine if the sector erase timer window is still open, see section DQ3, Sector Erase Timer.) Any command other than Sector Erase during this period will reset the device to read mode, ignoring the previous command string. In that case, restart the erase on those sectors and allow them to complete.

(Refer to the Write Operation Status Section for DQ3, Sector Erase Timer operation). Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 7).

If the multiple sector erase command is used, multiple sectors should be erased in groups to ensure that a group of sectors is exposed to the same number of program/erase cycles. In addition, the chip erase command should not be used on a device that uses sector erase or multiple sector erase commands.

Sector erase does *not* require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is *not* required to provide any controls or timings during these operations.

The automatic sector erase begins after the 80 µs time out from the rising edge of the $\overline{\text{WE}}$ pulse for the last sector erase command pulse and terminates when the data on DQ7, $\overline{\text{Data}}$ Polling, is "1" (see Write Operation Status section) at which time the device returns to read mode. $\overline{\text{Data}}$ Polling must be performed at an address within any of the sectors being erased.

Figure 2 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

WRITE OPERATION STATUS

Table 4. Write Operation Status

	Status	DQ7	DQ6	DQ5	DQ3	DQ2–DQ0
In Progress	Byte Program in Embedded Program Algorithm	$\overline{DQ7}$	Toggle	0	0	Reserved for future use
	Embedded Erase Algorithm	0	Toggle	0	1	
Exceeded Time Limits	Byte Program in Embedded Program Algorithm	$\overline{DQ7}$	Toggle	1	0	Reserved for future use
	Program/Erase in Embedded Erase Algorithm	0	Toggle	1	1	

Notes:

1. Performing successive read operations from any address will cause DQ6 to toggle.

DQ7
$\overline{\text{Data}}$ Polling

The Am29F010 device features $\overline{\text{Data}}$ Polling as a method to indicate to the host that the embedded algorithms are in progress or completed. During the Embedded Program Algorithm, an attempt to read the device will produce the complement of the data last written to DQ7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ7. During the Embedded Erase Algorithm, an attempt to read the device will produce a "0" at the DQ7 output. Upon completion of the Embedded Erase Algorithm an attempt to read the device will produce a "1" at the DQ7 output. The flowchart for $\overline{\text{Data}}$ Polling (DQ7) is shown in Figure 3.

For chip erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. For sector erase, the $\overline{\text{Data}}$ Polling is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse. $\overline{\text{Data}}$ Polling must be performed at sector addresses within any of the sectors being erased and **not** a sector that is protected. Otherwise, the status may not be valid.

Just prior to the completion of Embedded Algorithm operations DQ7 may change asynchronously while the output enable ($\overline{\text{OE}}$) is asserted low. This means that the device is driving status information on DQ7 at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operations and DQ7 has a valid data, the data outputs on DQ0–DQ6 may be still invalid. The valid data on DQ0–DQ7 can be read on the successive read attempts.

The $\overline{\text{Data}}$ Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm or sector erase time-out (see Table 4).

See Figure 11 for the $\overline{\text{Data}}$ Polling timing specifications and diagrams.

DQ6
Toggle Bit

The Am29F010 also features the "Toggle Bit" as a method to indicate to the host system that the embedded algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{\text{OE}}$ toggling) data from the device *at any address* will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ6 will stop toggling and valid data will be read on *the next* successive attempt. During programming, the Toggle Bit is valid after the rising edge of the fourth $\overline{\text{WE}}$ pulse in the four write pulse sequence. For chip erase, the Toggle Bit is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. For Sector erase, the Toggle Bit is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse. The Toggle Bit is active during the sector erase time-out.

Either $\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggling will cause DQ6 to toggle. See Figure 12 for the Toggle Bit timing specifications and diagrams.

DQ5
Exceeded Timing Limits

DQ5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ5 will produce a "1". This is a failure condition which indicates that the program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is the only operating function of the device under this condition. The $\overline{\text{CE}}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{\text{OE}}$ and $\overline{\text{WE}}$ pins will control the output disable functions as described in Table .

The DQ5 failure condition will also appear if a user tries to program a 1 to a location that is previously programmed to 0. In this case the device locks out and never completes the Embedded Program Algorithm. Hence, the system never reads a valid data on DQ7 bit and DQ6 never stops toggling. Once the device has exceeded timing limits, the DQ5 bit will indicate a

"1." Please note that this is not a device failure condition since the device was incorrectly used. If this occurs, reset the device.

DQ3

Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ3 will remain low until the time-out is complete. $\overline{\text{Data}}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit indicates the device has been written with a valid erase command, DQ3 may be used to determine if the sector erase timer window is still open. If DQ3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by $\overline{\text{Data}}$ Polling or Toggle Bit. If DQ3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 were high on the second status check, the command may not have been accepted.

Refer to Table 4: Write Operation Status.

Data Protection

The Am29F010 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, the Am29F010 locks out write cycles for $V_{CC} < V_{LKO}$ (see DC Characteristics section for voltages). When $V_{CC} < V_{LKO}$, the command register is disabled, all internal program/erase circuits are disabled, and the device resets to the read mode. The Am29F010 ignores all writes until $V_{CC} > V_{LKO}$. The user must ensure that the control pins are in the correct logic state when $V_{CC} > V_{LKO}$ to prevent unintentional writes.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on $\overline{\text{OE}}$, $\overline{\text{CE}}$, or $\overline{\text{WE}}$ will not initiate a write cycle.

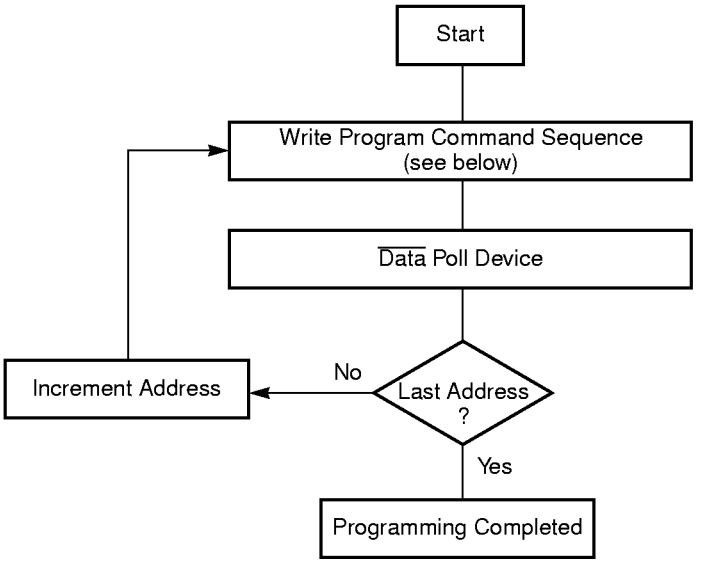
Logical Inhibit

Writing is inhibited by holding any one of $\overline{\text{OE}} = V_{IL}$, $\overline{\text{CE}} = V_{IH}$, or $\overline{\text{WE}} = V_{IH}$. To initiate a write cycle $\overline{\text{CE}}$ and $\overline{\text{WE}}$ must be a logical zero while $\overline{\text{OE}}$ is a logical one.

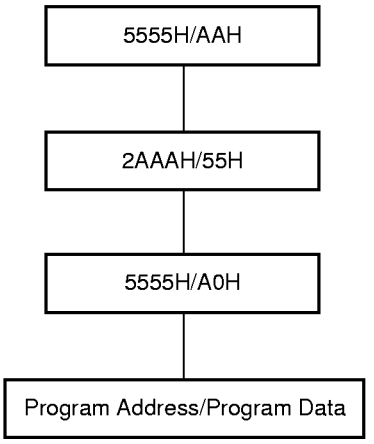
Power-Up Write Inhibit

Power-up of the device with $\overline{\text{WE}} = \overline{\text{CE}} = V_{IL}$ and $\overline{\text{OE}} = V_{IH}$ will not accept commands on the rising edge of $\overline{\text{WE}}$. The internal state machine is automatically reset to the read mode on power-up.

EMBEDDED ALGORITHMS



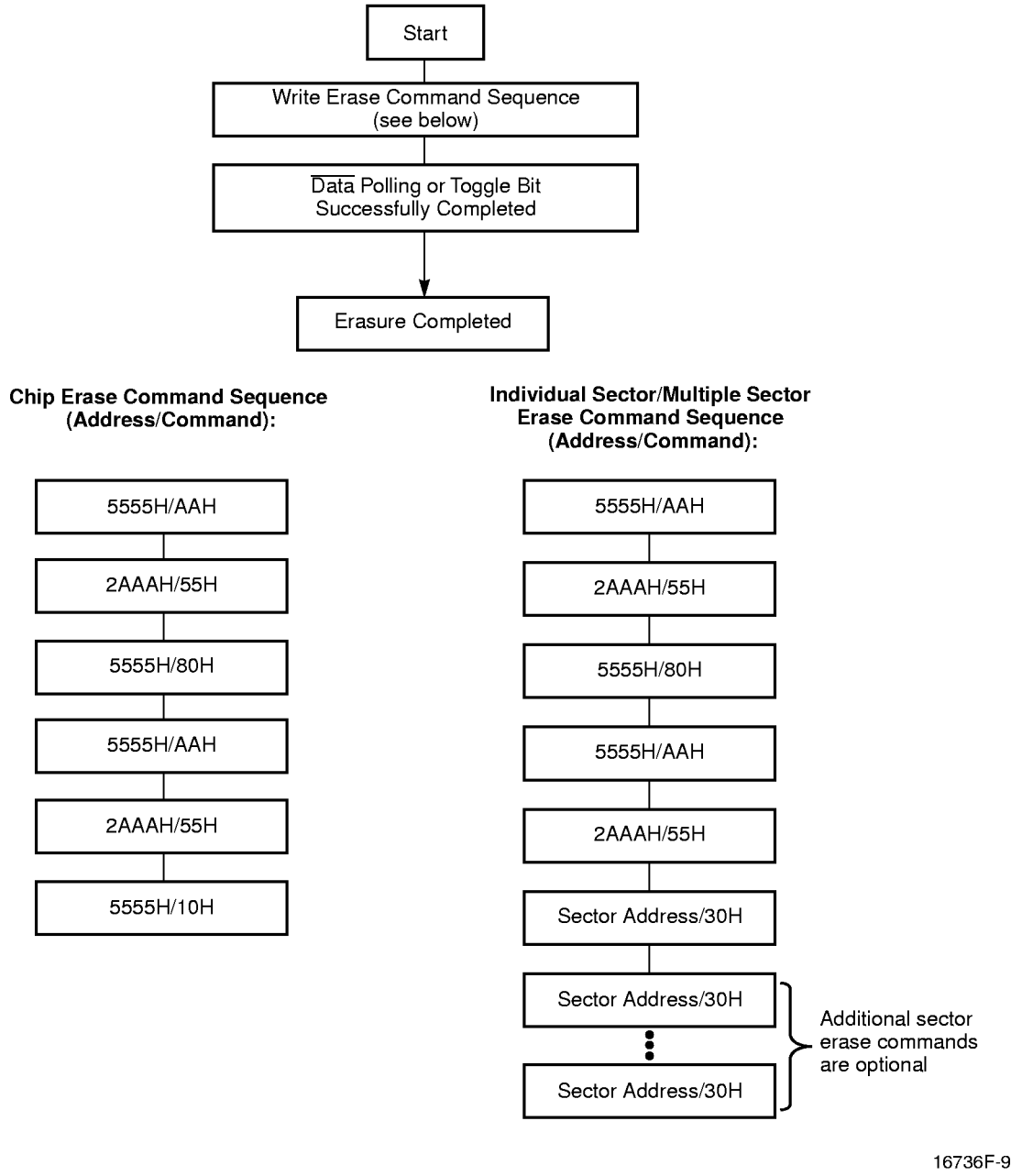
Program Command Sequence (Address/Command):



16736F-8

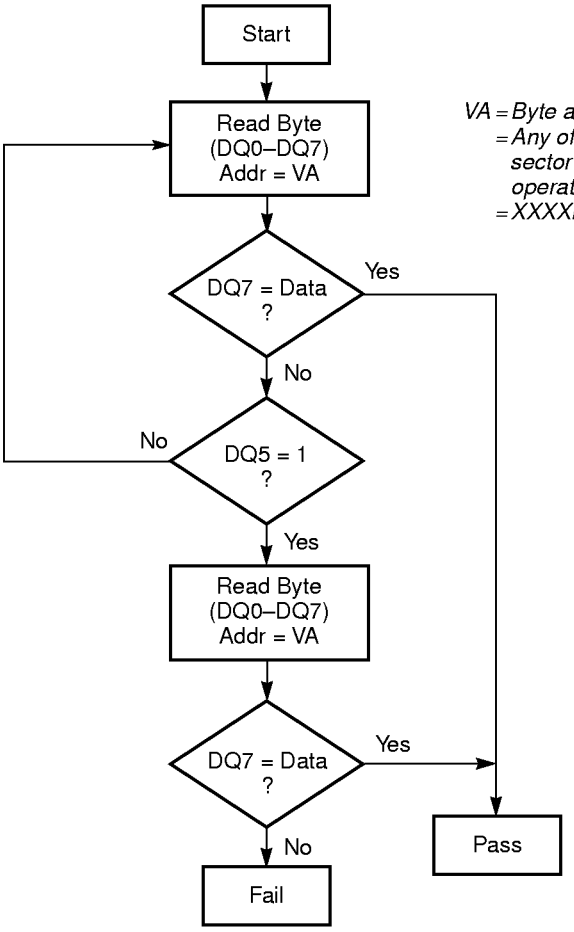
Figure 1. Embedded Programming Algorithm

EMBEDDED ALGORITHMS



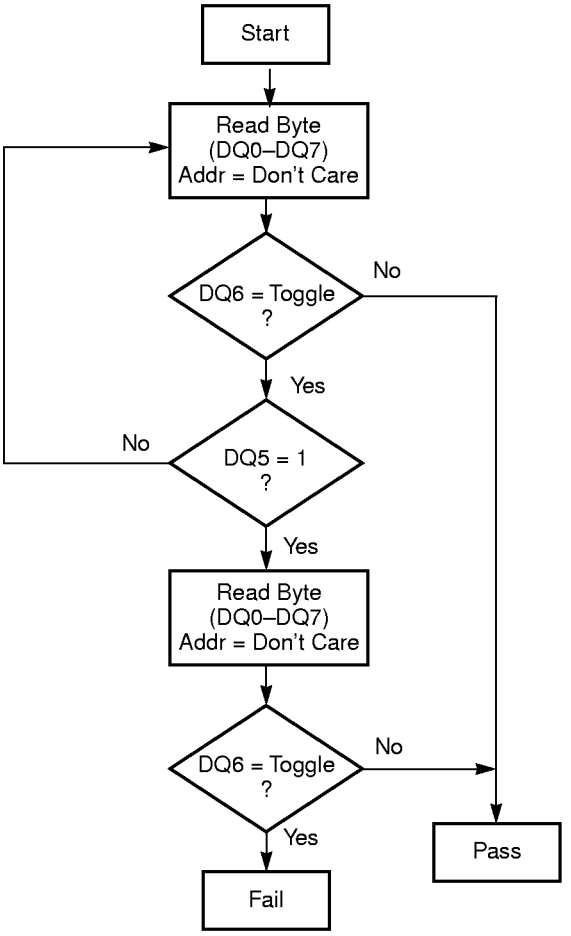
Note:
To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 were high on the second status check, the command may not have been accepted.

Figure 2. Embedded Erase Algorithm



Note:
DQ7 is rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.

Figure 3. $\overline{\text{Data}}$ Polling Algorithm



Note:
DQ6 is rechecked even if DQ5 = "1" because DQ6 may stop toggling at the same time as DQ5 changing to "1".

Figure 4. Toggle Bit Algorithm

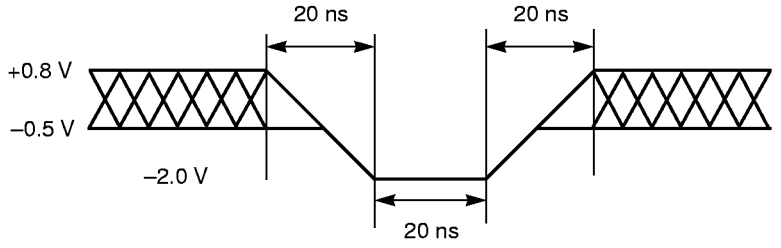


Figure 5. Maximum Negative Overshoot Waveform

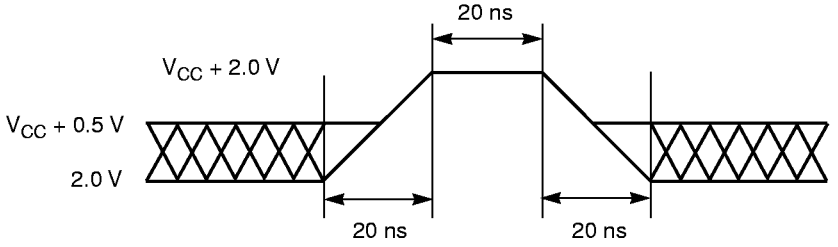


Figure 6. Maximum Positive Overshoot Waveform

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –65°C to +125°C

Ambient Temperature
with Power Applied. . . . . .–55°C to + 125°C

Voltage with Respect To Ground
All pins except A9 (Note 1). . . . . .–2.0 V to +7.0 V

V_{CC} (Note 1). . . . . .–2.0 V to +7.0 V

A9 (Note 2). . . . . .–2.0 V to +14.0 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V. During voltage transitions, input and I/O pins may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *Minimum DC input voltage on A9 pin is –0.5 V. During voltage transitions, A9 may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A). . . . . .0°C to +70°C

Industrial (I) Devices
Ambient Temperature (T_A). . . . . .–40°C to +85°C

Extended (E) Devices
Ambient Temperature (T_A). . . . . .–55°C to +125°C

V_{CC} Supply Voltages
V_{CC} for Am29F010-45, 55 (P). . . . +4.75 V to +5.25 V

V_{CC} for Am29F010-55 (J, E, F),
70, 90, 120 . . . . . –4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

TTL/NMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max		±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC}$ Max, A9 = 12.5 V		50	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max		±1.0	µA
I_{CC1}	V_{CC} Active Current (Note 1)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		30	mA
I_{CC2}	V_{CC} Active Current (Notes 2, 3)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		50	mA
I_{CC3}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IH}$		1.0	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{ID}	Voltage for Autoselect and Sector Unprotect	V_{CC} = 5.0 V	11.5	12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA, $V_{CC} = V_{CC}$ Min		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –2.5 mA, $V_{CC} = V_{CC}$ Min	2.4		V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2	3.7	V

Notes:

1. *The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.*
2. *I_{CC} active while Embedded Program or Erase Algorithm is in progress.*
3. *Not 100% tested.*

DC CHARACTERISTICS (continued)

CMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max		±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC}$ Max, A9 = 12.5 V		50	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max		±1.0	µA
I_{CC1}	V_{CC} Active Current (Note 1)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		30	mA
I_{CC2}	V_{CC} Active Current (Notes 2, 3)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		50	mA
I_{CC3}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{CC} \pm 0.5$ V		100	µA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 0.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 5.0 V	11.5	12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA, $V_{CC} = V_{CC}$ Min		0.45	V
V_{OH1}	Output Low Voltage	I_{OH} = –2.5 mA, $V_{CC} = V_{CC}$ Min	0.85 V_{CC}		V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC}$ Min	V_{CC} – 0.4		V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2		V

Notes:

1. *The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.*
2. *I_{CC} active while Embedded Program or Erase Algorithm is in progress.*
3. *Not 100% tested.*

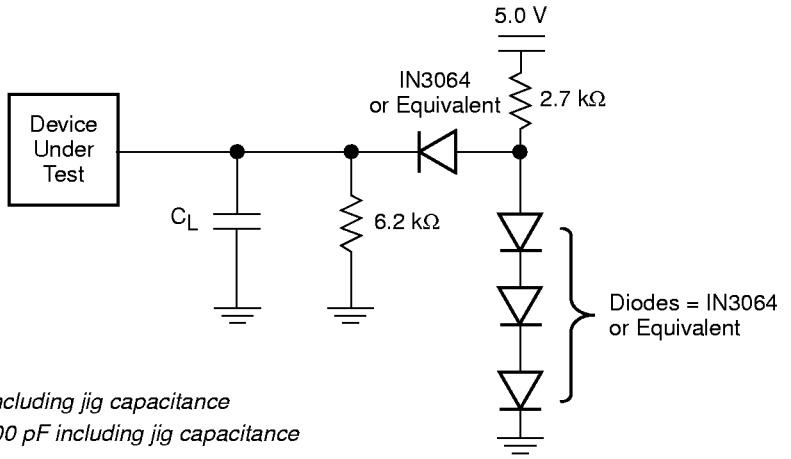
AC CHARACTERISTICS

Read Only Operations Characteristics

Parameter Symbols		Description	Test Setup		-45 (Note 1)	-55 (Note 2)	-70 (Note 2)	-90 (Note 2)	-120 (Note 2)	Unit
JEDEC	Standard									
t_{AVAV}	t_{RC}	Read Cycle Time (Note 4)		Min	45	55	70	90	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	Max	45	55	70	90	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Max	45	55	70	90	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		Max	25	30	30	35	50	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Notes 3, 4)		Max	10	15	20	20	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Notes 3, 4)		Max	10	15	20	20	30	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First		Min	0	0	0	0	0	ns

Notes:

1. *Test Conditions:*
   Output Load: 1 TTL gate and 30 pF
   Input rise and fall times: 5 ns
   Input pulse levels: 0.0 V to 3.0 V
   Timing measurement reference level
   Input: 1.5 V
   Output: 1.5 V
2. *Test Conditions:*
   Output Load: 1 TTL gate and 100 pF
   Input rise and fall times: 20 ns
   Input pulse levels: 0.45 V to 2.4 V
   Timing measurement reference level
   Input: 0.8 and 2.0 V
   Output: 0.8 and 2.0 V
3. *Output driver disable time.*
4. *Not 100% tested.*



Notes:

For -45: C_L = 30 pF including jig capacitance

For all others: C_L = 100 pF including jig capacitance

16736F-14

Figure 7. Test Conditions

AC CHARACTERISTICS

Write/Erase/Program Operations

Parameter Symbols		Description			-45	-55	-70	-90	-120	Unit
JEDEC	Standard									
t_{AVAV}	t_{WC}	Write Cycle Time (Note 2)		Min	45	55	70	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	35	45	45	45	50	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	20	20	30	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time	Read (Note 2)	Min	0	0	0	0	0	ns
			Toggle Bit and $\overline{Data}$ Polling (Note 2)	Min	10	10	10	10	10	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write ($\overline{OE}$ High to $\overline{WE}$ Low)		Min	0	0	0	0	0	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time		Min	0	0	0	0	0	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time		Min	0	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	25	30	35	45	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	20	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation		Typ	14	14	14	14	14	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)		Typ	1.3	1.3	1.3	1.3	1.3	sec
	t_{VCS}	V_{CC} Setup Time (Note 2)		Min	50	50	50	50	50	µs
	t_{VLHT}	Voltage Transition Time (Note 2)		Typ	4	4	4	4	4	µs
	t_{OESP}	$\overline{OE}$ Setup Time to $\overline{WE}$ Active (Note 2)		Typ	4	4	4	4	4	µs

Notes:

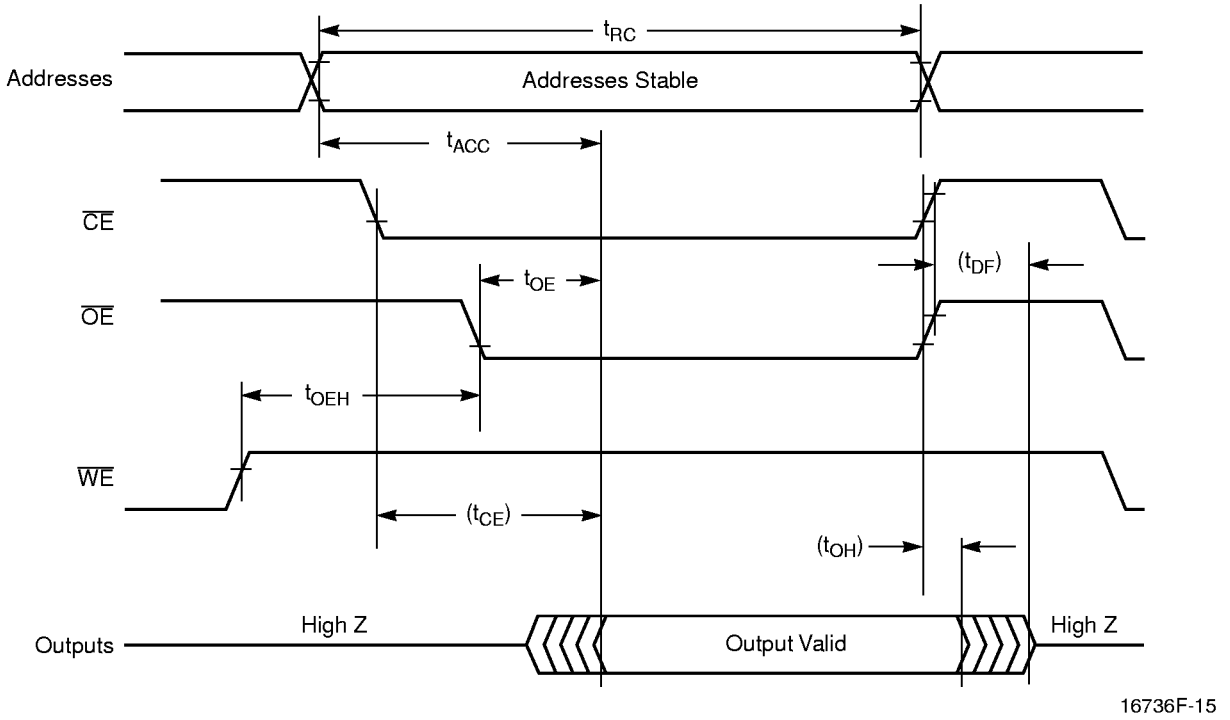
1. *This does not include the preprogramming time.*
2. *Not 100% tested.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

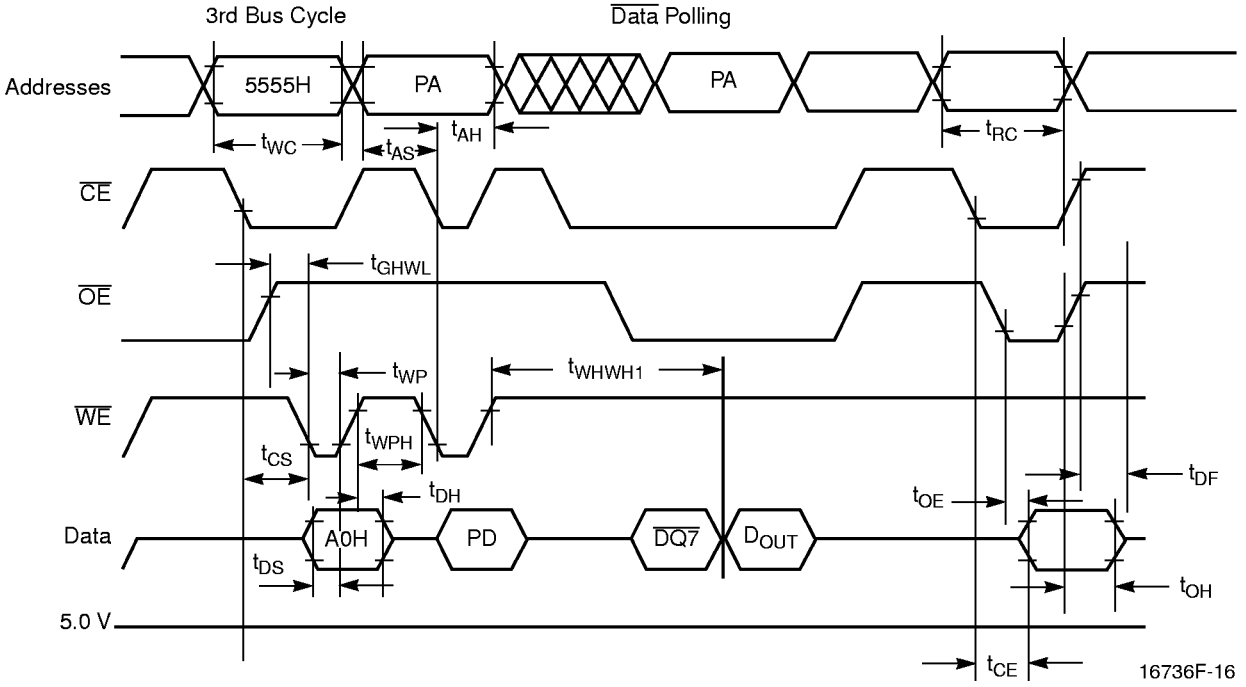
SWITCHING WAVEFORMS



16736F-15

Figure 8. AC Waveforms for Read Operations

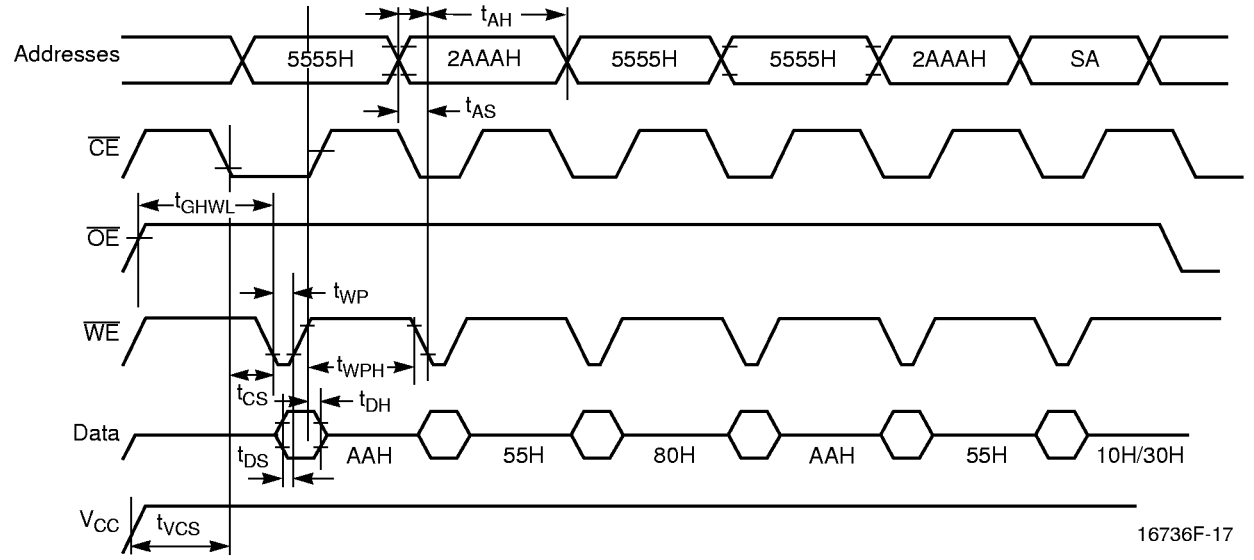
SWITCHING WAVEFORMS



Notes:

1. *PA is address of the memory location to be programmed.*
2. *PD is data to be programmed at byte address.*
3. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
4. *D_{OUT} is the output of the data written to the device.*
5. *Figure indicates last two bus cycles of four bus cycle sequence.*

Figure 9. Program Operation Timings

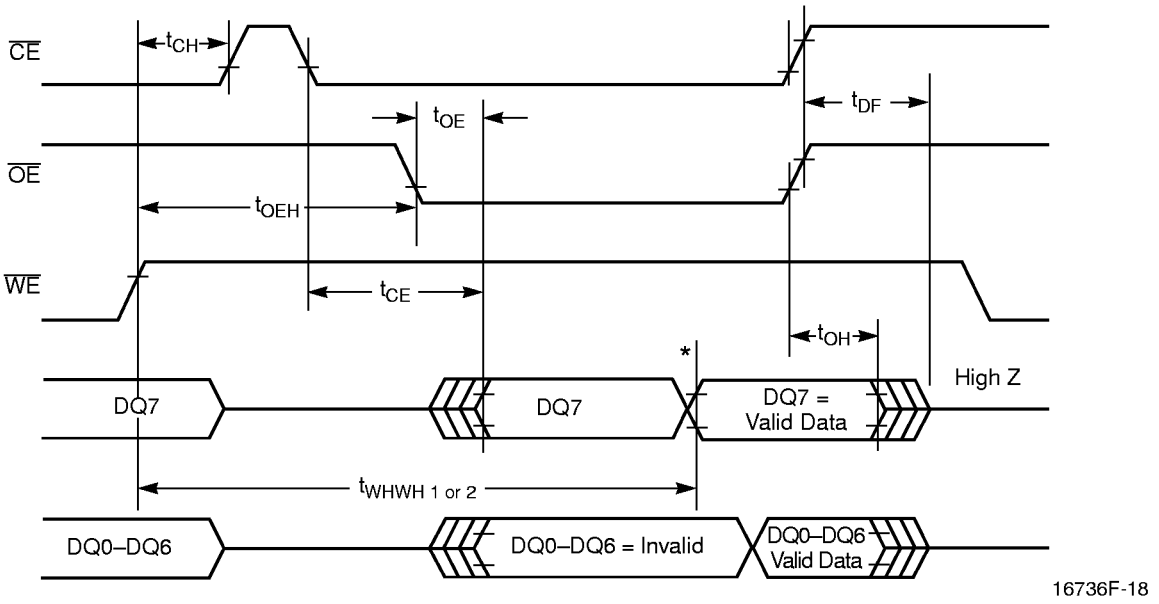


Note:

SA is the sector address for Sector Erase. Addresses = don't care for Chip Erase.

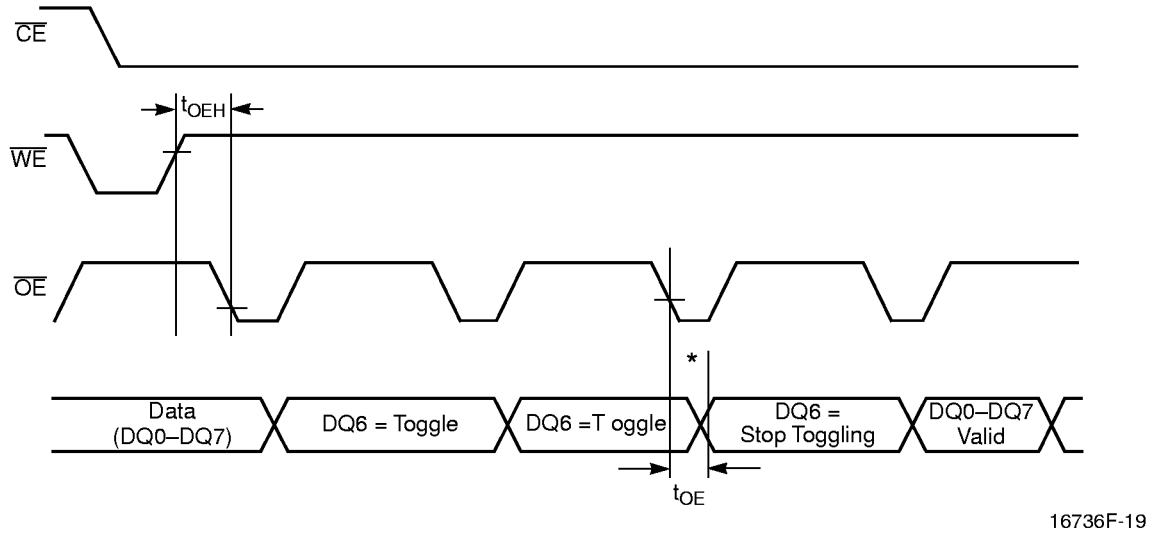
Figure 10. AC Waveforms Chip/Sector Erase Operations

SWITCHING WAVEFORMS



**DQ7=Valid $\overline{Data}$ (The device has completed the Embedded operation).*

Figure 11. AC Waveforms for $\overline{Data}$ Polling During Embedded Algorithm Operations



**DQ6 stops toggling (The device has completed the Embedded operation).*

Figure 12. AC Waveforms for Toggle Bit During Embedded Algorithm Operations

AC CHARACTERISTICS

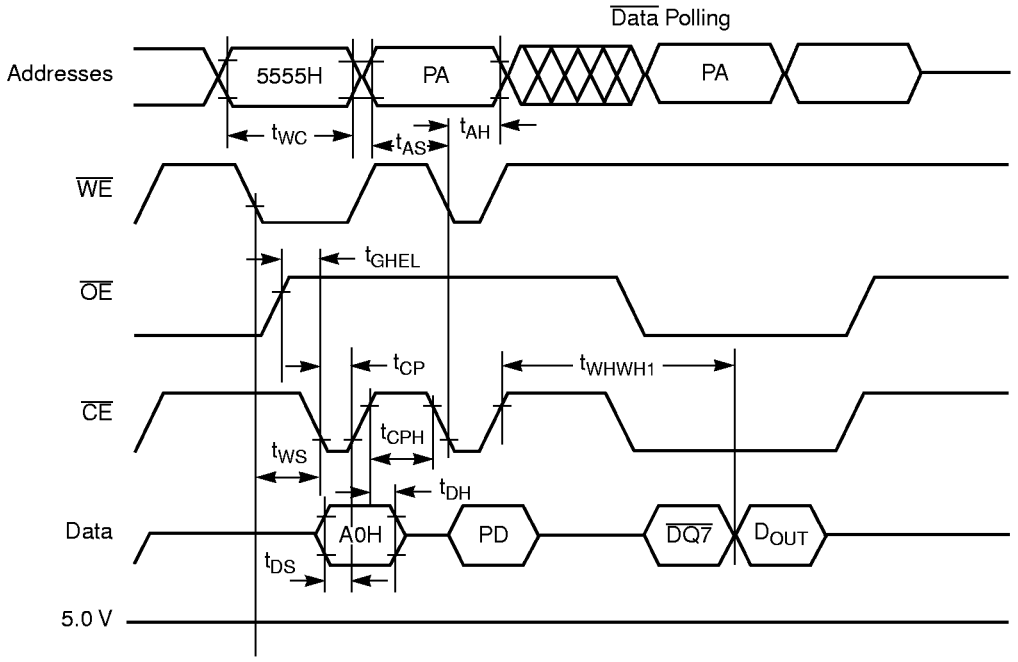
Write/Erase/Program Operations

Alternate $\overline{CE}$ Controlled Writes

Parameter Symbols		Description			-45	-55	-70	-90	-120	Unit
JEDEC	Standard									
t_{AVAV}	t_{WC}	Write Cycle Time (Note 2)		Min	45	55	70	90	120	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0	0	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	35	45	45	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	20	20	30	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time (Note 2)		Min	0	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time	Read (Note 2)	Min	0	0	0	0	0	ns
			Toggle Bit and $\overline{Data}$ Polling (Note 2)	Min	10	10	10	10	10	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write		Min	0	0	0	0	0	ns
t_{WLEL}	t_{WS}	$\overline{CE}$ Setup Time		Min	0	0	0	0	0	ns
t_{EHWH}	t_{WH}	$\overline{CE}$ Hold Time		Min	0	0	0	0	0	ns
t_{ELEH}	t_{CP}	Write Pulse Width		Min	25	30	35	45	50	ns
t_{EHEL}	t_{CPH}	Write Pulse Width High		Min	20	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation		Typ	14	14	14	14	14	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)		Typ	1.3	1.3	1.3	1.3	1.3	sec

Notes:

1. *This does not include the preprogramming time.*
2. *Not 100% tested.*



1. *PA is address of the memory location to be programmed.*
2. *PD is data to be programmed at byte address.*
3. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
4. *D_{OUT} is the output of the data written to the device.*
5. *Figure indicates last two bus cycles of four bus cycle sequence.*

Figure 13. Alternate $\overline{CE}$ Controlled Program Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits		Unit	Comments
	Typ (Note 1)	Max		
Chip/Sector Erase Time	1	15 (Note 1)	sec	Excludes 00H programming prior to erasure
Byte Programming Time	14	1000 (Note 3)	µs	Excludes system-level overhead (Note 4)
Chip Programming Time	1.8	12.5 (Notes 3, 5)	sec	Excludes system-level overhead (Note 4)

Notes:

1. *25°C, 5.0 V V_{CC}, 100,000 cycles.*
2. *Although Embedded Algorithms allow for longer chip program and erase time, the actual time will be considerably less since bytes program or erase significantly faster than the worst case byte.*
3. *Under worst case condition of 90°C, 4.5 V V_{CC}, 100,000 cycles.*
4. *System-level overhead is defined as the time required to execute the four bus cycle command necessary to program each byte. In the preprogramming step of the Embedded Erase algorithm, all bytes are programmed to 00H before erasure.*
5. *The Embedded Algorithms allow for 48 ms byte program time. DQ5 = "1" only after a byte takes the theoretical maximum time to program. A minimal number of bytes may require significantly more programming pulses than the typical byte. The majority of the bytes will program within one or two pulses. This is demonstrated by the Typical and Maximum Programming Times listed above.*
6. *100,000 program/erase cycles is guaranteed; 1,000,000 program/erase cycles is typical.*

LATCHUP CHARACTERISTICS

	Min	Max
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A9)	–1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
Current	–100 mA	+100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

PLCC PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	Control Pin Capacitance	V_{PP} = 0	8	12	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

PDIP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	Control Pin Capacitance	V_{PP} = 0	8	12	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

REVISION SUMMARY

Product Selector Guide:

There are now two V_{CC} supply operating ranges available for the 55 ns speed option. The PDIP package is only available in the ±5% V_{CC} operating range. The other packages are available in the ±10% operating range.

Ordering Information:

The 45 ns speed grade is now also available in PC configuration (PDIP package, commercial temperature.)

Operating Ranges:

V_{CC} Supply Voltages: Changed to reflect the available speed options.

AC Characteristics:

Write/Erase/Program Operations: Corrected to indicate t_{VLHT}, t_{OESP}, t_{WHWH1}, and t_{WHWH2} are typical values, not minimum values. Changed value for t_{WHWH2}.

AC Characteristics:

Write/Erase/Program Operations, Alternate $\overline{CE}$ Controlled Writes: Corrected to indicate t_{WHWH1} and t_{WHWH2} are typical values, not minimum values. Changed value for t_{WHWH2}.

Erase and Programming Performance:

Combined chip and sector erase specifications; changed typical and maximum values. Added Note 6.