W83194BR-B

W83194BG-B

Winbond Clock Generator For INTEL P4 845 Series Chipset

Date: 10/02/2006 Revision: 3.1

W83194BR-B Datasheet Revision History

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
1	n.a.			n.a.	All of the versions before 0.50 are for internal use.
2	n.a.	4/1/02	1.0	1.0	Change version and version on web site to 1.0
3	11	10/1/02	1.1	1.0	Modify ratio table of CPU, 3V66, and PCI clock selection.
4	All	2/25/03	2.0	1.0	Update new form
5		3/18/03	3.0		Change to B version, adding new register, VCN
6		10/02/06	3.1		Add Lead free part
7					
8					
9					
10					

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winbond

CLOCK GEN. FOR INTEL P4 845 SERIES CHIPSET

1. GENERAL DESCRIPTION

The W83194BR-B is a Clock Synthesizer for Intel P4 845 series chipset. W83194BR-B provides all clocks required for high-speed microprocessor and provides step-less frequency programming and 32 different frequencies of CPU, PCI, and 3V66 clocks setting. All clocks are externally selectable with smooth transitions.

The W83194BR-B provides I^2C serial bus interface to program the registers to enable or disable each clock outputs and provides +/-0.25% center type spread spectrum or programmable S.S.T. scale to reduce EMI.

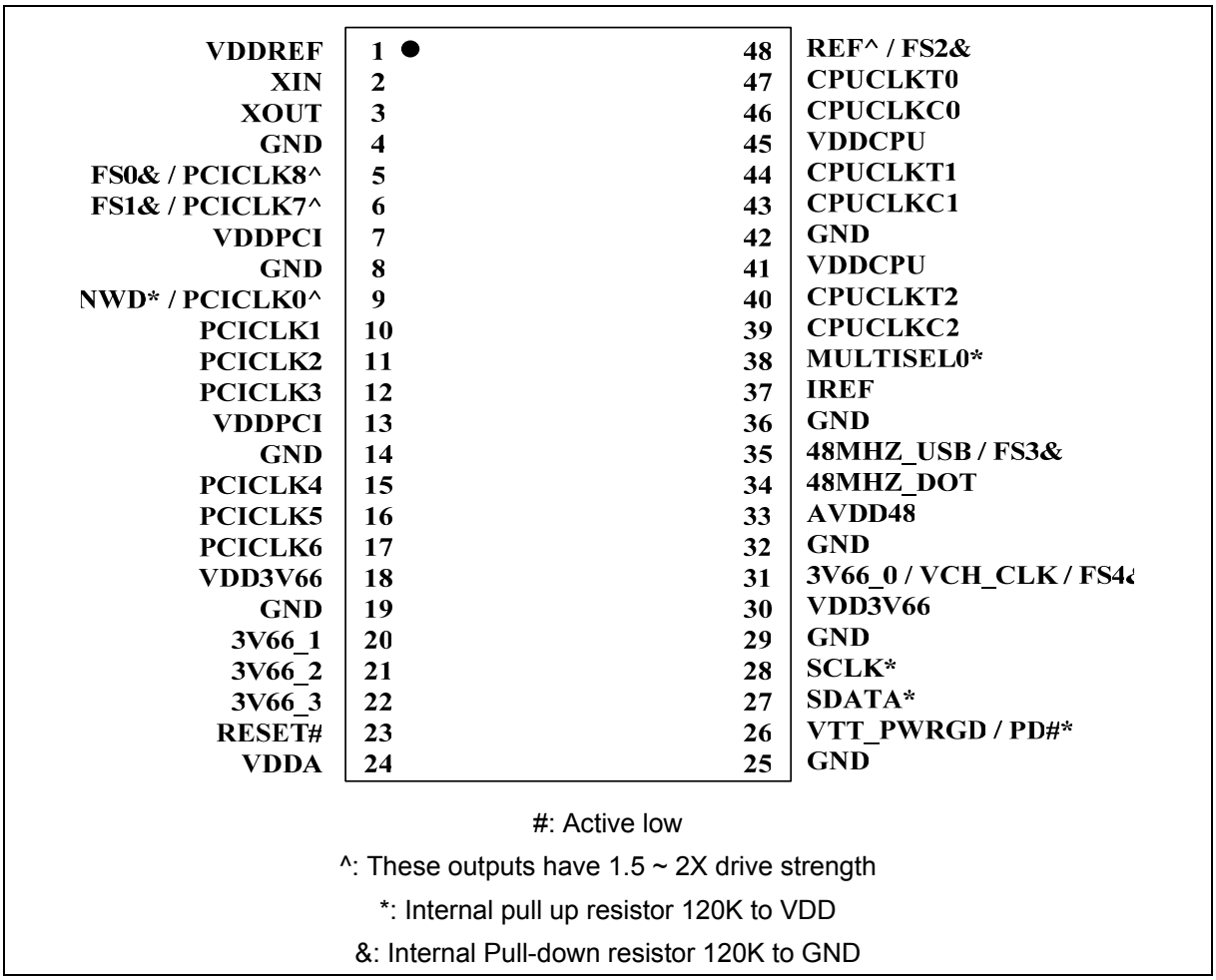
The W83194BR-B also has watch dog timer and reset output pin to support auto-reset when systems hanging caused by improper frequency setting.

The W83194BR-B accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. High drive PCI CLOCK outputs typically provide greater than 1 V /ns slew rate into 30 pF loads. CPU CLOCK outputs typically provide better than 1 V /ns slew rate into 20 pF loads as maintaining 50± 5% duty cycle. The fixed frequency outputs as REF and 48 MHz provide better than 0.5V /ns slew rate.

2. PRODUCT FEATURES

- 3 pairs of CPU clock outputs
- 4 3V66 clock outputs
- 9 PCI synchronous clocks
- 2 48MHz clock outputs for USB and DOT
- AGP/PCI clock out supports fix mode with 4 step option
- Slew rate control
- 3V66 leads PCICLK from 1.5ns to 3.5ns
- Smooth frequency switch with selections from 100 to 200MHz
- Step-less frequency programming
- I^2C 2-Wire serial interface and I^2C read back
- +/- 0.25% center type spread spectrum
- Programmable S.S.T. scale to reduce EMI
- Programmable registers to enable/stop each output and select modes
- Watch Dog Timer and RESET# output pins
- 48-pin SSOP package

3. PIN CONFIGURATION



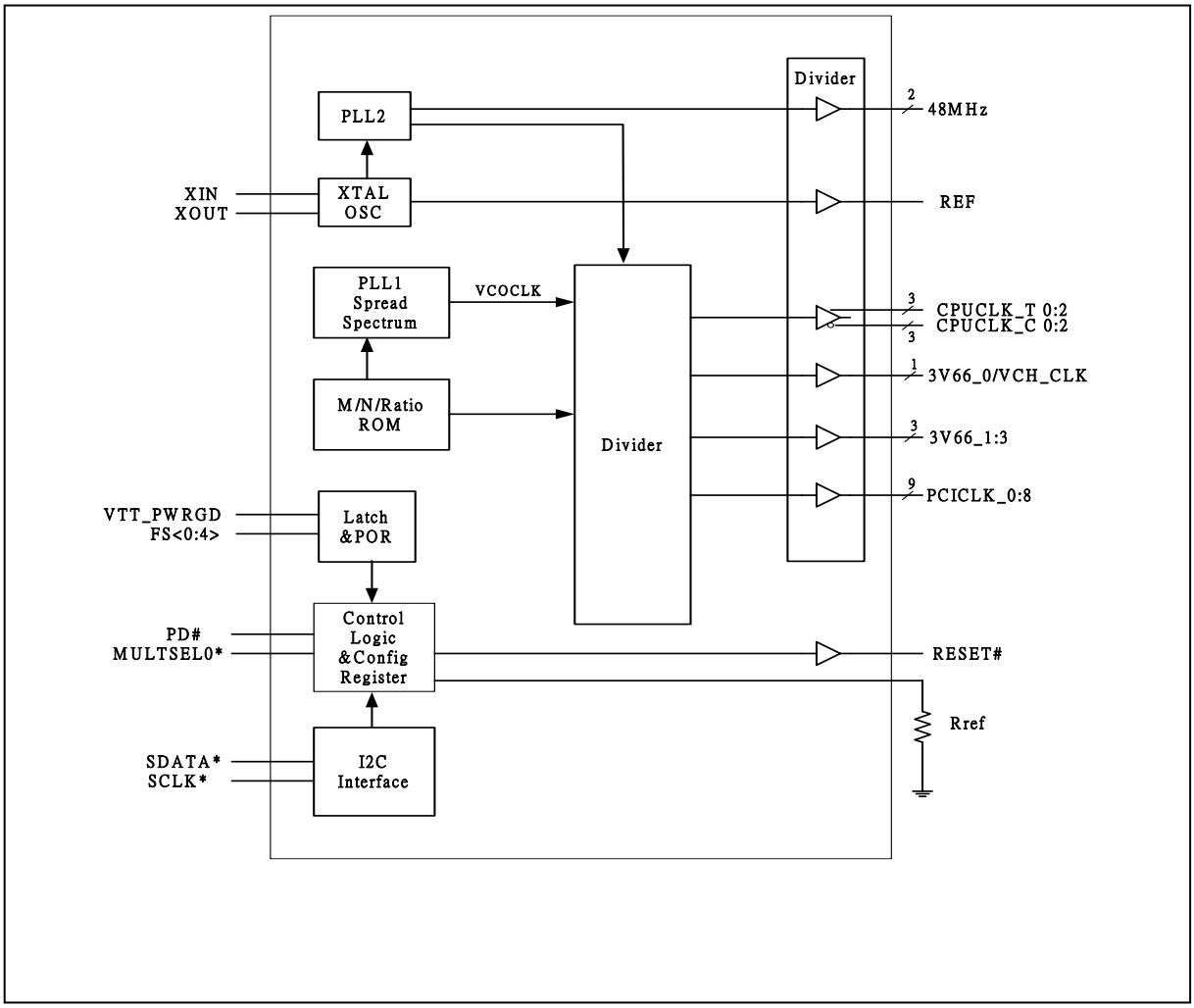
#: Active low

^: These outputs have 1.5 ~ 2X drive strength

*: Internal pull up resistor 120K to VDD

&: Internal Pull-down resistor 120K to GND

4. BLOCK DIAGRAM



5. PIN DESCRIPTION

BUFFER TYPE SYMBOL	DESCRIPTION
IN	Input
IN_{td120k}	Input pin and internal 120K pull down
OUT	Output
OD	Open Drain
I/O	Bi-directional Pin
I/OD	Bi-directional Pin, Open Drain
#	Active Low
*	Internal 120kΩ pull-up
&	Internal 120kΩ pull-down
^	1.5X~2X strength

5.1 Crystal I/O

PIN	PIN NAME	TYPE	DESCRIPTION
3	XIN	IN	Crystal input with internal loading capacitors (18pF) and feedback resistors.
4	XOUT	OUT	Crystal output at 14.318MHz nominally with internal loading capacitors (18pF).

5.2 CPU, 3V66, PCI Clock Outputs

<table>
<tr><th>PIN</th><th>PIN NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>47, 46, 44, 43, 40, 39</td><td>CPUCLKT [0:2]
CPUCLKC [0:2]</td><td>OUT</td><td>Differential clock outputs for host frequencies of CPU and chipset</td></tr>
<tr><td>38</td><td>MULTISEL0*</td><td>IN</td><td>Power on trapping for different current reference. The reference current is referred for Pin 37 (IREF). This pin is latched during VTT_PWRGD. This pin is internal pull up 120K.</td></tr>
<tr><td>37</td><td>IREF</td><td>IN</td><td>Deciding the reference current for the CPUCLK pairs.The pin was connected to the precision resistor tied to ground to decide the appropriate current. There are two mode to select different current via power on trapping the Pin 38 (MULTISEL0). The table is show as follows.
<table>
<tr><th>MULTSEL0</th><th>BOARD TARGET TRACE</th><th>REFERENCE R, IREF</th><th>OUTPUT CURRENT</th><th>IOH @ Z</th></tr>
<tr><td>0</td><td>50 Ohms</td><td>R=221
Iref=5.0mA</td><td>Ioh=4*Iref</td><td>1.0V @ 50</td></tr>
<tr><td>1</td><td>50 Ohms</td><td>R=475
Iref=232mA</td><td>Ioh=6*Iref</td><td>0.7V @ 50</td></tr>
</table></td></tr>
<tr><td>23</td><td>RESET#</td><td>OD</td><td>System reset signal when the watch dog is time out. This pin will generate 250mS when the watchdog timer is timeout.</td></tr>
<tr><td rowspan="2">26</td><td>VTT_PWRGD</td><td>IN</td><td>Power good input signal comes from ACPI with high active. This 3.3V input is level sensitive strobe used to determine FS [4:0] and MULTISEL0 input are valid and is ready to sample. This pin is high active.</td></tr>
<tr><td>PD#*</td><td>IN</td><td>Power Down Function. This is internal 120K pull up. This is multi-function pin. When the VTT_PWRGD signal is asserted (this is, turns from a logical Low to high), the pin will be switched into the function of power down (PD#).</td></tr>
<tr><td rowspan="3">31</td><td>3V66_0</td><td>OUT</td><td rowspan="2">66MHz or 48MHz outputs selected by I2C register.</td></tr>
<tr><td>VCH_CLK</td><td>OUT</td></tr>
<tr><td>FS4&</td><td>IN_{td120k}</td><td>Latched input for FS4 at initial power up for H/W selecting the output frequency of CPU 3V66 and PCI clocks. This is internal 120K pull down.</td></tr>
<tr><td rowspan="2">5</td><td>PCICLK8^</td><td>OUT</td><td>PCI clock output. This pin is with x1.5 ~ x2 driving strength.</td></tr>
<tr><td>FS0&</td><td>IN_{td120k}</td><td>Latched input for FS0 at initial power up for H/W selecting the output frequency of CPU, 3V66 and PCI clocks. This is internal 120K pull down.</td></tr>
</table>

CPU, 3V66, PCI Clock Outputs, continued.

PIN	PIN NAME	TYPE	DESCRIPTION
6	PCICLK7^	OUT	PCI clock output. This pin is with x1.5 ~ x2 driving strength.
	FS1&	IN_{td120k}	Latched input for FS1 at initial power up for H/W selecting the output frequency of CPU, 3V66 and PCI clocks. This is internal 120K pull down.
9	PCICLK0^	OUT	PCI clock outputs. This pin is with x1.5 ~ x2 driving strength.
	ENWD*	IN	Latched input for ENWD at initial power up for H/W enable the watch dog timer. This is internal 120K pull up.
10, 11, 12, 15, 16, 17	PCICLK [1:6]	OUT	PCI clock outputs.
20, 21, 22	3V66_1, 3V66_2, 3V66_3	OUT	3.3V output clocks for the chipset.

5.3 I2C Control Interface

PIN	PIN NAME	TYPE	DESCRIPTION
27	SDATA*	I/OD	Serial data of I^2C 2-wire control interface with internal pull-up resistor.
28	SCLK*	IN	Serial clock of I^2C 2-wire control interface with internal pull-up resistor.

5.4 Fixed Frequency Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
48	REF^	OUT	14.318NHz output. This pin is with x1.5 ~ x2 driving strength.
	FS2&	IN_{td120k}	Latched input for FS2 at initial power up for H/W selecting the output frequency of CPU, 3V66 and PCI clocks. This is internal 120K pull down.
34	48MHz_DOT	OUT	48MHz clock output for DOT.
35	48MHz_USB	OUT	48MHz clock output for USB.
	FS3&	IN_{td120k}	Latched input for FS3 at initial power up for H/W selecting the output frequency. This is internal 120K pull down.

5.5 Power Pins

PIN	PIN NAME	TYPE	DESCRIPTION
1,	VDDREF	PWR	3.3V power supply for REF.
7, 13	VDDPCI	PWR	3.3V power supply for PCI.
18, 30	VDD3V66	PWR	3.3V power supply for 3V66.
41, 45	VDDCPU	PWR	3.3V power supply for CPU.
24	VDDA	PWR	3.3V power supply for analog core.
33	AVDD48	PWR	Analog power 3.3V for 48MHz
4, 8, 14, 19, 25, 29, 32, 36, 42	GND	PWR	Ground pin for 3.3 V

6. FREQUENCY SELECTION BY HARDWARE OR SOFTWARE

This frequency table is used at power on latched FS [4:0] value or software programming at SSEL [4:0] (Register 0 bit 6 ~ 2).

FS4	FS3	FS2	FS1	FS0	CPU (MHZ)	3V66(MHZ)	PCI (MHZ)	SPREAD %
0	0	0	0	0	100.8	67.2	33.6	+/-0.25%
0	0	0	0	1	100.0	66.6	33.3	+/-0.25%
0	0	0	1	0	101.1	67.4	33.7	+/-0.25%
0	0	0	1	1	104.9	69.9	35.0	+/-0.25%
0	0	1	0	0	107.1	71.4	35.7	+/-0.25%
0	0	1	0	1	109.0	72.7	36.3	+/-0.25%
0	0	1	1	0	100.0	66.6	33.3	+/-0.25%
0	0	1	1	1	114.0	76.0	38.0	+/-0.25%
0	1	0	0	0	117.0	78.0	39.0	+/-0.25%
0	1	0	0	1	120.1	80.0	40.0	+/-0.25%
0	1	0	1	0	126.9	84.6	42.3	+/-0.25%
0	1	0	1	1	130.0	86.6	43.3	+/-0.25%
0	1	1	0	0	133.3	88.8	44.4	+/-0.25%
0	1	1	0	1	170.2	56.7	28.4	+/-0.25%
0	1	1	1	0	133.3	66.6	33.3	+/-0.25%
0	1	1	1	1	190.0	63.3	31.7	+/-0.25%
1	0	0	0	0	134.7	67.4	33.7	+/-0.25%
1	0	0	0	1	133.3	66.6	33.3	+/-0.25%
1	0	0	1	0	120.1	60.0	30.0	+/-0.25%
1	0	0	1	1	124.8	62.4	31.2	+/-0.25%
1	0	1	0	0	134.7	67.4	33.7	+/-0.25%
1	0	1	0	1	136.9	68.5	34.2	+/-0.25%
1	0	1	1	0	199.9	66.6	33.3	+/-0.25%
1	0	1	1	1	141.0	70.5	35.2	+/-0.25%
1	1	0	0	0	143.2	71.6	35.8	+/-0.25%
1	1	0	0	1	145.0	72.5	36.3	+/-0.25%
1	1	0	1	0	150.2	75.1	37.5	+/-0.25%
1	1	0	1	1	154.9	77.5	38.7	+/-0.25%
1	1	1	0	0	160.1	80.0	40.0	+/-0.25%
1	1	1	0	1	170.0	85.0	42.5	+/-0.25%
1	1	1	1	0	166.9	66.7	33.4	+/-0.25%
1	1	1	1	1	200.1	100.0	50.0	+/-0.25%

7. I²C CONTROL AND STATUS REGISTERS

(The register No. Is increased by 1 if use byte data read/write protocol)

7.1 Register 0: Frequency Select Register (Default = 0)

BIT	NAME	PWD	DESCRIPTION
7	EN_SPSP	0	Enable Spread Spectrum in the frequency table. 0 = Normal 1 = Spread Spectrum enabled
6	SSEL [4]	0	Frequency selection by software via I²C.
5	SSEL [3]	0	
4	SSEL [2]	0	
3	SSEL [1]	0	
2	SSEL [0]	0	
1	EN_SSEL	0	Enable software program FS [4:0]. 0 = Select frequency by hardware. 1= Select frequency by software I²C - Bit 6 ~ 2.
0	EN_SAFE_FREQ	0	Enable reload safe frequency when the watchdog is timeout. 0 = reload the FS [4:0] latched pins when watchdog time out. 1 = reload the safe frequency bit defined at Register 5 bit 4~0.

7.2 Register 1: CPU Clock Register (1 = Enable, 0 = Stopped)

BIT	PIN NO.	PWD	DESCRIPTION
7	47, 46	1	CPUCLKT2 / C2
6	44, 43	1	CPUCLKT1 / C1
5	40, 39	1	CPUCLKT0 / C0
4	-	X	FS [4] Read back.
3	-	X	FS [3] Read back
2	-	X	FS [2] Read back
1	-	X	FS [1] Read back
0	-	X	FS [0] Read back

7.3 Register 2: PCI Clock Register (1 = Enable, 0 = Stopped)

BIT	PIN NO.	PWD	DESCRIPTION
7	-	X	MULTISEL0 trapping pin data read back
6	17	1	PCICLK 6
5	16	1	PCICLK 5
4	15	1	PCICLK 4
3	12	1	PCICLK 3
2	11	1	PCICLK 2
1	10	1	PCICLK 1
0	9	1	PCICLK 0

7.4 Register 3: PCI, 48MHz Clock Register (1 = Enable, 0 = Stopped)

BIT	PIN NO.	PWD	DESCRIPTION
7	34	1	48MHZ_DOT
6	35	1	48MHZ_USB
5	48	1	REF
4	-	0	Reserved
3	EN_VCH_CLK	0	1 = VCH_CLK 48MHz clock output. 0 = 3V66_0 66MHz clock output (default).
2	-	1	Reserved
1	6	1	PCICLK7
0	5	1	PCICLK8

7.5 Register 4: 3V66 Control Register (1 = Enable, 0 = Stopped)

BIT	PIN NO.	PWD	DESCRIPTION
7	-	1	Reserved
6	-	1	Reserved
5	-	1	Reserved
4	-	1	Reserved
3	22	1	3V66_3
2	21	1	3V66_2
1	20	1	3V66_1
0	31	1	3V66_0/VCH_CLK

7.6 Register 5: Watchdog Control Register

BIT	NAME	PWD	DESCRIPTION
7	Reserved	0	Reserved
6	EN_WD	X	Enable Watchdog Timer if set to 1. Set to 0, disable watchdog timer. This bit is trapping pin during VTT_PWRGD#. Read this bit will return a counting state. If timers continue down count, this bit will return 1. Otherwise, this bit will return 0.
5	WD_TIMEOUT	0	Watchdog Timeout Status. If the watchdog is started and timer down counts to zero, this bit will be set to 1. Clear this bit to logic 0, If set to 1, when the watchdog is restart in the next time. This bit is Read Only.
4	SAF_FREQ [4]	0	Watchdog safe frequency bits. These bits will be reloaded into FS [4:0], if the watchdog is timeout and enable reload safe frequency bits.
3	SAF_FREQ [3]	0	
2	SAF_FREQ [2]	0	
1	SAF_FREQ [1]	0	
0	SAF_FREQ [0]	0	

7.7 Register 6: Watchdog Timer Register

BIT	NAME	PWD	DESCRIPTION
7	WD_TIME [7]	0	Watchdog timeout time. The bit resolution is 250mS. The default time is 8*250mS = 2.0 seconds. If the watchdog timer is start, this register will be down count. Read this register will return a down count value.
6	WD_TIME [6]	0	
5	WD_TIME [5]	0	
4	WD_TIME [4]	0	
3	WD_TIME [3]	1	
2	WD_TIME [2]	0	
1	WD_TIME [1]	0	
0	WD_TIME [0]	0	

7.8 Register 7: M/N Program Register

BIT	NAME	PWD	DESCRIPTION
7	N_DIV [8]	X	Programmable N divisor value. Bit 7 ~0 are defined in the Register 8.
6	TEST1	X	Test bit 1. Winbond test bit, do not change them.
5	TEST0	X	Test bit 0. Winbond test bit, do not change them.
4	M_DIV [4]	X	Programmable M divisor value.
3	M_DIV [3]	X	
2	M_DIV [2]	X	
1	M_DIV [1]	X	
0	M_DIV [0]	X	

7.9 Register 8: M/N Program Register

BIT	NAME	PWD	DESCRIPTION
7	N_DIV [7]	X	Programmable N divisor value bit 7 ~0. The bit 8 is defined in Register 7.
6	N_DIV [6]	X	
5	N_DIV [5]	X	
4	N_DIV [4]	X	
3	N_DIV [3]	X	
2	N_DIV [2]	X	
1	N_DIV [1]	X	
0	N_DIV [0]	X	

7.10 Register 9: Spread Spectrum Programming Register

BIT	NAME	PWD	DESCRIPTION
7	SP_UP [3]	0	Spread Spectrum Up Counter bit 3.
6	SP_UP [2]	0	Spread Spectrum Up Counter bit 2.
5	SP_UP [1]	0	Spread Spectrum Up Counter bit 1.
4	SP_UP [0]	1	Spread Spectrum Up Counter bit 0
3	SP_DOWN [3]	1	Spread Spectrum Down Counter bit 3
2	SP_DOWN [2]	1	Spread Spectrum Down Counter bit 2
1	SP_DOWN [1]	1	Spread Spectrum Down Counter bit 1
0	SP_DOWN [0]	1	Spread Spectrum Down Counter bit 0

7.11 Register 10: Divisor and Step-less Enable and Skew Control Register

BIT	NAME	PWD	DESCRIPTION
7	EN_MN_PROG	0	0: use frequency table 1: use M/N register to program frequency The equation is VCO freq. = 14.318MHz * (N+4)/ M. When the watchdog timer is timeout, this will be clear. In this time, the frequency is set to hardware default latched or safe frequency set by EN_SFAE_FREQ (Register 0 bit 0).
6	Test2	X	Test bit 2. Winbond test bit, do not change them.
5	RATIO_SEL [2]	X	CPU, 3V66, and PCI ratio selection. The ratio is shown as following table.
4	RATIO_SEL [1]	X	
3	RATIO_SEL [0]	X	
2	CPU_3V66_SKEW [2]	1	CPU to 3V66 skew.
1	CPU_3V66_SKEW [1]	0	
0	CPU_3V66_SKEW [0]	0	

Table of CPU, 3V66, and PCI clock ratio selection.

REG11 BIT5	REG11 BIT4	REG11 BIT3	VCO / CPU	VCO / 3V66	VCO / PCI
SEL2	SEL1	SEL0	RATIO	RATIO	RATIO
0	0	0	2	5	10
0	0	1	2	6	12
0	1	0	3	6	12
0	1	1	4	6	12
1	0	0	6	6	12
1	0	1	6	10	20
1	1	0	3	5	10
1	1	1	3	5	10

7.12 Register 11: C Winbond Chip ID Register (Read Only)

BIT	NAME	PWD	DESCRIPTION
7	CHPI_ID [7]	0	Winbond Chip ID. W83194BR-B is 0x32.
6	CHPI_ID [6]	0	Winbond Chip ID.
5	CHPI_ID [5]	1	Winbond Chip ID.
4	CHPI_ID [4]	1	Winbond Chip ID.
3	CHPI_ID [3]	0	Winbond Chip ID.
2	CHPI_ID [2]	0	Winbond Chip ID.
1	CHPI_ID [1]	1	Winbond Chip ID.
0	CHPI_ID [0]	0	Winbond Chip ID.

7.13 Register 12: Winbond Chip ID Register (Read Only)

BIT	NAME	PWD	DESCRIPTION
7	MAS_ID[1]	1	Winbond Master-Chip ID.
6	MAS_ID[0]	0	Winbond Master-Chip ID.
5	SUB_ID[1]	0	Winbond Sub-Chip ID.
4	SUB_ID[0]	1	Winbond Sub-Chip ID.
3	MAS_VER_ID[1]	0	Winbond Master's Version ID.
2	MAS_VER_ID[1]	1	Winbond Master's Version ID.
1	SUB_VER_ID[1]	0	Winbond Sub's Version ID.
0	SUB_VER_ID[1]	1	Winbond Sub's Version ID.

7.14 Register 13: SEL24_48 and FIX_3V66_PCI Control

<table>
<tr><th>BIT</th><th>NAME</th><th>PWD</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>SEL24_48</td><td>0</td><td>Pin 34, 48MHz_DOT output frequency select bit
SEL24_48=0, 48MHz_DOT=48MHz(Default)
SEL24_48=1, 48MHz_DOT=24MHz</td></tr>
<tr><td>6</td><td>Iref_test0</td><td>0</td><td>Control CPU_I/O Buffer Bias Current</td></tr>
<tr><td>5</td><td>FIX_3V66_PCI</td><td>0</td><td>0: normal mode, 1: fix mode</td></tr>
<tr><td>4</td><td>SEL [1]</td><td>0</td><td rowspan="2">3V66 & PCI FIX frequency (PCI=3V66/2)
SEL [1:0] for 3V66, PCI, When bit 5 set 1 these bit had function
<table>
<tr><th>SEL [0]</th><th>SEL [1]</th><th>3V66</th><th>PCI</th></tr>
<tr><td>0</td><td>0</td><td>72MHz</td><td>36MHz</td></tr>
<tr><td>0</td><td>1</td><td>64MHz</td><td>32MHz</td></tr>
<tr><td>1</td><td>0</td><td>76.8MHz</td><td>38.4MHz</td></tr>
<tr><td>1</td><td>1</td><td>67.2MHz</td><td>33.6MHz</td></tr>
</table></td></tr>
<tr><td>3</td><td>SEL [0]</td><td>0</td></tr>
<tr><td>2</td><td>CPU_PCI_SKEW [2]</td><td>1</td><td rowspan="3">CPU to PCI skew</td></tr>
<tr><td>1</td><td>CPU_PCI_SKEW [1]</td><td>0</td></tr>
<tr><td>0</td><td>CPU_PCI_SKEW [0]</td><td>0</td></tr>
</table>

7.15 Register 14: Control the period of spread spectrum

BIT	NAME	PWD	DESCRIPTION
7	-	0	Reserved
6	-	0	Reserved
5	SPCNT [5]	1	Program the period of spread spectrum.
4	SPCNT [4]	0	
3	SPCNT [3]	0	
2	SPCNT [2]	1	
1	SPCNT [1]	1	
0	SPCNT [0]	1	

Note: The Register 15:17 slew rate control select bit fit value Please fellow below table.

The S1_N is S1 complementary and S2_N is S2 complementary, please fit complementary value.

S1:S2	S1_N: S2_N	SLEW RATE STATUS
10/01	01/10	Normal
11	00	Strong
00	11	Weak

7.16 Register 15: Slew Rate Control

BIT	NAME	PWD	DESCRIPTION
7	REF_S1	0	Pin 48 REF output slew rate control bit. This slew rate status default is Weak.
6	REF_S1_N	1	
5	REF_S2	0	
4	REF_S2_N	1	
3	3V66_S1	1	Pin 20,21,22, 3V66 [1:3] output slew rate control bit. This slew rate status default is Normal.
2	3V66_S1_N	0	
1	3V66_S2	0	
0	3V66_S2_N	1	

7.17 Register 16: Slew Rate Control

BIT	NAME	PWD	DESCRIPTION
7	PCIF_S1	1	Pin 5,6,9, PCICLK [0,7,8] output slew rate control bit This slew rate status default is Strong.
6	PCIF_S1_N	0	
5	PCIF_S2	1	
4	PCIF_S2_N	0	
3	PCI_S1	1	Pin 10,11,12,15,16,17 PCICLK [1:6] output slew rate control bit This slew rate status default is Normal.
2	PCI_S1_N	0	
1	PCI_S2	0	
0	PCI_S2_N	1	

7.18 Register 17: Slew Rate Control

BIT	NAME	PWD	DESCRIPTION
7	3V66_S1	1	Pin 31 3V66_0/VCH output slew rate control bit. This slew rate status default is Normal.
6	3V66_S1_N	0	
5	3V66_S2	0	
4	3V66_S2_N	1	
3	U48M_S1	1	Pin 34,35 48MHz_USB, 48MHz_DOT output slew rate control bit. This slew rate status default is Normal.
2	U48M_S1_N	0	
1	U48M_S2	0	
0	U48M_S2_N	1	

7.19 Register 81: Winbond Test Register I

BIT	NAME	PWD	DESCRIPTION
7:0	TEST_REG1	00h	Winbond Test Register. User don't write it, otherwise this chip will get an unexpected result.

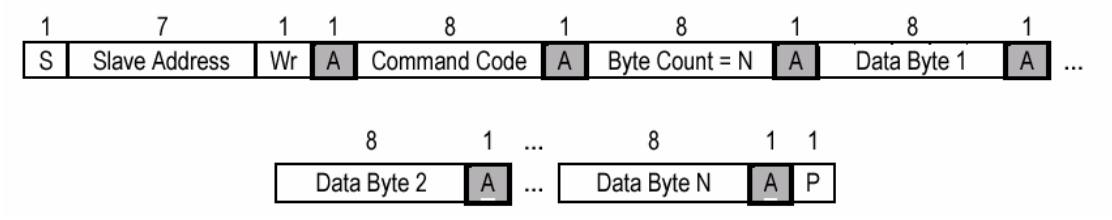
7.20 Register 82: Winbond Test Register II

BIT	NAME	PWD	DESCRIPTION
7:0	TEST_REG2	04h	Winbond Test Register. User don't write it, otherwise this chip will get an unexpected result.

8. ACCESS INTERFACE

The W83194BR-B provides I^2C Serial Bus for microprocessor to read/write internal registers. In the W83194BR-B is provided Block Read/Block Write and Byte-Data Read/Write protocol. The I^2C address is defined at 0xD2.

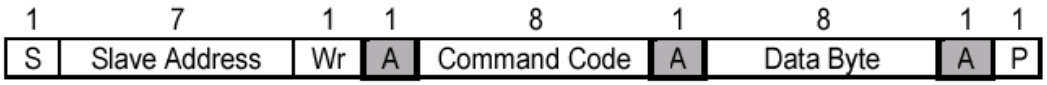
8.1 Block Write protocol



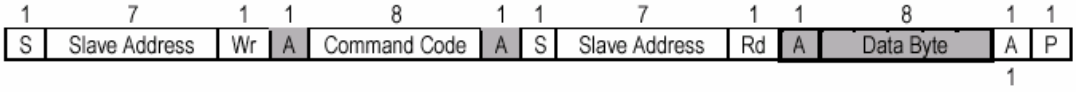
8.2 Block Read protocol

In block mode, the command code must filled 00H

8.3 Byte Write protocol



8.4 Byte Read protocol



9. SPECIFICATIONS

9.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Subjection to maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or VDD).

PARAMETER	RATING
Absolute 3.3V Core Supply Voltage	-0.5V to +4.6V
Absolute 3.3V I/O Supple Voltage	- 0.5 V to + 4.6 V
Operating 3.3V Core Supply Voltage	3.135V to 3.465V
Operating 3.3V I/O Supple Voltage	3.135V to 3.465V
Storage Temperature	- 65°C to + 150°C
Ambient Temperature	- 55°C to + 125°C
Operating Temperature	0°C to + 70°C
Input ESD protection (Human body model)	2000V

9.2 General Operating Characteristics

VDDREF =VDDA=VDDCPU=VDD3V66=VDDPCI=AVDD48= 3.3V ± 5 %, TA = 0℃ to +70℃, CI=10pF

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}		0.8	V_{dc}	
Input High Voltage	V_{IH}	2.0		V_{dc}	
Output Low Voltage	V_{OL}		0.4	V_{dc}	All outputs using 3.3V power
Output High Voltage	V_{OH}	2.4		V_{dc}	All outputs using 3.3V power
Dynamic Supply Current	I_{dd}		350	mA	CPU = 100 to 200 MHz PCI = 33.3 Mhz with load
Input pin capacitance	Cin		5	pF	
Output pin capacitance	Cout		6	pF	
Input pin inductance	Lin		7	nH	

9.3 Skew Group timing clock

VDDREF =VDDA=VDDCPU=VDD3V66=VDDPCI=AVDD48= 3.3V ± 5 %, TA = 0℃ to +70℃, CI=10pF					
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**	**TEST CONDITIONS**
CPU (early) to PCI Skew	1	2.6	4	ns	CPU Crossing point to PCI at 1.5V
CPU to CPU Skew			150	ps	Crossing point
AGP to AGP Skew			175	ps	Measured at 1.5V
PCI to PCI Skew			500	ps	Measured at 1.5V
48Mhz to 48Mhz Skew			1000	ps	Measured at 1.5V
REF to REF Skew			500	ps	Measured at 1.5V

9.4 CPU 0.7V Electrical Characteristics

*VDDA=VDDCPU= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load Rs=33, Rp=49.9 CI=10pF, Vol=0.14V, Voh=0.56V, Vr=475, IREF=2.32mA, Ioh=6*IREF*				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	175	700	ps	100 to 200 Mhz
Fall Time	175	700	ps	100 to 200Mhz
Absolute crossing point Voltages	250	550	mV	100 to 200Mhz
Cycle to Cycle jitter		125	ps	100 to 200Mhz
Duty Cycle	45	55	%	100 to 200Mhz

9.5 CPU 1.0V Electrical Characteristics

*VDDA=VDDC= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load Rs=33, Rp=49.9 CI=10pF, Vol=0.2V, Voh=0.8V, Vr=221, IREF=5.0mA, Ioh=4*IREF*				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	300	600	ps	100 to 200 Mhz
Fall Time	300	600	ps	100 to 200Mhz
Absolute crossing point Voltages	510	760	mV	100 to 200Mhz
Cycle to Cycle jitter		200	ps	100 to 200Mhz
Duty Cycle	45	55	%	100 to 200Mhz

9.6 AGP Electrical Characteristics

VDDAGP= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	500	1600	ps	
Fall Time	500	1600	ps	
Cycle to Cycle jitter		250	ps	
Duty Cycle	45	55	%	
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

9.7 PCI Electrical Characteristics

VDDPCI= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	500	2000	ps	
Fall Time	500	2000	ps	
Cycle to Cycle jitter		500	ps	
Duty Cycle	45	55	%	
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

9.8 24M, 48M Electrical Characteristics

VDD48= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	1000	4000	ps	
Fall Time	1000	4000	ps	
Long term jitter		500	ps	
Duty Cycle	45	55	%	
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

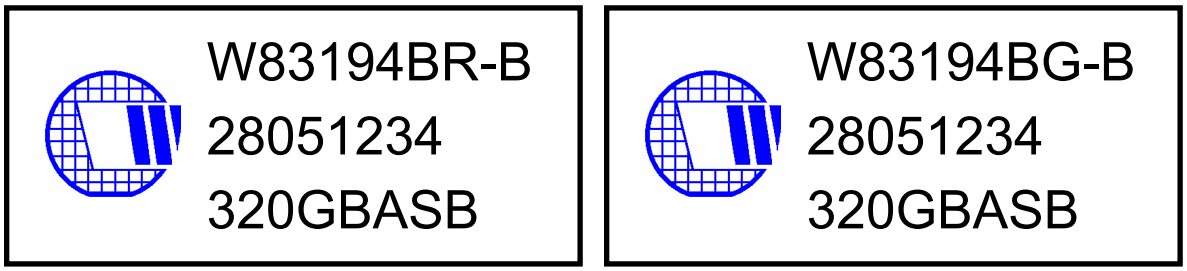
9.9 REF Electrical Characteristics

VDD48= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	1000	4000	ps	
Fall Time	1000	4000	ps	
Cycle to Cycle jitter		1000	ps	
Duty Cycle	45	55	%	
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

10. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83194BR-B	48 PIN SSOP	Commercial, 0°C to +70°C
W83194BG-B	48 PIN SSOP(Lead free part)	Commercial, 0°C to +70°C

11. HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: Normal:W83194BR-B, Lead free: W83194BG-B

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 942 G E D SB

320: packages made in '2003, week 20

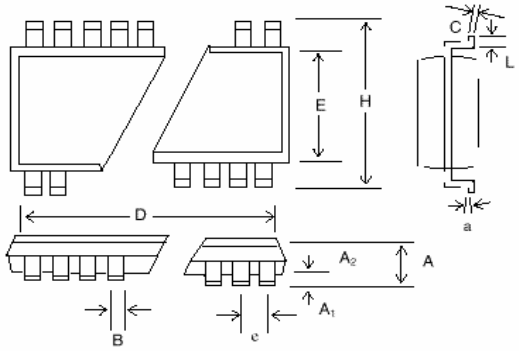
G: assembly house ID; O means OSE, G means GR

E: Internal use code

D: IC revision

SB: Internal use code

12. PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0°	5°	8°	0°	5°	8°

VERSION CHANGE NOTICE 1

1. DESCRIPTION:

1. This version change notice is for W83194BR-B to be changed from A version to B version. It is only for customers who use A version. If you have never used A version, you can skip the following contents.
2. For customers who use A version , the major difference between A version and B version is chip ID and part of frequency table. B version can almost replace A version without any change.

This B revision includes:

1. New Feature supports AGP/PCI clock out in fix mode with 4 step option, and slew rate control with CPU,AGP,PCI,REF,48MHZ.
2. Skew control between CPU with PCI.
3. Pin name of Pin 5,6 (PCICLK_F1, PCICLK_F2) are changed to PCICLK7, PCICLK8.
4. Modify 8 sets FS[0:4] in frequency table to support new CPU frequency table

Difference in Frequency Table

FS4	FS3	FS2	FS1	FS0	VERSION B				VERSION A			
					CPU (MHZ)	3V66 (M HZ)	PCI (MHZ)	SPREAD %	CPU (MHZ)	3V66 (M HZ)	PCI (MHZ)	SPREAD %
0	0	0	0	1	100.0	66.6	33.3	+/-0.25%	100.3	66.87	33.43	-0.50%
0	0	0	1	0	101.1	67.4	33.7	+/-0.25%	103	68.67	34.33	+/-0.25%
0	0	1	1	0	100.0	66.6	33.3	+/-0.25%	111	74	37	+/-0.25%
0	1	1	1	0	133.3	66.6	33.3	+/-0.25%	180	60	30	+/-0.25%
1	0	0	0	0	134.7	67.4	33.7	+/-0.25%	133.9	66.95	33.48	+/-0.25%
1	0	0	0	1	133.3	66.6	33.3	+/-0.25%	133.33	66.67	33.33	-0.50%
1	0	1	1	0	199.9	66.6	33.3	+/-0.25%	139	69.5	34.75	+/-0.25%
1	1	1	1	0	166.9	66.7	33.4	+/-0.25%	66.67	66.67	33.34	+/-0.25%

3. The Version A M/N/Ratio register has default value; Version B M/N/Ratio register is frequency table mirror value.

4. Modify Ratio table

Ratio Table

REG10 BIT5	REG10 BIT4	REG10 BIT3	VERSION B			VERSION A		
SEL2	SEL1	SEL0	VCO/CPU	VCO/ 3V66	VCO/PCI	VCO/CPU	VCO/ 3V66	VCO/PCI
0	0	0	2	5	10	2	4	8
0	0	1	2	6	12	2	5	10
0	1	0	3	6	12	2	6	12
0	1	1	4	6	12	3	6	12
1	0	0	6	6	12	4	4	8
1	0	1	6	10	20	4	6	12
1	1	0	3	5	10	6	6	12
1	1	1	3	5	10	X	X	X

5. Modify Register 12, and add register 13~17.

1.1 Register 12: Winbond Chip ID Register (Read Only)

VERSION B			VERSION A		
BIT	NAME	PWD	BIT	NAME	PWD
7	MAS_ID[1]	**1**	7	SUB_ID [3]	0
6	MAS_ID[0]	**0**	6	SUB_ID [2]	0
5	SUB_ID[1]	**0**	5	SUB_ID [1]	0
4	SUB_ID[0]	**1**	4	SUB_ID [0]	1
3	MAS_VER_ID[1]	**0**	3	VER_ID [3]	0
2	MAS_VER_ID[1]	**1**	2	VER_ID [2]	0
1	SUB_VER_ID[1]	**0**	1	VER_ID [1]	0
0	SUB_VER_ID[1]	**1**	0	VER_ID [0]	1

Note: Register 12 Default value in Version A is 11H Version B is 95H.

1.2 Register 13: SEL24_48 and FIX_3V66_PCI Control

<table>
<tr><th>BIT</th><th>NAME</th><th>PWD</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>SEL24_48</td><td>0</td><td>Pin 34, 48MHz_DOT output frequency select bit
SEL24_48=0, 48MHz_DOT=48MHz(Default)
SEL24_48=1, 48MHz_DOT=24MHz</td></tr>
<tr><td>6</td><td>Iref_test0</td><td>0</td><td>Control CPU_I/O Buffer Bias Current</td></tr>
<tr><td>5</td><td>FIX_3V66_PCI</td><td>0</td><td>0: normal mode, 1: fix mode</td></tr>
<tr><td>4</td><td>SEL [1]</td><td>0</td><td rowspan="2">3V66 & PCI FIX frequency (PCI=3V66/2)
SEL [1:0] for 3V66, PCI, When bit 5 set 1 these bit had function
<table>
<tr><td>SEL [0]</td><td>SEL [1]</td><td>3V66</td><td>PCI</td></tr>
<tr><td>0</td><td>0</td><td>72MHz</td><td>36MHz</td></tr>
<tr><td>0</td><td>1</td><td>64MHz</td><td>32MHz</td></tr>
<tr><td>1</td><td>0</td><td>76.8MHz</td><td>38.4MHz</td></tr>
<tr><td>1</td><td>1</td><td>67.2MHz</td><td>33.6MHz</td></tr>
</table></td></tr>
<tr><td>3</td><td>SEL [0]</td><td>0</td></tr>
<tr><td>2</td><td>CPU_PCI_SKEW [2]</td><td>1</td><td rowspan="3">CPU to PCI skew</td></tr>
<tr><td>1</td><td>CPU_PCI_SKEW [1]</td><td>0</td></tr>
<tr><td>0</td><td>CPU_PCI_SKEW [0]</td><td>0</td></tr>
</table>

1.3 Register 14: Control the period of spread spectrum

BIT	NAME	PWD	DESCRIPTION
7	-	0	Reserved
6	-	0	Reserved
5	SPCNT [5]	1	Program the period of spread spectrum.
4	SPCNT [4]	0	
3	SPCNT [3]	0	
2	SPCNT [2]	1	
1	SPCNT [1]	1	
0	SPCNT [0]	1	

Note: The Register 15:17 slew rate control select bit fit value Please fellow below table.

The S1_N is S1 complementary and S2_N is S2 complementary, please fit complementary value.

S1:S2	S1_N: S2_N	SLEW RATE STATUS
10/01	01/10	Normal
11	00	Strong
00	11	Weak

1.4 Register 15: Slew Rate Control

BIT	NAME	PWD	DESCRIPTION
7	REF_S1	0	Pin 48 REF output slew rate control bit. This slew rate status default is Weak.
6	REF_S1_N	1	
5	REF_S2	0	
4	REF_S2_N	1	
3	3V66_S1	1	Pin 20,21,22, 3V66 [1:3] output slew rate control bit. This slew rate status default is Normal.
2	3V66_S1_N	0	
1	3V66_S2	0	
0	3V66_S2_N	1	

1.5 Register 16: Slew Rate Control

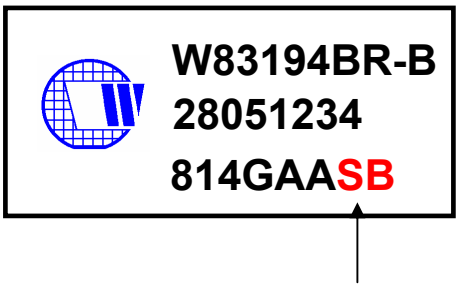
BIT	NAME	PWD	DESCRIPTION
7	PCIF_S1	1	Pin 5,6,9, PCICLK [0,7,8] output slew rate control bit This slew rate status default is Strong.
6	PCIF_S1_N	0	
5	PCIF_S2	1	
4	PCIF_S2_N	0	
3	PCI_S1	1	Pin 10,11,12,15,16,17 PCICLK [1:6] output slew rate control bit This slew rate status default is Normal.
2	PCI_S1_N	0	
1	PCI_S2	0	
0	PCI_S2_N	1	

1.6 Register 17: Slew Rate Control

BIT	NAME	PWD	DESCRIPTION
7	3V66_S1	1	Pin 31 3V66_0/VCH output slew rate control bit. This slew rate status default is Normal.
6	3V66_S1_N	0	
5	3V66_S2	0	
4	3V66_S2_N	1	
3	U48M_S1	1	Pin 34,35 48MHz_USB, 48MHz_DOT output slew rate control bit. This slew rate status default is Normal.
2	U48M_S1_N	0	
1	U48M_S2	0	
0	U48M_S2_N	1	

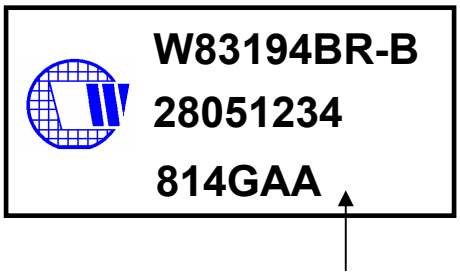
2. TOP MARKING DIFFERENCE BETWEEN VERSION A AND VERSION B.

Version B



SB included

Version A



Without SB

W83194BR-B Version Change Notices List

	DATE	VERSION	REMARK
1	10/02/06		Release Notice for A version to B version.
2			
3			
4			

Important Notice

Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Further more, Winbond products are not intended for applications wherein failure of Winbond products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.