1.1 Scope.

This specification covers the detail requirements for a complete 12-bit digital-to-analog converter with microprocessor interface, buried Zener reference and output amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number[1]
−1	AD667S(X)/883B

NOTE
[1]See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-28	28-Pin DIP
E	E-28A	28-Pin LCC

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

V_{CC} to Power Ground	0 to +18V
V_{EE} to Power Ground	0 to −18V
Digital Inputs (Pins 11-15, 17-28) to Power Ground	−1.0V to +7.0V
Ref In to Reference Ground	±12V
Bipolar Offset to Reference Ground	±12V
10V Span R to Reference Ground	±12V
20V Span R to Reference Ground	±24V
Ref Out, V_{OUT} (Pins 6, 9)	Indefinite Short to Power Ground Momentary Short to V_{CC}
Power Dissipation	1000mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 25°C/W for D-28
θ_{JA} = 60°C/W for D-28
θ_{JC} = 42°C/W for E-28A
θ_{JA} = 125°C/W for E-28A

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Table 1.

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition[1]	Units
Relative Accuracy	RA	-1	1/2	1/2	3/4	All Bits with Positive Errors On. All Bits with Negative Errors On	± LSB max
Differential Nonlinearity	DNL	-1	3/4	3/4	1	Major Carry Errors	± LSB max
Gain Error[2]	A_E	-1	0.20	0.20		All Bits On	± % FSR max
Gain Temperature Coefficient	TCA_E	-1	30		30	All Bits On	± ppm/°C max
Unipolar Offset Error	V_{OS}	-1	2	2		All Bits Off	± LSB max
Temperature Coefficient Unipolar Offset	TCV_{OS}	-1	3		3	All Bits Off	± ppm/°C max
Bipolar Zero Error[2]	B_{PZE}	-1	0.10	0.10		MSB On, All Other Bits Off Bipolar Mode	± % FSR max
B/P Zero Temperature Coefficient	TCB_{PZE}	-1	10		10	MSB On, All Other Bits Off Bipolar Mode	± ppm/°C max
Input Resistance	R_{IN}	-1	15				kΩmin
			25				kΩ max
Reference Output Voltage[3]	V_{REF}	-1	9.9 10.10	9.9 10.10	9.9 10.10	Bipolar Mode, V_S = ± 11.4 0.1mA External Load	+ V min + V max
Output Current	I_{OUT}	-1	5				± mA min
Output Short-Circuit Current	I_{SC}	-1	40				+ mA max
Latch Functionality	$A_{F\Delta}$	-1	1	1	1	See Notes 4 & 5	± LSB max
Latch Functionality	$V_{OS\Delta}$	-1	1	1	1	See Note 4	± LSB max
Power Supply Rejection Ratio	PSRR	-1	10	10		All Bits On + 11.4V ≤ V_{CC} ≤ + 16.5V	ppm of FSR/% max
			10	10		All Bits On - 11.4V ≤ V_{EE} ≤ - 16.5V	
Power Supply Current	I_{CC}	-1	12	12		V_{CC} = + 16.5V, V_{EE} = - 16.5V I_{CC}: All Bits On	+ mA max
	I_{EE}	-1	25	25		I_{EE}: All Bits On	- mA max
Digital Input High Voltage	V_{IH}	-1	2.0	2.0	2.0		+ V min
			5.5				+ V max
Digital Input Low Voltage	V_{IL}	-1	0.8	0.8	0.7		+ V max
Digital Input High Current	I_{IH}	-1	10	10		V_{IH} = 5.5V	+ μA max
Digital Input Low Current	I_{IL}	-1	5	5		V_{IL} = 0.0V	+ μA max
Data Setup Time[6]	t_{DC}	-1	50				ns min
Data Hold Time[6]	t_{DH}	-1	0				ns min
$\overline{CS}$ Pulse Width[6]	t_{CP}	-1	100				ns min
Address Valid End of $\overline{CS}$[6]	t_{AC}	-1	100				ns min
Output Voltage Settling Time[6]	t_{SL}	-1	4			R_{FB} = 10k R_L = 2k|500pF	μs max
			3			R_{FB} = 5k See Figure 1	

NOTES

[1] V_{CC} = + 15V, V_{EE} = - 15V, 50Ω resistor Pin 6 to Pin 7, A_0, A_1, A_2, A_3, $\overline{CS}$ = LOGIC "0", V_{IH} = 2.0V, V_{IL} = 0.8V, Unipolar configuration unless otherwise specified.
Unipolar Configuration – Pins 1 and 2 to Pin 9, Pin 4 to Pin 5.
Bipolar Configuration – Pin 1 to Pin 9, 50Ω resistor Pin 4 to Pin 6.

[2] Adjustable to 0.

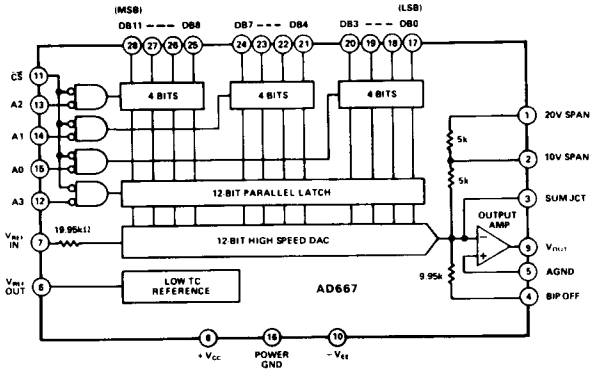
[3] In subgroup 1, the reference output is loaded with 0.5mA nominal reference current, 1.0mA bipolar offset current and 0.1mA additional current.
In subgroups 2 and 3, only the 0.5mA reference input current is applied. The reference must be buffered to supply external loads at elevated temperatures.

[4] All bits low, A_0, A_1, A_2, A_3 LOGIC "0"; A_0, A_1, A_2, A_3 initialized to LOGIC "1", each 4-Bit register set to LOGIC "1", and A_0, A_1, A_2 set sequentially to LOGIC "0" and back to LOGIC "1" to latch data into first rank.

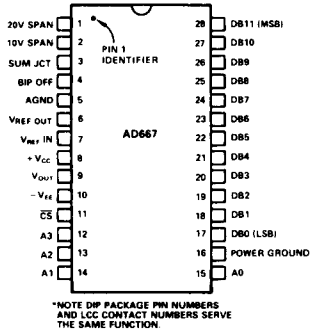
[5] A_3 set to LOGIC "0" and back to LOGIC "1" to latch full-scale output into second rank.

[6] See Figure 1 and Table 2.

3.2.1 Functional Block Diagram and Terminal Assignments.

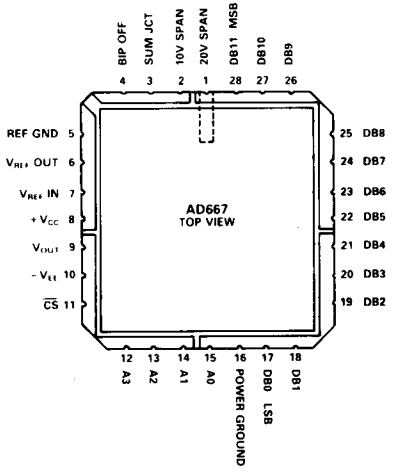


D PACKAGE (DIP)



*NOTE DIP PACKAGE PIN NUMBERS AND LCC CONTACT NUMBERS SERVE THE SAME FUNCTION.

E PACKAGE (LCC)



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (56).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

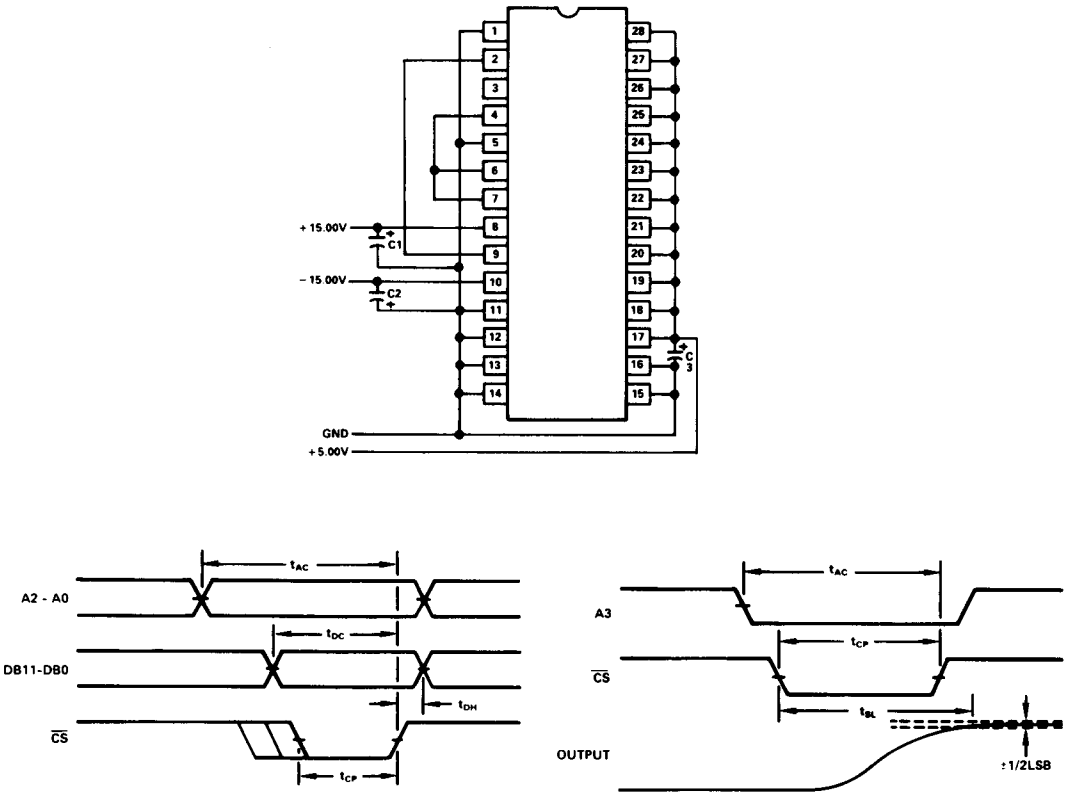


Figure 1.

Table 2. AD667 Truth Table

$\overline{CS}$	A3	A2	A1	A0	Operation
1	X	X	X	X	No Operation
X	1	1	1	1	No Operation
0	1	1	1	0	Enable 4 LSBs of First Rank
0	1	1	0	1	Enable 4 Middle Bits of First Rank
0	1	0	1	1	Enable 4 MSBs of First Rank
0	0	1	1	1	Loads Second Rank from First Rank
0	0	0	0	0	All Latches Transparent

"X" = Don't Care